Nuclear Physics Division
Data Acquisition Group

Description and Technical Information for Version 4 Trigger Supervisor (TS) Module

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1 Introduction

The Trigger Supervisor (TS) version 4 module is being designed for the Jefferson Lab 12GeV upgrade, mainly for Hall-D [(Collaboration G. , 2009)] and Hall-B [(Collaboration C. , 2009)], with other experimental Halls [(experiments, 1990)] compatibility. This module is the interface between the trigger system and data acquisition system of the experiment. The TS acts as the central control point for data acquisition. It provides a synchronous clock source to the experiment, trigger signal for the data readout, and a sync signal to align the front end electronics. Together with the Trigger Interface and Distribution (TID) modules and Signal Distribution (SD) modules, the clock, trigger and sync signals are distributed to the front end electronics, and the BUSY signals from the front end electronics are monitored. Figure 1 shows the placement of the TS module and TID modules in the global trigger distribution scheme in experiment setup.

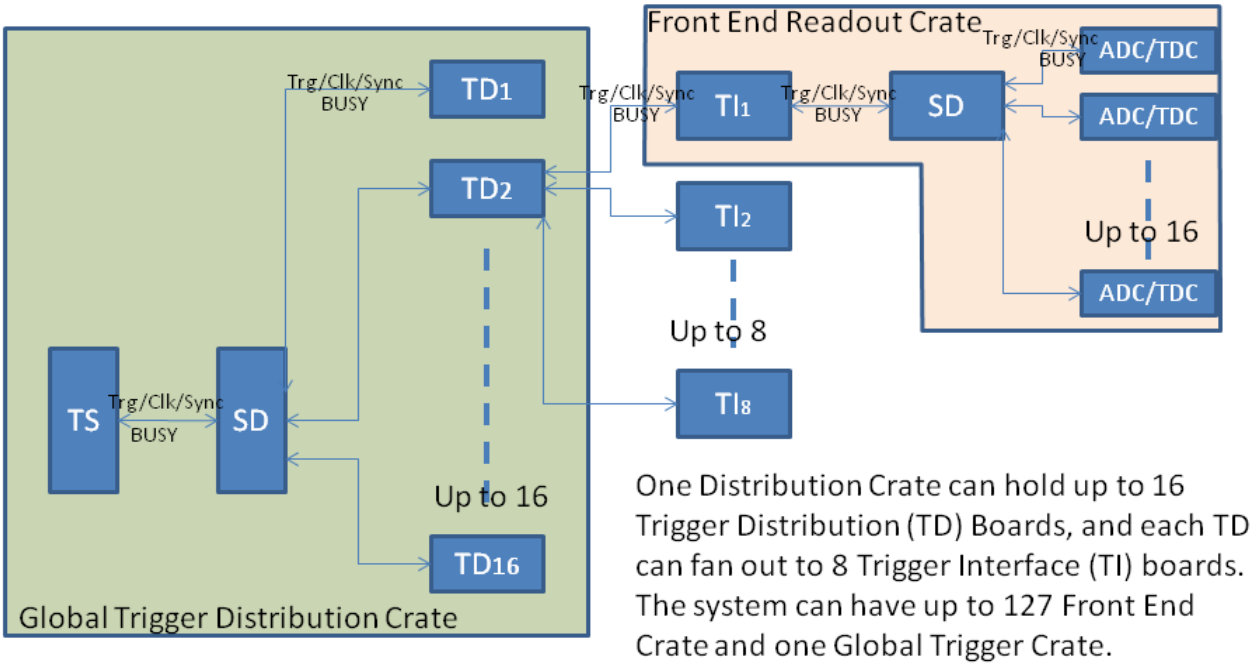

Figure 1 Trigger distribution scheme

There is one TS module in the system. It receives the trigger from GTP (in global trigger crate) through a copper cable via the VME P2 backplane. Normally, the TS is located in the last payload slot (PP#18) in the trigger distribution crate. The trigger/clock/sync signals from TS pass to the Signal Distribution (SD) module in switch slot#B. The SD will fan out the signals (up) to 16 Trigger Distribution (TD) modules located in the payload slot #1-16. Each TD can fan out (up) to 8 Trigger Interface (TI) modules in front end crates. So, the system can have up to 127 front end crates plus a global trigger crate and a trigger distribution crate. The busy signals from front end electronics can propagate back to the TS in other direction. Figure 2 shows the crate level diagram.

Within the crate, the signals are mainly transmitted via the VXS P0 connector. Fibers are used for between crates, that is, between TI and TD modules, transmission. The quad optic transceiver HFBR-7924 is used with multiple fibers. The four optical Tx/Rx pairs (between TI and TD) are assigned as following:

Tx Pair #1: Trigger, Rx Pair #1: Trigger Acknowledge, Readout Acknowledge, and Busy;

Tx Pair #2: Clock, Rx Pair #2: un-used;

Tx Pair #3: Sync, Rx Pair #3: un-used;

Tx Pair #4: loop back, Rx Pair #4: fiber latency measurement.

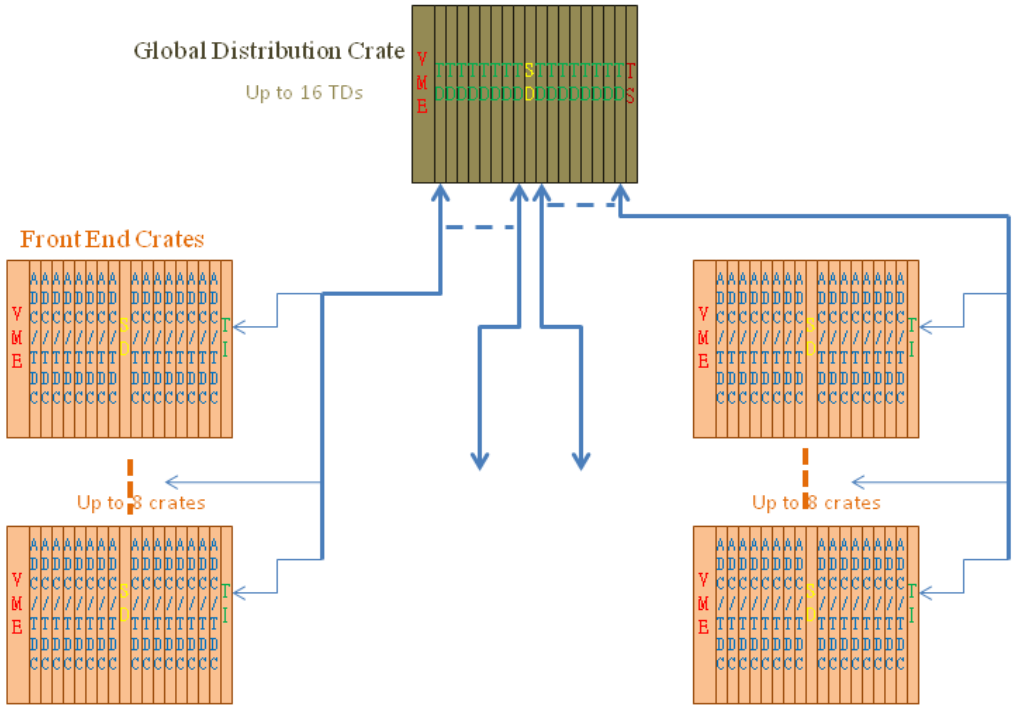

Figure 2 Trigger distribution at crate level diagram

2 Purpose of the module

The TS is the top level control module for Data acquisition system. It receives trigger from trigger system. It controls the trigger signal to generate events. The input to the TS is trigger, the output from the TS is event.

The TS in the global trigger distribution crate receives 30 level one trigger primitive signals and two source synchronizing clocks from the Global Trigger Processor (GTP) via four copper cables through a VME transition card on VME P2. The TS receive another 30 trigger signals and two source synchronizing clock signals from the front panel connectors. TS also receive another 15 asynchronous trigger signals from another front panel connector. The TS can pre-scale the primitive signals, and generate final event trigger signals to initiate data acquisition process, taking into account of the front-end electronics status (BUSY for example).

In addition to the trigger generation from GTP and front panel, the TS can also accept up to 256 kinds of calibration triggers by VME command, random triggers, and predetermined number of triggers by VME. The TS supports more than 2048 different event types (11 bits). The 11-bit trigger type, together with another two-bit trigger source, will be sent to the front end electronics via TI/TD modules. If the front-end electronics buffer is

(almost) full (defined as BUSY), or the trigger generation is inhibited, the TS will not generate event signal to initiate further data readout, instead it will start a dead time counter as data acquisition efficiency.

The TS will supply the experiment with a synchronous 250 MHz clock, which can be sourced by either an on-board oscillator or an external input through the front panel. The trigger data (16-bit word including 11 bit as trigger/event type) will be serialized by the derived 62.5 MHz (250 MHz divided by four) clock.

The TS will generate a SYNC signal to align the trigger signals received by the TI boards through their deserializers.

Another purpose of the TS is to control the data acquisition. If the data acquisition cannot keep up with the trigger, the data buffer on front end electronics may overflow. The front end can assert a BUSY signal, and the BUSY will propagate to the TS. The TS can make decision to limit the trigger rate (for data readout), or even stop the trigger completely. If the trigger is inhibited (by asserting the inhibit signal from front panel), the TS will block all the triggers for data acquisition.

There are two optional optic links which is using the same front panel space as clock input and clock output. With these two links, the TS can directly connect to the Trigger Interface board (without Signal Distribution board and Trigger Distribution board). This is especially useful when integrating with Global Trigger Processor and testing the trigger system. The TS will behave like a “mini” trigger distribution crate. The TS can also drive the P0 connector in pulse mode, so that the TS behaves like a TI itself.

3 Functional Descriptions

3.1 General description

Figure 3 shows the block diagram of the TS module, indicating the major components used in the design. A Xilinx XC5VFX70T-FG1136 FPGA is used to generate the trigger (from three sources) for data readout. It also interfaces with VME, serializes the trigger data at 16ns interval and distribute to the front end electronics. It generates the SYNC signals to align the whole experiment. The FPGA may also limit or disable the trigger depending on the front-end status. The clock is distributed by the MC100LVEP111, a multiplexer and fan out clock driver component. The simple fan-out structure will not introduce unnecessary jitter on the clock.

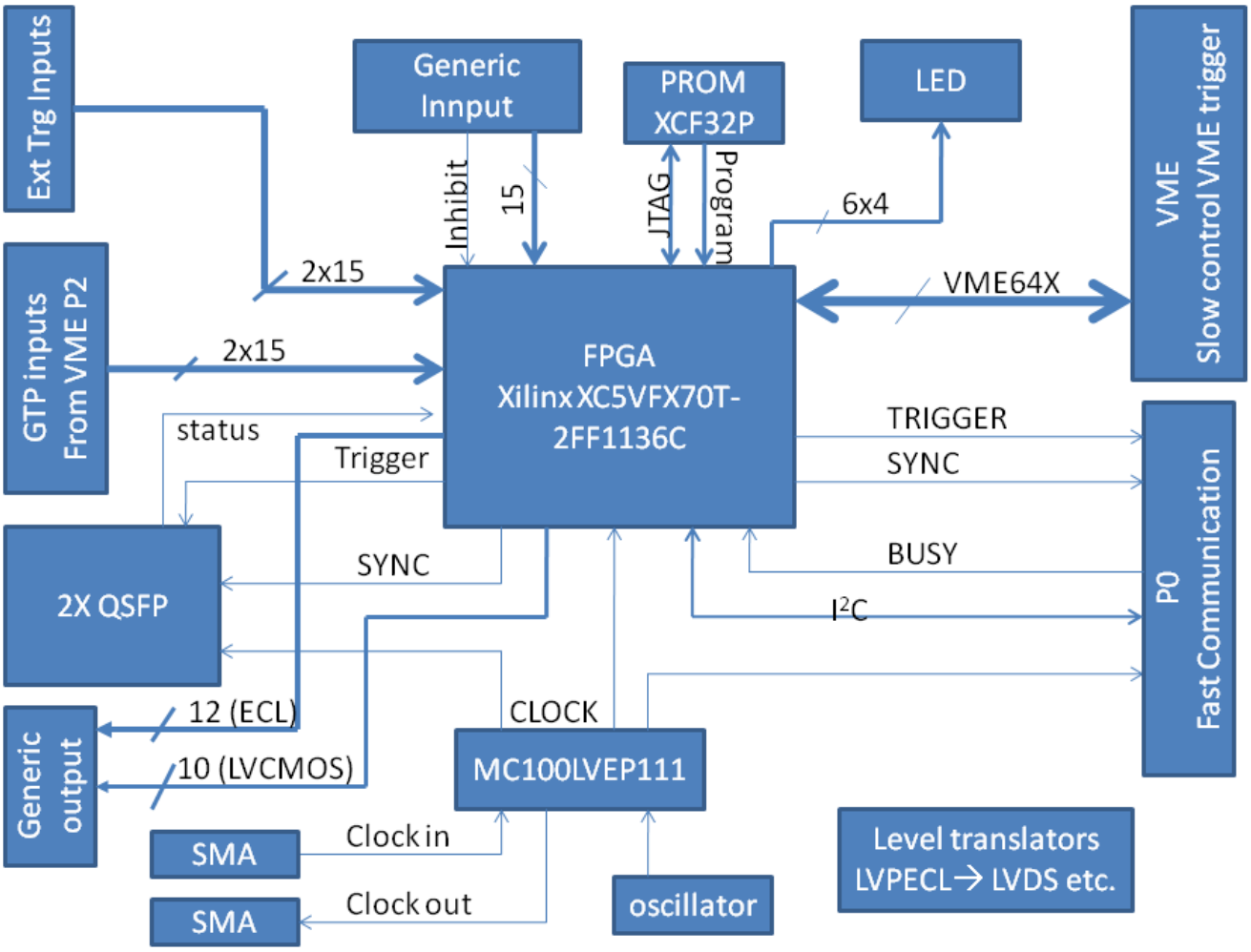

Figure 3 Trigger Supervisor (TS) functional diagram

3.2 Fiber links

The AFBR-79Q4Z is a multi-channel (4 Rx, 4 Tx) fiber optic link. It is more advanced technologically than HFBR-7924, and it is cheaper too, as it is widely used in Infini-band applications. For the TS, two modules are put on the front panel. The two QSFP modules give the TS extra flexibility, that it can bypass the SD-TD network, and distribute triggers directly to two TI modules in the front end crates. The TS will serve as a "mini" trigger distribution crate with full Global Trigger Processor board inputs. If this feature is not necessary, the two QSFP is connected to FPGA MGT transceivers, each can be a four channel full duplex transceivers for data testing. With the potential of MGT, the total data rate can be > 40Gbps. (The XC5VFX70T MGT limit is 6 Gbps per channel)

The AFBR-79Q4Z will have Trigger, Clock, Sync as Tx channels, trigger acknowledge and BUSY as Rx channel. And another generic Rx/Tx pair for future expansion (as the extra Xilinx GTP modules in the FPGA allows), or four channel full duplex transceivers for future development.

3.3: Clock generation:

One of the TS's major functions is the pipeline clock generation. The clock is generated by its on-board low jitter oscillator (Crystek CCPD-034M-50-250, 250 MHz). The TS can also accept an external input through front panel. The external clock input can also give the flexibility of using an accelerator synced clock if we can get one and we need to.

The clock is distributed to FPGA, two optical links, and through P0 to SD. The FPGA will generate other frequencies as needed from the 250 MHz clock. The MC100LVEP111 is used for the clock distribution.

3.4 Trigger generation (Event type generation):

The trigger generation is the most important function for the TS. The Data Acquisition system treats each trigger as one event, and the pipeline front end data are grouped by events, or triggers. The trigger system (electronics) generates the level one trigger primitives. It is up to the TS to match the trigger with the DAQ events. The TS should maximize the DAQ efficiency without messing up the events.

The trigger input signals can be extended to cover the full event. Because of the trigger primitive natural latency uncertainties (detector signal flight time etc), this signal extension will match the event to the real beam collision. An extra inhibit window can also be set to veto the next event, so no two events will be generated from the same collision. These two parameters can be adjusted between 16ns to 500ns.

The earliest trigger primitive timing will be used to tag as the event timing. The precision for this is 4ns. This timing information will be sent as part of the trigger word to the TI, so the TI has the option to generate trigger (decode trigger) in 4ns precision.

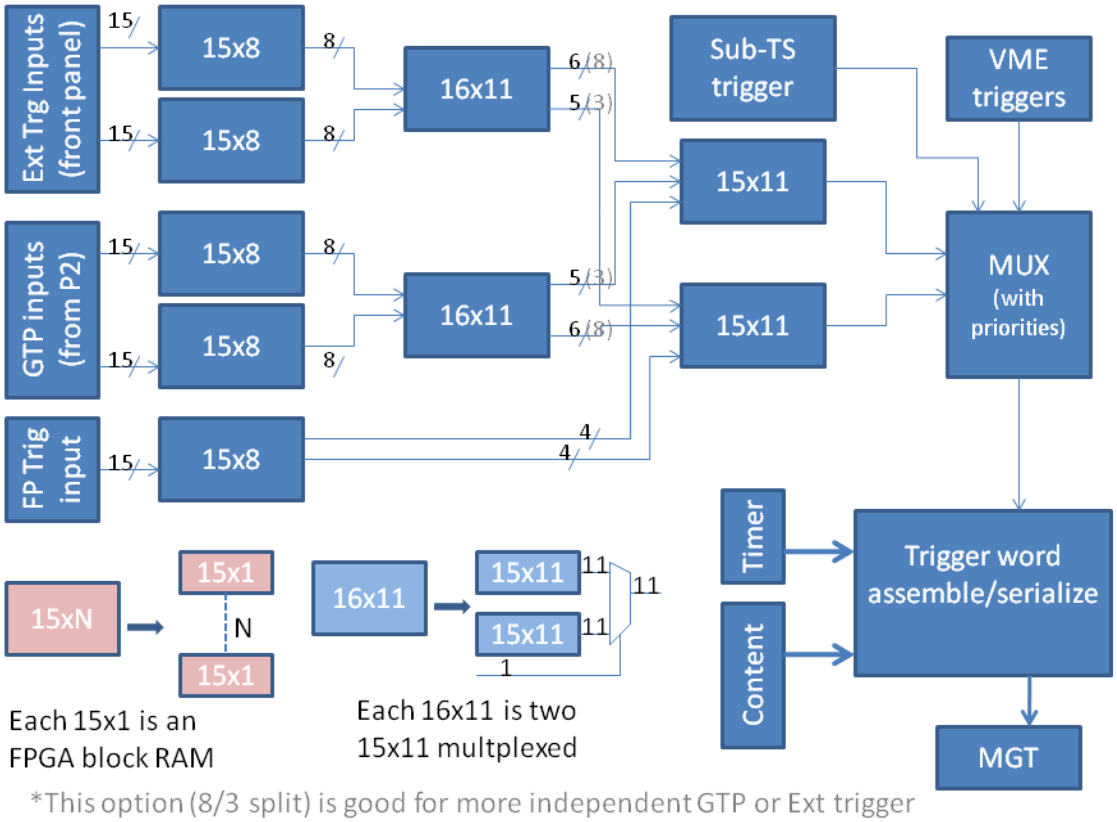

Figure 4 Trigger (event) generation in TS

The trigger primitives (GTP inputs or external inputs) can be realigned (width extended) and pre-scaled before being used to form a trigger type. The trigger type is a look up table with 75 address inputs and two 11 bits outputs. This is implemented using the block RAM in the FPGA. The lookup table is implemented physically by 106 36Kbit blockRAM modules inside the FPGA. The block RAM can be set to a default by firmware. The lookup table can be reloaded every time the power is up, or the trigger pattern needs be changed. In standard VME A24 access, the loading takes less than 1 second. It is possible that the tables be reloaded by an external non-volatile flash memory. This will speed up the trigger reconfiguration without re-compiling the FPGA.

The detailed GTP trigger primitive inputs and their lookup table structure is also shown in the above figure. If the trigger type is going to be sent in one trigger link word, the trigger type will be limited to 10 bit (1K types). The asymmetric trigger type definition is used with the details shown in next table in section 3.8.

If there are trigger collision, which means that two or more triggers are needed to send in the same time window (16 ns), or there is one trigger, but the front end electronics is busy, or the trigger is inhibited, the trigger collision will be generated. In this case, the trigger will be lost (or the higher priority trigger be generated, and the lower priority trigger be lost). The trigger collision condition is sent out. The TS will record the busy time. Together with the live time, the TS is recording the trigger efficiency, or data acquisition efficiency.

3.5: TS partitions (Sub_TS)

The TS can also generate triggers as four mini trigger supervisor boards (Sub-TS). The sub-TS works in parallel with the main TS functions. Each sub-TS has its own event type look up table and data stream.

Each sub-TS can have up to 13 trigger inputs. These 13 trigger inputs can generate up to 7 different event types by a lookup table implemented by the FPGA block RAM. The user can choose any five trigger inputs from the 30 GTP triggers, any five from the 30 front panel synchronous inputs (external trigger), and any three from the 15 front panel asynchronous trigger inputs. The seven event type is encoded in three bits (code 0 is excluded). Figure 5 shows the diagram of one sub-TS event type generation.

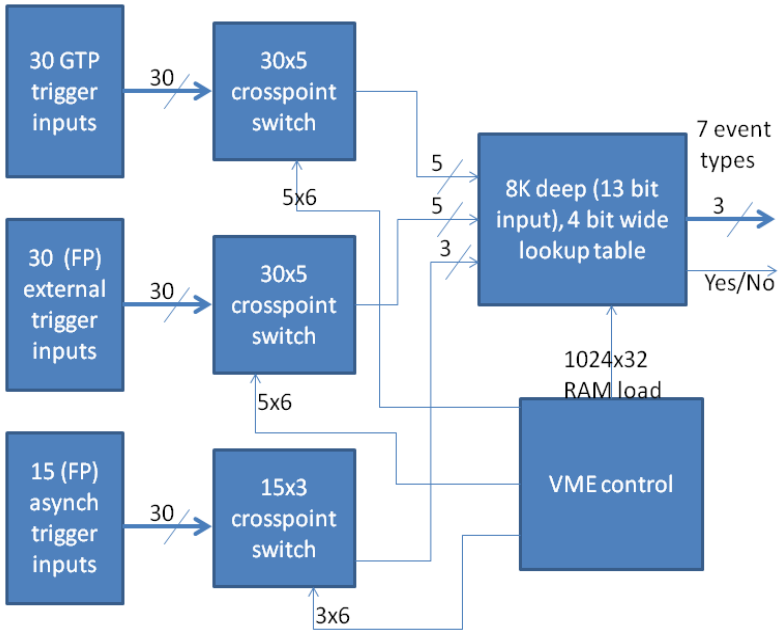

Figure 5 sub-TS event type generation

The four sub-TS work in parallel. Trigger word with bits (15:12) = “1011” indicates that the trigger word is a sub-TS trigger strobe. The detailed trigger word is in section 3.8. Each sub-TS event type uses three bits of the lower 12-bit of the sub-TS trigger strobe word. There is no sub-TS trigger timing information, nor trigger content word. The sub-TS can also work together with the normal TS, though the normal TS trigger strobe has higher priority than the sub-TS trigger strobe word.

In this way, the TI can decode both the standard TS trigger strobe word and sub-TS trigger strobe word. The TI needs to know which sub-TS to enable (extra trigger source). Actually, one TI can respond to multiple sub-TS (partition) triggers.

The TS has trigger data per event, which can be read out by the A32D32 access (and up to 2esst). Each sub-TS has its own event data, which can be read out by VME A24 D32 single word access.

3.6: Serial Flash Memory

A 4Mb (at least) serial flash memory can be used to store the trigger lookup tables. When the TS is powered down, the memory retains the trigger table. When the TS is powered up, the board will automatically load the lookup table back to the FPGA to initialize the block RAM (as the block-ram is much faster than the external flash memory). If the trigger table is going to be changed (for example, different trigger modes), the user need load the new trigger table into the flash memory, then send a VME command to load the block-ram by the flash memory. In this case, the TS is still operating in the previous trigger mode while the new trigger mode (lookup table) is being loaded. But as the lookup table needs less than one second to load through VME, there is really little point to use this serial flash memory. (The Serial flash memory needs 1 second if the clock is 4MHz).

3.7: Fixed Latency CLKSYNC

The CLKSYNC signal is a 250Mbps serial line that operates in synchronous mode. This serial link allows a 4bit command to be sent at chosen 4ns points in time. CLKSYNC is synchronized to the master clock CLK250 and is sampled every 4ns cycle. The line is considered to be idle when more than 4 samples in a row are read ‘1’. A command is sent between idle times by sending first a ‘0’ followed by the 4bits that comprise the command, LSB first. After the command has been sent, a final ‘1’ is sent so that the line will return back to the IDLE state. The encoding portion of this serial protocol is performed on the TS in the FPGA. The CLKSYNC output from the FPGA can be delayed (time adjustment) by the FPGA IODELAY. As the clocks are synced and sourced by the TS, this delay setting is not expected to change between different firmware versions. The TS will send the CLKSYNC to the TD boards via P0 and SD. The TD will fan out to the TI boards via optical transceivers. The CLKSYNC transferred is Manchester encoded version of CLKSYNC, which balanced the differential lines.

The CLKSYNC is synchronized across the TI boards by applying different delays on the signal which is determined by measuring the fiber latency. The CLKSYNC link is used in conjunction with a synchronous FIFO to enforce a fixed latency on the serial trigger link. On the TI board, the trigger word is clocked into a FIFO using the FPGA built in RocketIO MGT transceivers and the user clock, which is the same as the external 62.5MHz clock. Data words are clocked out of the FIFO using a 62.5MHz clock derived from (and in phase with) the system CLK250. At startup the FIFO is reset (0 words) and reading the FIFO is disabled. No words are written into the FIFO since the TS is not yet transmitting data words on the trigger link (i.e. received data valid signal is not asserted). Acceptance of triggers by the TS is also disabled. On trigger start, the TS starts transmission (time words) on the trigger link, and after a fixed number of 62.5MHz clock cycles, the TS issues a TRG_START

command on the CLKSYNC line. When TI receives valid TS data, it writes to the trigger word FIFO, but the FIFO will not be readout until the TI receives the TRG_START command on CLKSYNC line. In response to the TRG_START command, the TI resets the trigger FIFO readout address, and enables continuous readout of the FIFO. The trigger words from the TI board FIFO are synchronized across the system. In TS and TI MGT transceivers, the phase alignment is used to remove the elastic buffer delays as the Tx/Rx are using the same clock (or the clocks generated from the same clock). This is illustrated in figure 6:

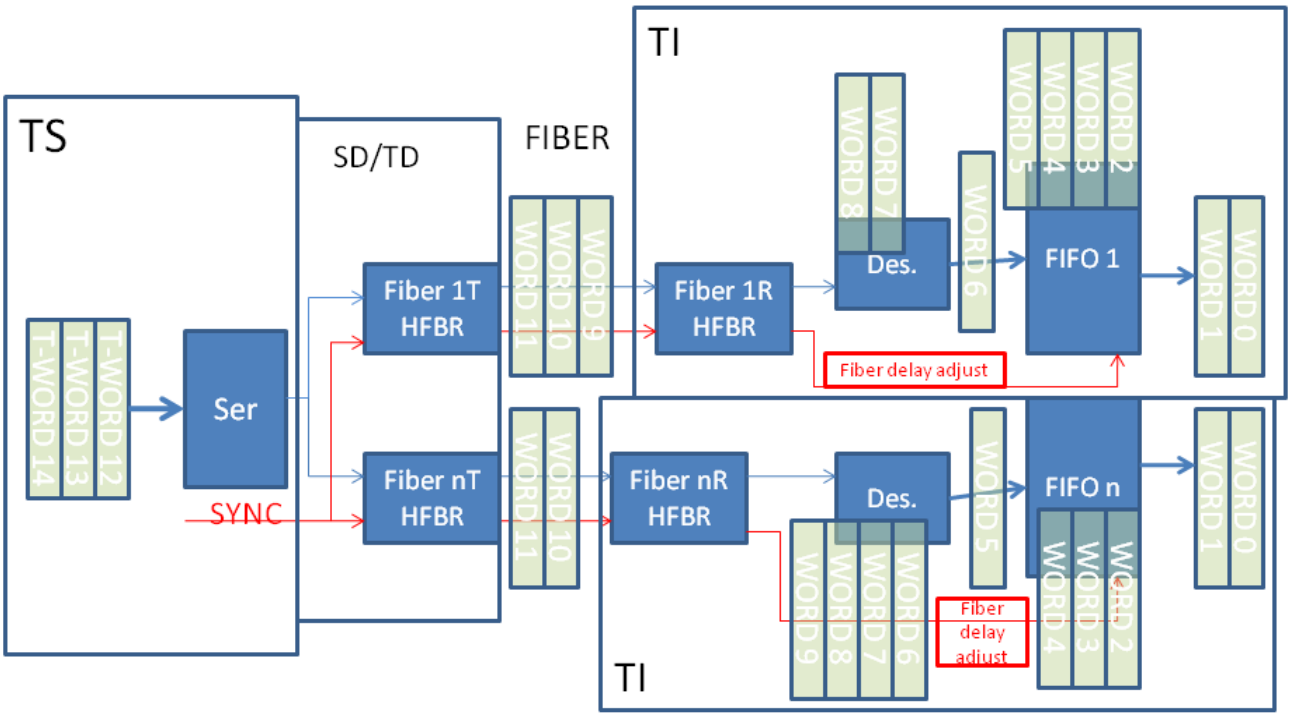

Figure 6 Illustration of the Global Trigger Synchronization process

The CLKSYNC link is also used to synchronize the lower frequency clocks derived in the TI from the distributed system clock (CLK250) have the same phase across all TI boards in the front-end data acquisition system. At startup, the TS issues a CLKSYNC command CLKRESET, which is phase aligned with the 62.5MHz clock on TS. This signal resets the clock distribution chip (AD9510) in each TI on the same CLK250 edge, assuring that the lower frequency clocks (125MHz, 62.5MHz, 41.67MHz and 31.25MHz) are in phase across the entire system. This command is sent before the TI sync command. The delay between them is determined by the maximum RocketIO MGT reset recovery time, as the MGT clock is changed (AD9510 clock reset). The time could be several milliseconds.

3.8: Encoded Trigger Word

A 1.25Gbps serial link operating over the fiber link, is used for distributing a 16bit trigger word every 16ns. There is also a link going in the opposite direction, allowing status words to be sent back to the trigger distribution crate. The 16bit trigger words are decoded as follows (TS->TD->TI flow):

Trigger strobe word – generated by the TS in response to the acceptance of a level 1 trigger as a DAQ event. Upon receipt, the TS encodes this word with highest priority. The TS transmits this word with fixed latency relative to the accepted trigger. Two-bit timing information is added in the word to distinguish which quadrant of the 16 ns period the trigger is generated, so it is fully compatible with the 4ns pipeline design architecture. The TI can distribute trigger signal in 4ns precision. This could potentially reduce the FADC readout window width, and reduce the event size.

Trigger content word – additional information about this trigger event for use by the ROCs. It is queued in a FIFO and sent in any frame not used by a trigger strobe word. The TID matches the trigger strobe and trigger content words by the order of their reception.

Control Word – establish synchronization, request status, or other command. They can be queued in a FIFO and sent in any frame not used by a trigger strobe word. Right now, this is connected to a VME register directly. The decoding is depending on the TI.

Master Time Word – since the link must always be transmitting valid data to keep its latency fixed, bits [13:2] of the TS time is transmitted whenever no other word types are available. Bit(1:0) is transmitted in trigger strobe words. By continuously receiving bits [13:2] of the TS time, each TID can promptly detect if its subsystem has lost global synchronization (i.e. compare the global time with its own time). Otherwise, the loss of synchronization could only be detected at the event building stage. The continuous transmission of 'known' (i.e. predictable) data also allows one to monitor the integrity of the link.

This table shows the format of the trigger word (as decoded on the TI prototypes).

Bit13	Bit12	Word Type	Meaning of Bit[11:0]
0	0	Time	Lower 12 bits of TS time (bit(13:2))
0	1	Control	Control or Command
1	0	Trigger Strobe	Trigger type/Trigger quadrant: Bit(11:2): trigger source and trigger type Bit(1:0): trigger time, 4ns quadrant
1	1	Trigger Content	Additional Trigger data

Bit[15] is used for error detection, right now, this is a simple parity bit; bit[14] = not Bit[15]

This table shows the format of the trigger word (Proposed for new firmware).

Bit15	Bit14	Bit13	Bit12	Meaning of Bit[11:0]		Word Type
0	1	0	0	Lower 12 bits of TS time (bit(13:2))		Time
0	1	0	1	Control or Command		Control
0	1	1	0	Trigger Source/Trigger Type Bit(11:10): trigger source (random, regular …); Bit(9:0) trigger type		VME Trigger Strobe
0	1	1	1	Additional Trigger data		Trigger Content
1	0	1	0	0	Trigger type A, time(1:0)	Trigger Strobe A

1	0	1	0	1	Trigger Type B,		time(1,0)	Trigger Strobe B
1	0	1	1	subTS#4	subTS#3	subTS#2	subTS#1	

The Trigger content words include an event counter. The TI can use this content word to check its synchronization if any trigger is missing by the TI/TD. The trigger format can be easily changed as long as the TS encoding and TI decoding are consistent.

3.9 VME interface

The TS is a VXS payload board. It is compatible with VME64x backplane. Normally, it is a VME slave board, with interrupt capability. The TS is implemented the same way as the TI/TD board.

For simplicity, three kinds of VME address modifier codes are implemented. (1), User defined address modifier. This is similar to the A24 address modifier. It is used to load the PROM by the on-board discrete components. (2), Standard A24 address modifier. This is used to read/write the registers on the FPGA, slow controls of the TS peripherals. (3), A32 data transfer. This is used to transfer data to the ROC (Read Out Controller). For the details of A32 mode support, refer to the VME interface design (Ed, 2010) .

3.10: The Xilinx PROM programming.

The Xilinx XCF32P PROM is used to program the FPGA. It can save one version of the (XC5VFX70T) FPGA firmware when it is used in non-compression mode. It can save two versions of the firmware when bit stream compression is used, and the FPGA resource usage is not too high. The PROM is programmed using VME with emergency logic decoding (that is: discrete logic VME to JTAG engine). It can be addressed in the VME64x crates by its geographical address. If it is in the crate without geographical address, only one TS or TID in the crate should be addressed as geographical slot#0. To avoid conflict with other VME addressing, the user-defined address modifiers are used for the PROM loading. The emergency logic supports A24D32 user defined address modifier codes: 0x19, 0x1A, 0x1D and 0x1E (Similar to 0x39, 0x3A, 0x3D and 0x3E). Out of the data, bit[1] is used for TDI, bit[0] is used for TMS, and all the other 30 bits are unused. This approach is fully tested on TI/TD boards. This emergency loading provides VME remote firmware re-loading and broadcast firmware loading even if the FPGA is not working. One 33 MHz on-board oscillator is used to program the FPGA, and used by the FPGA for slow control. The PROM needs be in master mode if bit compression is used.

The PROM can also be programmed by the on-board JTAG connector and VME-JTAG engine (after the FPGA is programmed and working) implemented in the FPGA. The JTAG engine in the FPGA provides VME remote firmware loading when the FPGA is working with more efficient VME data transfer.

3.11: Serial data communication with SD and other switch slot modules

As there is no VME access to the switch slots (SD for example), the TS has implemented an I^2C bus to each switch slot. The TS will act as I^2C master, and the switch slot module acts as slave. The I^2C is FAST mode with higher clock frequency. For details, refer to the VME to I2C implementation [(GU, 2010)] documented earlier.

The TS can communicate with the switch slot module via a 250Mbps link, (it is possible to increase it to 500 Mbps using DDR techniques). This is implemented using the Xilinx SelectIO standard differential IO pin pair. The switch slot module can also send data to TS using this link. The direction of the data link depends on

the firmware (TS and SD) implementation. This can serve as a complimentary to the slow I2C interface as one possible usage.

3.12: Trigger data receivers

The Micrel SY55855 LVDS receiver is used to receive the GTP data from P2 backplane. The output (LVDS) goes directly to the FPGA for processing.

The Maxim max9602 is used to receive the trigger input from the front panel (external trigger in or generic input). The max9602 uses -5 as VEE, +5 as VCC and +2.5V as Vout. So, it can receive any differential input with common voltage of -2V to +3V (which includes ECL, LVDS, LVPECL …), and the LVPECL25 output is compatible with the extended LVDS input of the FPGA.

4. Specification Sheet

4.1 Mechanical

Single-width VITA 41 Payload Module with the size of 6Ux160mm. It will be positioned in the PP18 of global clock/trigger distribution crate. If there is no SD in the crate, the TS can be plugged in any of the payload slots to act as a "mini" trigger distribution crate.

4.2 High speed serial P0 inputs:

BUSY LVDS signals on P0;

I^2C to VXS Switch slot# B, switch slot #A;

High speed LVDS data link (can be output too).

4.3 High speed serial P0 outputs (LVPECL):

Two 250 MHz clock to Switch slot#B; one to the switch slot#A;

1.25 Gbps Encoded (serialized) TRIGGER Signal, or pulsed Trigger1 and Trigger2;

250 Mbps Manchester encoded SYNC Signal;

Pulsed trigger, which used the Trigger2 line on SD to distribute trigger to TD boards.

4.4 High speed P2 GTP trigger primitive inputs:

250 Mbps GPT trigger primitive inputs via a backplane transition board;

P2 Row A and Row C are used, 32-pairs for 32 GTP inputs (the 1st and 17th pairs are used as data source synchronized clock);

LVPECL Signal;

Some of the 32-pairs may not be used.

4.5 External trigger inputs:

30-bit differential external trigger in four groups with 7/8 bits per group;

Two source synced clocks

4.6 Front panel general inputs:

16-bit general purpose differential inputs, which could be additional 15-bit asynchronous trigger inputs and one trigger inhibit (or busy) bit on 34-pin connector;

250MHz Clock Input (SMA), LVPECL input;

4.7 Front panel general outputs:

10 LVCMOS single-ended outputs (TS status);

12 ECL differential outputs (TS status);

250 MHz clock output (SMA) LVPECL.

4.8 Fiber channel signals: two AFBR-79Q4Z modules

CLKSYNC Fixed Latency Link

250Mbps Serial Communication

Manchester Encoded

CLKSYNC to CLK skew variation < 1ns

This link can optionally been connected to the FPGA's MGT Rx/Tx directly;

TRIGGER_TX/STATUS_RX

1.25Gbps Trigger Word Line

Provides 16bit parallel data every 16ns

A BUSY status word in the opposite direction, which also includes trigger acknowledge, and front end data readout acknowledge.

This link is connected to the FPGA's MGT Rx/Tx directly;

CLK

250MHz low jitter clock

This link can optionally been connected to the FPGA's MGT Rx/Tx directly;

SPARE

Generic Rx/Tx pair connected to the FPGA MGT transceiver with loopback capability.

4.9 Indicators: Front Panel:

Six sets of LEDs on front panel:

Set 1 (LEDA): TS board status

FPGA is ready;

Board OK;

Lengthened trigger active;

Lengthened VME DTACK indicator.

Set 2 (LEDB): External 30-bit trigger input indicator;

Set 3 (LEDC): GTP 30-bit trigger input indicator;

Set 4 (LEDD): AFBR-79Q4 status

Set 5 (LEDE): 10 LVCMOS, 12 ECL outputs status

Set 6 (LEDF): 15-bit asynchronous trigger inputs and inhibit

On board:

Power OK near each regulator or DC-DC converter;

FPGA program DONE;

4.10 Programming:

VME64x, A24/D32, A32/D64 slave

4.11 Firmware loading:

VME to JTAG A24D32 with user defined AM (Address Modifier) for remote firmware loading with redundant On board JTAG connector;

Custom VME to JTAG engine implemented in the FPGA using A24 standard AM.

It is possible that two revisions of the firmware be stored in the PROM simultaneously, with one as backup; or as two different configurations of TS.

4.12 Power requirements:

+3.3v @ 1.5 Amps; +5V @ 4 Amp; +12V, -12V @ 0.3 Amp (From Backplane), total < 35 W;

DC-DC converters for +1.8V, +2.5V, +3.3V and -5V, and Local regulators for other required voltages: +1.0V, +1.2V, +3.3V clock.

4.13 Environment:

Forced air cooling: Weiner standard

Commercial grade components (0-75 Celsius)

5 TS operation procedure:

The TS needs be properly set and plugged into the proper crate and slot. Damage may happen to the TS, the crate, or other PCBs in the crate if the right procedure is not followed.

5.1 TS Power supply:

The TS use +3.3V directly from VME64x crate. It can also generate its own +3.3V supply by a DC-DC converter from +5V from VME. This switch is selected by loading the on-board FUSE or DC-DC converter. To avoid conflict, do not populate both (VXS crate is a VME64x compatible backplane).

5.2 Hardware setting (Switch etc.):

A 8-bit switch is used to set the TS working mode:

Bit8: LVPECL, open=high, Clock source selection. When high, the clock source is on board oscillator; when low, the clock source is front panel clock inputs; The switch setting can be overwritten by a software setting (FPGA pin drive).

Bit7: open=high, A24 address space selection. When LOW, use the VME64x GA(4:0); HIGH, use the switch bit(5:1) as A24 address space setting;

Bit6: FPGA firmware revision selection, low: revision 0, high: revision 1; This can be overwritten by the FPGA MULTIBOOT RS0 if the revision 1 should fail (and if rev1 is selected).

Bit(5:1): A24 address space A(19:23). As the TS and TD are the only VME custom modules in the global trigger distribution crate, the switch Bit(5:1) and Bit7 will most likely be left unused as both the TS and TD support the Geographic address GA(4:0), and the VXS crate is VME64x compatible.

5.3 Software setting:

After the board is properly set, and plugged in the right slot, some software setting needs be applied for the board to work. Some parts of the board needs be powered down to reduce the power consumption. The FPGA MGT transceivers will be automatically powered depending on the mode setting. The TS software setup sequence: (The TS may not work if the sequence is not followed)

- TS clock selection: This is important for the trigger distribution system to work properly
- Trigger table loading: This is the most important step, and it is required every time the TS is powered up, or the FPGA is reprogrammed;
- Some other reset/initialize in specified order.

6. VME Programming Requirements

There are three categories of Address Modifier codes are supported on the TS: the user-defined Address Modifier codes (A24) for emergency firmware loading; Standard A24 for FPGA register read/write and slow control; A32 block transfer for VME data readout. The A24 address space is set by the 5-bit Geographical address of the VME64x backplane or the onboard binary switch (as mentioned in section 5.2).

6.1 VME to JTAG emergency loading:

The AM[5:0] user defined codes are used for this logic. This works even before the FPGA is programmed and working. It is almost the same as A24D32 mode. The valid AM codes are: 0x19, 0x1A, 0x1D and 0x1E. These AM codes are user defined, and similar to the AM codes 0x39, 0x3A, 0x3D and 0x3E.

The valid address bits are A[31:24] do not care; A[23:19]=GA[4:0] for VME64x crates, or A[23:19]=0 for non-VME64x crates; A[18:2]=b’00011111111111111.

Data bit[1] is used for TDI; data bit[0] is used for TMS.

For example, if the board is in slot#5 (that is ~GA(4:0)= 11010), you need write to A(23:0)=0x28fffc.

If data(1:0)=00, both TMS and TDI will be low;

if data(1:0)=01, TMS is high, TDI is low;
if data(1:0)=10, TMS is low, TDI is high;
if data(1:0)=11, both TDI and TMS are high.

The normal A24 address should try to avoid this address (0x0fffc).

A more advanced example: Instruction register shift (8-bit, shift in 0x5a) starting from/end up at the 'reset idle' mode: 14 consecutive writes to the address 0x28fffc with AM=0x19, 1a, 1d or 1e, the data are 1, 1, 0, 0, 0, 2, 0, 2, 2, 0, 2, 1, 1, 0 respectively.

Data	1	1	0	0	0	2	0	2	2	0	2	1	1	0
TMS	H	H	L	L	L	L	L	L	L	L	L	H	H	L
TDI	0x	0x	0x	0x	0	1	0	1	1	0	1	0	0x	0x

"TMS H" means logic High, "TMS L" means logic Low, "TDI 0" means 0 or Low, "TDI 1" means 1 or High, and "TDI 0x" means DO NOT CARE by the JTAG, but the set value is 0.

6.2 Configuration Registers:

A24D32 are used for register read/write. Similar to the emergency loading logic, the base address is determined by the Geographic Address in VME64x crate, and external switch for non-VME64x crate. That is, A[23:19]=GA[4:0], or SW[5:1]. [0xXX, BIT(m,n)] means the register offset and bits in old TI firmware design.

- Address offset: 0x00000: Board ID:

  Bit 7-0 (R/W): Crate ID; Reset default 0x00; [0x00, BIT(7:0)]
  Bit 12-8 (R): A24 address, higher 5 bits; Reset default 000 [0x54, BIT(4:0)]
  Bit 13 (R): '1': TS is in running mode, it is GA parity bit for TI;
  Bit 15-14 (R): '10': TS is in running mode (no more register changes), others: TS not in running mode;
  Bit 31-16 (R): hex 0x71D5 (0x71: TI, 0x75: TS, 0x7D: TD, 0x71D5: TIDS). [0x54, BIT(31:16)]

- Address offset: 0x00004: Optic transceiver enable:

  Bit 7-0 (R/W): on TI: HFBR#8, #7, … #1 Enable, Reset default 0xFF all enabled. [0x04, BIT(7:0)]
  Bit 0: '1' enable HFBR#1, '0' disable HFBR#1; ('disable' means 'power down')
  Bit 1: '1' enable HFBR#2, '0' disable HFBR#2;
  Bit 2: '1' enable HFBR#3, '0' disable HFBR#3;
  Bit 3: '1' enable HFBR#4, '0' disable HFBR#4;
  Bit 4: '1' enable HFBR#5, '0' disable HFBR#5;
  Bit 5: '1' enable HFBR#6, '0' disable HFBR#6;
  Bit 6: '1' enable HFBR#7, '0' disable HFBR#7;
  Bit 7: '1' enable HFBR#8, '0' disable HFBR#8;
  On TS, they set the mode for TS's two QSFP optic transceiver:

Bit 0: unused
Bit 1: FiberLP; Low Power select; but not valid for this transceiver (Class 1 power level module, 1.5W)
Bit 2: FiberMS, low true, module select; this select the module for I2C interface active.
Bit 3: FiberRst, low true, optic transceiver reset;

- Address offset: 0x00008: Interrupt setting:

  Bit 7-0 (R/W): Interrupt ID; Reset default 0xC8 [0x08, BIT(7:0)]
  Bit 10-8 (R/W): Interrupt level; Reset default 5; [0x08, BIT(10:8)]
  Bit 16 (R/W): IRQ enable. Reset default: 0; [0x04, BIT(13)]

- Address offset: 0x0000C: Trigger delay and Pulse width:

  Bit 7-0 (R/W): Trigger_1 delay, (n+1)*4 ns; Reset default 0x07; [0x0C, BIT(7:0)]
  Bit 15-8 (R/W): Trigger_1 Pulse width (n+1)*4 ns; Reset default 0x07; [0x0C, BIT(15:8)]
  Bit 23-16 (R/W): Trigger_2 delay, (n+1)*4 ns; Reset default 0x07; [0x0C, BIT(23:16)]
  Bit 31-24 (R/W): Trigger_2 Pulse width (n+1)*4 ns. Reset default 0x07; [0x0C, BIT(27:24)]

- Address offset: 0x00010: A32 address space:

  Bit 13-5 (R/W): Address Max; Reset default 0x1FF; [0x10, BIT(13:5)]
  Bit 22:14 (R/W): Address Min; Reset default 0x000; [0x10, BIT(22:14)]
  Bit 31-23 (R/W): Base Address. Reset default 0x100; [0x10, BIT(31:23)]

- Address offset: 0x00014: Block size:

  Bit 7-0 (R/W): Block size. Reset default 0x01; [0x00, BIT(15:8)]

- Address offset: 0x00018: TI data format control: Reset default 011; [0x00, BIT(31:29)]

  Bit 0: if '1', two block placeholder words are enabled; '0' disabled.
  Bit 2-1: Event format control:
  00: Shortest words per trigger;
  01: The TI timing word is enabled;
  10: The TI status word is enabled;
  11: The TI timing word and status word are enabled;

- Address offset: 0x0001C: VME setting; Reset default 0x011:

  Bit 0 (R/W): '1' enable Bus_Error_En, so the block read can be terminated by event block trailer; [0x10, BIT(0)]
  Bit 1 (R/W): '1' en_token_in is true, '0' en_token_in is false; [0x10, BIT(1)]
  Bit 2 (R/W): '1' enable 'Multi-board' readout, '0' disable 'Multi-board'; [0x10, BIT(2)]; asset to enable multi-board token passing protocol;
  Bit 3 (R/W): '1' enable en_A32m, '0' disable en_A32m; [0x10, BIT(3)]; assert to enable common A32 multi-board addressing of module;
  Bit 4 (R/W): '1' enable en_A32, '0' disable en_A32; [0x10, BIT(4)]
  Bit 7 (R/W): '1' enable VME bus interrupt for module error?
  Bit 8 (R/W): '1' I2C device address 0x1101xxx, '0' I2C device address 0x0000xxx; [0x04, BIT8]
  Bit 9 (R/W): '1' token_in high, '0' token_in low; [0x04, BIT(9)]

Bit 10 (R/W): ‘1’ first_board true, ‘0’ first_board false; [0x04, BIT(10)]
Bit 11 (R/W): ‘1’ last_board true, ‘0’ last board false; [0x04, BIT(11)]
Bit 15 (R/W): ‘1’ disable data readout buffer full [0x04, BIT(15)]

- Address offset: 0x00020: Trigger source register:

Bit 15-0 (R/W): Trigger source enables: Reset default 0x0000; [0x00, BIT(23:16)]
Bit 0: P0 trigger input;
Bit 1: HFBR#1 trigger input;
Bit 2: TS loopback trigger input; (No effect on TS)
Bit 3: Front Panel trigger input;
Bit 4: VME trigger;
Bit 5: Front Panel Trigger Codes (as Supervisor) inputs;
Bit 6: TS_rev2 trigger input;
Bit 7: Random Trigger.
Bit 8: FP/Ext/GTP trigger enable on TS;
Bit 9: P2 Busy used as Trigger input [0x28, BIT(6)]
Bit 12: SubTS#1 trigger enable, this is valid on TI only;
Bit 13: SubTS#2 trigger enable, this is valid on TI only;
Bit 14: SubTS#3 trigger enable, this is valid on TI only;
Bit 15: SubTS#4 trigger enable, this is valid on TI only;
Bit 31-16 (R): Trigger source monitor. [0x00, BIT(31:24)]

- Address offset: 0x00024: Sync Source register:

Bit 15-0 (R/W): Sync Source enables: Reset default 0x02; [0x00, BIT(28:24)]
Bit 0: P0 sync input;
Bit 1: HFBR#1 sync input;
Bit 2: HFBR#5 sync input;
Bit 3: Front panel sync input;
Bit 4: TS loopback SYNC enable
Bit 31-16 (R): Sync source monitoring. [0x28, BIT(23:16)]

- Address offset: 0x00028: Busy source registers:

Bit 15-0 (R/W): Busy source enables: [0x04, BIT(31:16)]
Bit 0: ‘1’ enable the Switch Slot #A BUSY input, ‘0’ disable;
Bit 1: ‘1’ enable the Switch Slot #B BUSY input, ‘0’ disable;
Bit 2: ‘1’ enable the VME P2 BUSY input, ‘0’ disable;
Bit 3: ‘1’ enable the FTDC front panel BUSY input, ‘0’ disable;
Bit 4: ‘1’ enable the FADC front panel BUSY input, ‘0’ disable;
Bit 5: ‘1’ enable the Front Panel BUSY, which is the same as TsRev2 busy;
Bit 6: ‘1’ Use P2 BUSY input as trigger1 input (useful and valid for TD only);
Bit 7: ‘1’ enable TS feed_back BUSY, ‘0’ disable the busy. (useful in TM mode);
Bit 15-8: HFBR #8-#1 BUSY enables: ‘1’ enable the HFBR BUSY input, ‘0’ disable;
Bit 8: TI_A busy

Bit9: TI_B busy
Bit10: TS data block readout interrupt N reaches 0x8000;
Bit 31-16 (R): BUSY source monitoring. [0x28, BIT(15:0)]

- Address offset: 0x0002C: Clock source selection:

  Bit 1-0 (R/W): software bit switch to control the clock source. Reset default 00; [0x08, BIT(13:12)]
  Bit[1:0] = 00: oscillator clock;
  Bit[1:0] = 01: HFBR#5 clock input; (not valid for current setup)
  Bit[1:0] = 10: HFBR#1 clock input;
  Bit[1:0] = 11: Front panel 34-pin connector clock input.
  00, 11: oscillator clock on TS;
  01, 10: SMA external clock input on TS;

- Address offset: 0x00030: Trigger_1 pre-scale:

  Bit 15-0 (R/W): pre-scale factor: Rate = Rate_0 / (Bit(15:0)+1). [0x0C, BIT(31:28)]

- Address offset: 0x00034: Trigger block inhibit:

  Bit 7-0 (R/W): TS trigger inhibit threshold (in the unit of event blocks); Reset default 0x01; [0x08, BIT(31:24)]
  Bit 23-8 (R): Number of blocks in the DAQ ready to be readout. [0x14, BIT(31:24)]
  (on TI, Bit 23-16 (R): Number of events before the a block is formed. [0x14, BIT(23:16)])
  Bit 31-24 (R): Number of missing block acknowledge;

- Address offset: 0x00038: Trigger rules:

  Bit 7-0 (R/W): No more than 1 Trigger in (Bit(6:0)*(16/500 ns)); Bit7 determines 16ns or 500ns step. Reset default 0x03; [R:0x58, BIT(23:16)] [W:0x810, BIT(7:0)]
  Bit 15-8 (R/W): no more than 2 trigger in (Bit(14:8)*(16/500ns)); Bit15 determines 16ns or 500ns step. Reset default 0x03; [W:0x810, BIT(15:8)]
  Bit 23-16 (R/W): no more than 3 triggers in (Bit(22:16)*(16/500 ns)); Bit23 determines 16ns or 500ns step. Reset default 0x03; [R:0x58, BIT(31:24)] [W:0x810, BIT(23:16)]
  Bit 31-24 (R/W): no more than 4 triggers in (Bit(30:24)*(16/500 ns)). Bit31 determines 16ns or 500ns step. Reset default 0x03; [W:0x810, BIT(31:24)]

- Address offset: 0x0003C: Trigger coincidence window:

  Bit 7-0 (R/W): Trigger input coincidence window; Reset default 0x01;
  Bit15-8 (R/W): Trigger inhibit window (extra to bit(7:0)). Reset default 0x00;
  These two parameters are used to determine the event resolution

- Address offset: 0x00040: GTP trigger input enable:

  Bit 31-0 (R/W): 32-bit GTP input enables. Reset default 0x00000000;

- Address offset: 0x00044: Front panel external trigger input enable:

  Bit 31-0 (R/W): Front panel 32-bit external trigger input enable. Reset default 0x00000000;

- Address offset: 0x00048: Front panel generic trigger input enable:

  Bit 15-0 (R/W): Front panel generic trigger input enable (34-pin TI). Reset default 0x00000000; [0x08, BIT(21:16)]

- Address offset: 0x0004C: Blocks for VME interrupt:

  Bit 15-0 (R/W): 4-bit output to the front panel generic output connector; Reset default 0x0000; [0x2C, BIT(3:0)]
  Bit 23-16 (R): Number of data blocks ready for VME interrupt. [0x2C, BIT(31:24)]
  Bit 31-24 (R): on TI: Number of events of a partial block (or, before the block is formed)
  On TS: bit(15:8) of the number of data blocks ready for VME interrupt.

- Address offset: 0x00050: Sync delay setting (to compensate for the fiber length):

  Bit 7-0 (R): on TI: SYNC phase of HFBR#1 input; [0x1C, BIT(7:0)]
  Bit 15-8 (R/W): HFBR#1 SYNC input delay; Reset default 0x00; [0x1C, BIT(15:8)]
  Bit 23-16 (R/W): TM (internal loopback) SYNC delay; Reset default 0x00; [0x1C, BIT(23:16)]
  Bit 23-16 (R): on TI: SYNC phase of HFBR#5 input; [0x1C, BIT(23:16)]
  Bit(31:24 (R/W): HFBR#5 SYNC input delay. Reset default 0x00; [0x1C, BIT(31:24)]

- Address offset: 0x00054: GTP input pre-scale: Reset default 0x00000000;

  Bit 3-0 (R/W): GTP input #1 pre-scale;
  Bit 7-4 (R/W): GTP input #2 pre-scale;
  Bit 11-8 (R/W): GTP input #3 pre-scale;
  Bit 15-12 (R/W): GTP input #4 pre-scale;
  Bit 19-16 (R/W): GTP input #5 pre-scale;
  Bit 23-20 (R/W): GTP input #6 pre-scale;
  Bit 27-24 (R/W): GTP input #7 pre-scale;
  Bit 31-28 (R/W): GTP input #8 pre-scale.

- Address offset: 0x00058: GTP input pre-scale: Reset default 0x00000000;

  Bit 3-0 (R/W): GTP input #9 pre-scale;
  Bit 7-4 (R/W): GTP input #10 pre-scale;
  Bit 11-8 (R/W): GTP input #11 pre-scale;
  Bit 15-12 (R/W): GTP input #12 pre-scale;
  Bit 19-16 (R/W): GTP input #13 pre-scale;
  Bit 23-20 (R/W): GTP input #14 pre-scale;
  Bit 27-24 (R/W): GTP input #15 pre-scale;
  Bit 31-28 (R/W): GTP input #16 pre-scale.

- Address offset: 0x0005C: GTP input pre-scale: Reset default 0x00000000;

  Bit 3-0 (R/W): GTP input #17 pre-scale;
  Bit 7-4 (R/W): GTP input #18 pre-scale;
  Bit 11-8 (R/W): GTP input #19 pre-scale;
  Bit 15-12 (R/W): GTP input #20 pre-scale;

Bit 19-16 (R/W): GTP input #21 pre-scale;
Bit 23-20 (R/W): GTP input #22 pre-scale;
Bit 27-24 (R/W): GTP input #23 pre-scale;
Bit 31-28 (R/W): GTP input #24 pre-scale.

- Address offset: 0x00060: GTP input pre-scale: Reset default 0x00000000;

  Bit 3-0 (R/W): GTP input #25 pre-scale;
  Bit 7-4 (R/W): GTP input #26 pre-scale;
  Bit 11-8 (R/W): GTP input #27 pre-scale;
  Bit 15-12 (R/W): GTP input #28 pre-scale;
  Bit 19-16 (R/W): GTP input #29 pre-scale;
  Bit 23-20 (R/W): GTP input #30 pre-scale;
  Bit 27-24 (R/W): GTP input #31 pre-scale;
  Bit 31-28 (R/W): GTP input #32 pre-scale.

- Address offset: 0x00064: Front Panel external trigger input pre-scale: Reset default 0x00000000

  Bit 3-0 (R/W): FP external trigger input #1, B#1 pre-scale;
  Bit 7-4 (R/W): FP external trigger input #2, B#2 pre-scale;
  Bit 11-8 (R/W): FP external trigger input #3, B#3 pre-scale;
  Bit 15-12 (R/W): FP external trigger input #4, B#4 pre-scale;
  Bit 19-16 (R/W): FP external trigger input #5, B#5 pre-scale;
  Bit 23-20 (R/W): FP external trigger input #6, B#6 pre-scale;
  Bit 27-24 (R/W): FP external trigger input #7, B#7 pre-scale;
  Bit 31-28 (R/W): FP external trigger input #8, B#8 pre-scale.

- Address offset: 0x00068: Front Panel external trigger input pre-scale: Reset default 0x00000000

  Bit 3-0 (R/W): FP external trigger input #9, A#1 pre-scale;
  Bit 7-4 (R/W): FP external trigger input #10, A#2 pre-scale;
  Bit 11-8 (R/W): FP external trigger input #11, A#3 pre-scale;
  Bit 15-12 (R/W): FP external trigger input #12, A#4 pre-scale;
  Bit 19-16 (R/W): FP external trigger input #13, A#5 pre-scale;
  Bit 23-20 (R/W): FP external trigger input #14, A#6 pre-scale;
  Bit 27-24 (R/W): FP external trigger input #15, A#7 pre-scale;
  Bit 31-28 (R/W): FP external trigger input #16, A#8 pre-scale.

- Address offset: 0x0006C: Front Panel external trigger input pre-scale: Reset default 0x00000000

  Bit 3-0 (R/W): FP external trigger input #17, D#1 pre-scale;
  Bit 7-4 (R/W): FP external trigger input #18, D#2 pre-scale;
  Bit 11-8 (R/W): FP external trigger input #19, D#3 pre-scale;
  Bit 15-12 (R/W): FP external trigger input #20, D#4 pre-scale;
  Bit 19-16 (R/W): FP external trigger input #21, D#5 pre-scale;
  Bit 23-20 (R/W): FP external trigger input #22, D#6 pre-scale;
  Bit 27-24 (R/W): FP external trigger input #23, D#7 pre-scale;

Bit 31-28 (R/W): FP external trigger input #24, D#8 pre-scale.

- Address offset: 0x00070: Front Panel external trigger input pre-scale: Reset default 0x00000000

  Bit 3-0 (R/W): FP external trigger input #25, C#1 pre-scale;
  Bit 7-4 (R/W): FP external trigger input #26, C#2 pre-scale;
  Bit 11-8 (R/W): FP external trigger input #27, C#3 pre-scale;
  Bit 15-12 (R/W): FP external trigger input #28, C#4 pre-scale;
  Bit 19-16 (R/W): FP external trigger input #29, C#5 pre-scale;
  Bit 23-20 (R/W): FP external trigger input #30, C#6 pre-scale;
  Bit 27-24 (R/W): FP external trigger input #31, C#7 pre-scale;
  Bit 31-28 (R/W): FP external trigger input #32, C#8 pre-scale.

- Address offset: 0x00074: Front Panel generic trigger input pre-scale: Reset default 0x00000000

  Bit 3-0 (R/W): FP Generic trigger input #1 and #9 pre-scale; (#1 is not trigger input, it is INHIBIT)
  Bit 7-4 (R/W): FP Generic trigger input #2 and #10 pre-scale;
  Bit 11-8 (R/W): FP Generic trigger input #3 and #11 pre-scale;
  Bit 15-12 (R/W): FP Generic trigger input #4 and #12 pre-scale;
  Bit 19-16 (R/W): FP Generic trigger input #5 and #13 pre-scale;
  Bit 23-20 (R/W): FP Generic trigger input #6 and #14 pre-scale;
  Bit 27-24 (R/W): FP Generic trigger input #7 and #15 pre-scale;
  Bit 31-28 (R/W): FP Generic trigger input #8 and #16 pre-scale.

- Address offset: 0x00078: VME Sync Load[0x900, BIT(7:0)]

  Bit 7-4 == Bit 3-0 (R/W): 4-bit sync code; Decoding of the Sync command (bit[7:0]):
  0x11: VME clock DCM reset, and full reset;
  0x22: CLK250 resync (AD9510, DCM resync and MGT reset);
  0x33: AD9510 re-sync (slower clock phase adjustment), part of 0x22 function;
  0x44: Reset the MGT status_B registers;
  0x55: Trigger link enable (serial link started), FIFO read counter reset;
  0x77: Trigger link disable, trigger FIFO write counter reset;
  0xDD: (SyncReset), FPGA logic and counter reset, this reset all goes to SD, CTP/GTP;
  0x66, 0x88, 0x99, 0xaa, 0xbb, 0xcc, 0xee: to be assigned;
  0x00, 0xff: reserved, not to be assigned

- Address offset: 0x0007C: VME Sync Delay. The latency before being serialized.

  Bit 6-0 (R/W): latency, in 4ns steps. Reset default 000,0111 [0x904, BIT(6:0)]

- Address offset: 0x00080: Reset pulse width: Reset default 00,0111

  Bit 7-0 (R/W): Reset (to SW#A, SW#B and on-board) pulse width. Pulse width is (Bit(6:0)*(4/32 ns)), Bit(7) determines the steps (4ns or 32ns); [0x904, BIT(13:8), bit(13) set to pulse to 1us wide]

- Address offset: 0x00084: VME Trigger Command Register

  Bit 11-0 (R/W): Trigger Command code transmitted in the trigger link; [0x800, BIT(11:0)]

- Address offset: 0x00088 (R/W): VME Random Trigger Command Register: [0x808, BIT(15:0)]

  Bit 2-0: Random trigger_1 rates: 500KHz/($2^{Bit(2:0)}$);
  Bit 3: enable/disable random trigger_1;
  Bit 7-4: same as Bit(3-0) for redundancy check. No match, no trigger_1;
  Bit 10-8: Random trigger_2 rates: 500KHz/($2^{Bit(2:0)}$);
  Bit 11: enable/disable random trigger_2;
  Bit 15-12: same as Bit(11-8) for redundancy check. No match, no trigger_2.

- Address offset: 0x0008C(R/W): VME Trigger Generation: [0x804, BIT(31:0)]

  Bit 15-0: Number of trigger_1s to be generated;
  Bit 31-16: (trigger rate control) Time between triggers. T = (120+30*Bit(30:16)*$1024^{Bit(31)}$) ns. (Assuming that the ClkVme=33MHz or 30ns period).

- Address offset: 0x00090(R/W): VME Trigger_2 Generation: [0x80C, BIT(31:0)]

  Bit 15-0: Number of trigger_2s to be generated;
  Bit 31-16: (trigger rate control) Time between triggers. T = (120+30*Bit(30:16)*$1024^{Bit(31)}$) ns. (Assuming that the ClkVme=33MHz or 30ns period).

- Address offset: 0x00094 (R): Number of Blocks in the DAQ system: [0x14, BIT(15:0)]

  Bit 31-24: Number of events of a partial data block;
  Bit 23-0: Number of full data blocks the TIDS has ever generated;

- Address offset: 0x00098: to be assigned;
-
- Address offset: 0x0009C (R/W): The FPGA running mode;

  Bit 7-0: TS in running mode if set to 0x5A; if other value, not in running mode. Reset default 0x00;
  TI in running mode if set to 0x71. TI starts clock monitoring in 'running' mode.

- Address offset: 0x000A0 (R): Fiber latency measurement result: [0x18]

  Bit 31-23: latency data in 4ns steps
  Bit 22-16: Delay in the IODelay, in 5000/64=78.125ps steps
  Bit 15:0: Delay in the carry chain, two bits per slice, (or two mux per bit)

- Address offset: 0x000A4 (R): Fiber SYNC delay and phase alignment: [0x1C] (kind of repeat of 0x50)

  Bit 31-24: HFBR#5 sync delay;
  Bit 23-16: HFBR#5 IODelay, for phase adjustment;
  Bit 15-8: HFBR#1 Sync delay (in 4ns steps);
  Bit 7-0: HFBR#1 IODelay, for phase adjustment.

- Address offset: 0x000A8 (R): Trigger live timer: [0x20]

  Bit 31-0 (r): board live time counter. The real time is Bit(31:0)*256*30ns.

- Address offset: 0x000AC (R): Trigger busy (trigger dead) timer: [0x24]

Bit 31-0 (r): TID busy (can not accept trigger, or trigger dead) time counter. The real time is Bit(31:0)*256*30ns. This counter and the live time counter make up the total time counter, which is the total time since any one of the trigger sources is enabled.

- Address offset: 0x000B0 (R): MGT STATUS_A: [0x30]

  Bit 7-0: MGT[7:0] reset_done;
  Bit 11-8: MGT PLL lock detected (two MGTs per PLL lock);
  Bit 31-12 : not used yet;}

- Address offset: 0x000B4 (R): MGT STATUS_B registers: [0x34]

  Bit 7-0: Channel bonding sequence detected in MGT[7:0];
  Bit 15-8: received data is not an 8B/10B character, or has disparity error in MGT[7:0];
  Bit 23-16: RX disparity error has occurred in MGT[7:0];
  Bit 31-24: Rx data not in 8B/10B table has occurred in MGT[7:0].

- Address offset: 0x000B8 (R): MGT trigger data buffer length: [0x38]

  Bit 9-0: Global trigger data buffer length (to be minimized to 0 for the longest fiber);
  Bit 11-10: Data generation fifo full (in TRGDAQ module);
  Bit 13-12: Data Readout fifo prog_almost_full (in VME module);
  Bit 15:14: Data Readout fifo full; The order should be: DataReadoutFifoProgFull → DataGenFifoFull → DataReadoutFifoFull
  Bit 25-16: Sub-system trigger data buffer length;
  Bit 27: TI is in running mode if '1';
  Bit 28: HFBR#1 MGT receiver error;
  Bit 29: CLK250 DCM locked;
  Bit 30: Clk125 DCM locked;
  Bit 31: VME CLK (33MHz or 25MHz) DCM locked

- Address offset: 0x000BC (R): TS input trigger counter: [0x3C]

  Bit 31-0: Number of triggers received by TS (before BUSY inhibits).

- Address offset: 0x000C0 (R): valid for TM (or with TS function), not valid for TI: [0x40]

  Bit 7-0: Number of blocks to be readout on HFBR#1;
  Bit 15-8: Number of blocks is still missing on HFBR#1
  Bit 23-16: Number of blocks to be readout on HFBR#2
  Bit 31-24: Number of blocks is still missing on HFBR#2

- Address offset: 0x000C4 (R): valid for TM (or with TS function), not valid for TI: [0x44]

  Bit 7-0: Number of blocks to be readout on HFBR#3;
  Bit 15-8: Number of blocks is still missing on HFBR#3;
  Bit 23-16: Number of blocks to be readout on HFBR#4;
  Bit 31-24: Number of blocks is still missing on HFBR#4;
  For TS, Bit 31-0: External Trigger counter, Number of triggers from External trigger before lookup table.

- Address offset: 0x000C8 (R): valid for TM (or with TS function), not valid for TI: [0x48]

  Bit 7-0: Number of blocks to be readout on HFBR#5;
  Bit 15-8: Number of blocks is still missing on HFBR#5;
  Bit 23-16: Number of blocks to be readout on HFBR#6;
  Bit 31-24: Number of blocks is still missing on HFBR#6;
  For TS, Bit 31-0: FrontPanel Trigger counter, Number of triggers from FP trigger before lookup table.

- Address offset: 0x000CC (R): valid for TM (or with TS function), not valid for TI: [0x4C]

  Bit 7-0: Number of blocks to be readout on HFBR#7;
  Bit 15-8: Number of blocks is still missing on HFBR#7;
  Bit 23-16: Number of blocks to be readout on HFBR#8;
  Bit 31-24: Number of blocks is still missing on HFBR#8;

- Address offset: 0x000D0 (R): valid for TM (or with TS function)

  Bit 4-0: A24 address used for the module (to match with A23-A19); [0x54, BIT(4:0)]
  Bit 9-5: A24 address set by the onboard hardware switch; [0x54, BIT(9:5)]
  Bit 14-10: GA(4:0), VME64x geographic address; [0x54, BIT(14:10)]
  Bit 15: parity of GA(4:0); [0x54, BIT15]
  Bit 27-16: Number of blocks to be readout on TM itself; [0x50, BIT(23:16)]
  Bit 31-28: Number of blocks is still missing on TM itself; [0x50, BIT(31:24)]

- Address offset: 0x000F0 (R): valid for TM (or with TS function)

  Bit 31-0: Number of valid code from Front Panel Async trigger inputs

- Address offset: 0x000F4 (R): valid for TS

  Bit 31-0: Number of valid code from GTP trigger inputs

- Address offset: 0x000F8 (R): valid for TS

  Bit 31-0: Number of valid code from Front Panel sync trigger (External) inputs

- Address offset: 0x000FC (R/W): Generic enable control

  Bit 0: Enable the front panel (external input) signal to latch the trigger input scalars;
  Bit 1: Enable the front panel (same signal as controlled by bit0) to reset the trigger input scalars; These two bits are kind of related to the OneShotVme command, offset 0x100, bit 24 and bit25.

- Address offset: 0x00100 (W): Reset and one-shot registers. The signal will be one ClkVme cycle. If the ClkVme is 25 MHz, the one-shot will be 40ns wide. Positive logic. [0x100]

  Bit 0: not used;
  Bit 1: if '1', RESET signal to reset the VME_to_I2C engine;
  Bit 2: if '1', RESET signal to reset the VME_to_JTAG engine;
  Bit 3: if '1', RESET signal to reset the VME_to_SFM engine;
  Bit 4: if '1', RESET signal to reset the VME registers (TID settings) to their default values;
  Bit 7: if '1', this register will generate a BUSY reset, and Trg_Ack pulse (TS rev2 compatible).

Bit 8: if '1', Reset the CLK250/Clk200 DCM.
Bit 9: if '1', Reset the CLK125 DCM.
Bit 10: if '1', Reset the MGT (MultiGigabit Transceiver,) inside the FPGA.
Bit 11: if '1', Auto alignment of SYNC phase from HFBR#1; auto align P0 sync input for TD.
Bit 12: if '1', TI: Auto alignment of SYNC phase from HFBR#5;
TS: reset the BRAM loading address to 0 (very beginning).
Bit 13: if '1', Auto alignment of fiber latency measurement signals;
Bit 14: if '1', Reset the IODELAY;
Bit 15: if '1', Measure the fiber latency
Bit 16: if '1', this register will generate a 'TAKE_TOKEN'
Bit 17: if '1', the available number of data blocks will decrease by 1,
Bit 24: if '1', all the trigger input scalars are latched (ready for read out);
Bit 25: if '1', all the trigger input scalars are reset. (Bit 24 and Bit 25 can be set simultaneously)

- Address offset: 0x008CX (0x8C0 – 0x8FC) (W): Trigger table loading: (prototype TS / TImaster) [0x8CX]

  Bit 31-0: 32-bit wide table loading.
  Address bits(5-2) are used to load 16 32-bit words;
  6-bit read addressing with 8-bit trigger type (byte wide)

- Address offset: 0x140 (R/W): SubTS#1 Front Panel Async trigger input selection

  Bit 17-12: SubTS#1 trigger signal #13 source selection from FP inputs.
  Bit 11-6: SubTS#1 trigger signal #12 source selection from FP inputs.
  Bit 5-0: SubTS#1 trigger signal #11 source selection from FP inputs.

- Address offset: 0x144 (R/W): SubTS#1 GTP trigger input selection

  Bit 29-24: SubTS#1 trigger signal #5 source selection from GTP inputs.
  Bit 23-18: SubTS#1 trigger signal #4 source selection from GTP inputs.
  Bit 17-12: SubTS#1 trigger signal #3 source selection from GTP inputs.
  Bit 11-6: SubTS#1 trigger signal #2 source selection from GTP inputs.
  Bit 5-0: SubTS#1 trigger signal #1 source selection from GTP inputs.

- Address offset: 0x148 (R/W): SubTS#1 Front Panel External Sync trigger input selection

  Bit 29-24: SubTS#1 trigger signal #10 source selection from EXT inputs.
  Bit 23-18: SubTS#1 trigger signal #9 source selection from EXT inputs.
  Bit 17-12: SubTS#1 trigger signal #8 source selection from EXT inputs.
  Bit 11-6: SubTS#1 trigger signal #7 source selection from EXT inputs.
  Bit 5-0: SubTS#1 trigger signal #6 source selection from EXT inputs.

- Address offset: 0x14C (W): SubTS#1 lookup table loading

  Bit 31-0: SubTS#1 lookup table context. 1024 operations are required for one Block RAM loading.

- Address offset: 0x150 (R): SubTS#1 data readout

  Bit 31-0: SubTS#1 event data.

- Address offset: 0x154 (R): SubTS#1 Data Block available register

  Bit 31-24: SubTS#1 number of event before forming an data block.
  Bit 23-8: SubTS#1 number of blocks of data generated.
  Bit 7-0: SubTS#1 number of data blocks to be read out.

- Address offset: 0x158 (R/W): SubTS#1 Busy setting

  Bit 31-24: SubTS#1: buffer threshold for number of data blocks on TS.
  Bit 17: SubTS#1: '1' enable the number of data block threshold.
  Bit 16: SubTS#1: '1' enable the data fifo Programmable_almost_full backpressure.
  Bit 15-0: SubTS#1: TD_busy input 15-0 enables for SubTS#1 (or, is this TD belong to SubTS#1)

- Address offset: 0x15C (R): SubTS#1 Busy time

  Bit 15-0: SubTS#1: Busy time. Busy percentage: Bit(15-0)/0xf000; This number is updated ~every second

- Address offset: 0x00180 (R): FP input trigger scalar for #1 (INHIBIT, not valid):

  Bit 31-0: 32-bit scalar, number of input counter

- Address offset: 0x00184 (R): FP input trigger scalar for #2:

  Bit 31-0: 32-bit scalar, number of FP input#2 counter

- Address offset: 0x00188 (R): FP input trigger scalar for #3:

  Bit 31-0: 32-bit scalar, number of FP input#3 counter

- Address offset: 0x0018C (R): FP input trigger scalar for #4:

  Bit 31-0: 32-bit scalar, number of FP input#4 counter

- Address offset: 0x00190 (R): GTP input trigger scalar for #1 (clock, not valid):

  Bit 31-0: 32-bit scalar, number of GTP input#1 counter

- Address offset: 0x00194 (R): GTP input trigger scalar for #2:

  Bit 31-0: 32-bit scalar, number of GTP input#2 counter

- Address offset: 0x00198 (R): GTP input trigger scalar for #3:

  Bit 31-0: 32-bit scalar, number of GTP input#3 counter

- Address offset: 0x0019C (R): GTP input trigger scalar for #4:

  Bit 31-0: 32-bit scalar, number of GTP input#4 counter

- Address offset: 0x001A0 (R): GTP input trigger scalar for #5:

  Bit 31-0: 32-bit scalar, number of GTP input#5 counter

- Address offset: 0x001A4 (R): GTP input trigger scalar for #6:

  Bit 31-0: 32-bit scalar, number of GTP input#6 counter

- Address offset: 0x001A8 (R): GTP input trigger scalar for #7:

Bit 31-0: 32-bit scalar, number of GTP input#7 counter

- Address offset: 0x001AC (R): GTP input trigger scalar for #8:

  Bit 31-0: 32-bit scalar, number of GTP input#8 counter

- Address offset: 0x001B0 (R): External input trigger scalar for #1 (B1):

  Bit 31-0: 32-bit scalar, number of External trigger input#1 counter

- Address offset: 0x001B4 (R): External input trigger scalar for #2 (B2):

  Bit 31-0: 32-bit scalar, number of External trigger input#2 counter

- Address offset: 0x001B8 (R): External input trigger scalar for #3 (B3):

  Bit 31-0: 32-bit scalar, number of External trigger input#3 counter

- Address offset: 0x001BC (R): External input trigger scalar for #4 (B4):

  Bit 31-0: 32-bit scalar, number of External trigger input#4 counter

- Address offset: 0x001C0 (R): External input trigger scalar for #5 (B5):

  Bit 31-0: 32-bit scalar, number of External trigger input#5 counter

- Address offset: 0x001C4 (R): External input trigger scalar for #6 (B6):

  Bit 31-0: 32-bit scalar, number of External trigger input#6 counter

- Address offset: 0x001C8 (R): External input trigger scalar for #7 (B7):

  Bit 31-0: 32-bit scalar, number of External trigger input#7 counter

- Address offset: 0x001CC (R): External input trigger scalar for #8 (B8):

  Bit 31-0: 32-bit scalar, number of External trigger input#8 counter

- Address offset: 0x340 (R/W): SubTS#2 Front Panel Async trigger input selection

  Bit 17-12: SubTS#2 trigger signal #13 source selection from FP inputs.
  Bit 11-6: SubTS#2 trigger signal #12 source selection from FP inputs.
  Bit 5-0: SubTS#2 trigger signal #11 source selection from FP inputs.

- Address offset: 0x344 (R/W): SubTS#2 GTP trigger input selection

  Bit 29-24: SubTS#2 trigger signal #5 source selection from GTP inputs.
  Bit 23-18: SubTS#2 trigger signal #4 source selection from GTP inputs.
  Bit 17-12: SubTS#2 trigger signal #3 source selection from GTP inputs.
  Bit 11-6: SubTS#2 trigger signal #2 source selection from GTP inputs.
  Bit 5-0: SubTS#2 trigger signal #1 source selection from GTP inputs.

- Address offset: 0x348 (R/W): SubTS#2 Front Panel External Sync trigger input selection

  Bit 29-24: SubTS#2 trigger signal #10 source selection from EXT inputs.
  Bit 23-18: SubTS#2 trigger signal #9 source selection from EXT inputs.

Bit 17-12: SubTS#2 trigger signal #8 source selection from EXT inputs.
Bit 11-6: SubTS#2 trigger signal #7 source selection from EXT inputs.
Bit 5-0: SubTS#2 trigger signal #6 source selection from EXT inputs.

- Address offset: 0x34C (W): SubTS#2 lookup table loading

  Bit 31-0: SubTS#2 lookup table context. 1024 operations are required for one Block RAM loading.

- Address offset: 0x350 (R): SubTS#2 data readout

  Bit 31-0: SubTS#2 event data.

- Address offset: 0x354 (R): SubTS#2 Data Block available register

  Bit 31-24: SubTS#2 number of event before forming an data block.
  Bit 23-8: SubTS#2 number of blocks of data generated.
  Bit 7-0: SubTS#2 number of data blocks to be read out.

- Address offset: 0x358 (R/W): SubTS#2 Busy setting

  Bit 31-24: SubTS#2: buffer threshold for number of data blocks on TS.
  Bit 17: SubTS#2: '1' enable the number of data block threshold.
  Bit 16: SubTS#2: '1' enable the data fifo Programmable_almost_full backpressure.
  Bit 15-0: SubTS#2: TD_busy input 15-0 enables for SubTS#2 (or, is this TD belong to SubTS#2)

- Address offset: 0x35C (R): SubTS#2 Busy time

  Bit 15-0: SubTS#2: Busy time. Busy percentage: Bit(15-0)/0xf000; This number is updated ~every second

- Address offset: 0x00380 (R): FP input trigger scalar for #5:

  Bit 31-0: 32-bit scalar, number of FP input#5 counter

- Address offset: 0x00384 (R): FP input trigger scalar for #6:

  Bit 31-0: 32-bit scalar, number of FP input#6 counter

- Address offset: 0x00388 (R): FP input trigger scalar for #7:

  Bit 31-0: 32-bit scalar, number of FP input#7 counter

- Address offset: 0x0038C (R): FP input trigger scalar for #8:

  Bit 31-0: 32-bit scalar, number of FP input#8 counter

- Address offset: 0x00390 (R): GTP input trigger scalar for #9:

  Bit 31-0: 32-bit scalar, number of GTP input#9 counter

- Address offset: 0x00394 (R): GTP input trigger scalar for #10:

  Bit 31-0: 32-bit scalar, number of GTP input#10 counter

- Address offset: 0x00398 (R): GTP input trigger scalar for #11:

  Bit 31-0: 32-bit scalar, number of GTP input#11 counter

- Address offset: 0x0039C (R): GTP input trigger scalar for #12:

  Bit 31-0: 32-bit scalar, number of GTP input#12 counter
- Address offset: 0x003A0 (R): GTP input trigger scalar for #13:

  Bit 31-0: 32-bit scalar, number of GTP input#3 counter
- Address offset: 0x003A4 (R): GTP input trigger scalar for #14:

  Bit 31-0: 32-bit scalar, number of GTP input#14 counter
- Address offset: 0x003A8 (R): GTP input trigger scalar for #15:

  Bit 31-0: 32-bit scalar, number of GTP input#15 counter
- Address offset: 0x003AC (R): GTP input trigger scalar for #16:

  Bit 31-0: 32-bit scalar, number of GTP input#16 counter
- Address offset: 0x003B0 (R): External input trigger scalar for #9 (A1):

  Bit 31-0: 32-bit scalar, number of External trigger input#9 counter
- Address offset: 0x003B4 (R): External input trigger scalar for #10 (A2):

  Bit 31-0: 32-bit scalar, number of External trigger input#10 counter
- Address offset: 0x003B8 (R): External input trigger scalar for #11 (A3):

  Bit 31-0: 32-bit scalar, number of External trigger input#11 counter
- Address offset: 0x003BC (R): External input trigger scalar for #12 (A4):

  Bit 31-0: 32-bit scalar, number of External trigger input#12 counter
- Address offset: 0x003C0 (R): External input trigger scalar for #13 (A5):

  Bit 31-0: 32-bit scalar, number of External trigger input#13 counter
- Address offset: 0x003C4 (R): External input trigger scalar for #14 (A6):

  Bit 31-0: 32-bit scalar, number of External trigger input#14 counter
- Address offset: 0x003C8 (R): External input trigger scalar for #15 (A7):

  Bit 31-0: 32-bit scalar, number of External trigger input#15 counter
- Address offset: 0x003CC (R): External input trigger scalar for #16 (A8):

  Bit 31-0: 32-bit scalar, number of External trigger input#16 counter

- Address offset: 0x540 (R/W): SubTS#3 Front Panel Async trigger input selection

  Bit 17-12: SubTS#3 trigger signal #13 source selection from FP inputs.
  Bit 11-6: SubTS#3 trigger signal #12 source selection from FP inputs.
  Bit 5-0: SubTS#3 trigger signal #11 source selection from FP inputs.

- Address offset: 0x544 (R/W): SubTS#3 GTP trigger input selection

  Bit 29-24: SubTS#3 trigger signal #5 source selection from GTP inputs.
  Bit 23-18: SubTS#3 trigger signal #4 source selection from GTP inputs.
  Bit 17-12: SubTS#3 trigger signal #3 source selection from GTP inputs.
  Bit 11-6: SubTS#3 trigger signal #2 source selection from GTP inputs.
  Bit 5-0: SubTS#3 trigger signal #1 source selection from GTP inputs.

- Address offset: 0x548 (R/W): SubTS#3 Front Panel External Sync trigger input selection

  Bit 29-24: SubTS#3 trigger signal #10 source selection from EXT inputs.
  Bit 23-18: SubTS#3 trigger signal #9 source selection from EXT inputs.
  Bit 17-12: SubTS#3 trigger signal #8 source selection from EXT inputs.
  Bit 11-6: SubTS#3 trigger signal #7 source selection from EXT inputs.
  Bit 5-0: SubTS#3 trigger signal #6 source selection from EXT inputs.

- Address offset: 0x54C (W): SubTS#3 lookup table loading

  Bit 31-0: SubTS#3 lookup table context. 1024 operations are required for one Block RAM loading.

- Address offset: 0x550 (R): SubTS#3 data readout

  Bit 31-0: SubTS#3 event data.

- Address offset: 0x554 (R): SubTS#3 Data Block available register

  Bit 31-24: SubTS#3 number of event before forming an data block.
  Bit 23-8: SubTS#3 number of blocks of data generated.
  Bit 7-0: SubTS#3 number of data blocks to be read out.

- Address offset: 0x558 (R/W): SubTS#3 Busy setting

  Bit 31-24: SubTS#3: buffer threshold for number of data blocks on TS.
  Bit 17: SubTS#3: ‘1’ enable the number of data block threshold.
  Bit 16: SubTS#3: ‘1’ enable the data fifo Programmable_almost_full backpressure.
  Bit 15-0: SubTS#3: TD_busy input 15-0 enables for SubTS#3 (or, is this TD belong to SubTS#3)

- Address offset: 0x55C (R): SubTS#3 Busy time

  Bit 15-0: SubTS#3: Busy time. Busy percentage: Bit(15-0)/0xf000; This number is updated ~every second

- Address offset: 0x00580 (R): FP input trigger scalar for #9:

  Bit 31-0: 32-bit scalar, number of FP input#9 counter

- Address offset: 0x00584 (R): FP input trigger scalar for #10:

  Bit 31-0: 32-bit scalar, number of FP input#10 counter

- Address offset: 0x00588 (R): FP input trigger scalar for #11:

  Bit 31-0: 32-bit scalar, number of FP input#11 counter

- Address offset: 0x0058C (R): FP input trigger scalar for #12:

Bit 31-0: 32-bit scalar, number of FP input#12 counter

- Address offset: 0x00590 (R): GTP input trigger scalar for #17:

  Bit 31-0: 32-bit scalar, number of GTP input#17 counter

- Address offset: 0x00594 (R): GTP input trigger scalar for #18:

  Bit 31-0: 32-bit scalar, number of GTP input#18 counter

- Address offset: 0x00598 (R): GTP input trigger scalar for #19:

  Bit 31-0: 32-bit scalar, number of GTP input#19 counter

- Address offset: 0x0059C (R): GTP input trigger scalar for #20:

  Bit 31-0: 32-bit scalar, number of GTP input#20 counter

- Address offset: 0x005A0 (R): GTP input trigger scalar for #21:

  Bit 31-0: 32-bit scalar, number of GTP input#21 counter

- Address offset: 0x005A4 (R): GTP input trigger scalar for #22:

  Bit 31-0: 32-bit scalar, number of GTP input#22 counter

- Address offset: 0x005A8 (R): GTP input trigger scalar for #23:

  Bit 31-0: 32-bit scalar, number of GTP input#23 counter

- Address offset: 0x005AC (R): GTP input trigger scalar for #24:

  Bit 31-0: 32-bit scalar, number of GTP input#24 counter

- Address offset: 0x005B0 (R): External input trigger scalar for #17 (D1):

  Bit 31-0: 32-bit scalar, number of External trigger input#17 counter

- Address offset: 0x005B4 (R): External input trigger scalar for #18 (D2):

  Bit 31-0: 32-bit scalar, number of External trigger input#18 counter

- Address offset: 0x005B8 (R): External input trigger scalar for #19 (D3):

  Bit 31-0: 32-bit scalar, number of External trigger input#19 counter

- Address offset: 0x005BC (R): External input trigger scalar for #20 (D4):

  Bit 31-0: 32-bit scalar, number of External trigger input#20 counter

- Address offset: 0x005C0 (R): External input trigger scalar for #21 (D5):

  Bit 31-0: 32-bit scalar, number of External trigger input#21 counter

- Address offset: 0x005C4 (R): External input trigger scalar for #22 (D6):

  Bit 31-0: 32-bit scalar, number of External trigger input#22 counter

- Address offset: 0x005C8 (R): External input trigger scalar for #23 (D7):

Bit 31-0: 32-bit scalar, number of External trigger input#23 counter

- Address offset: 0x005CC (R): External input trigger scalar for #24 (D8):

  Bit 31-0: 32-bit scalar, number of External trigger input#24 counter

- Address offset: 0x740 (R/W): SubTS#4 Front Panel Async trigger input selection

  Bit 17-12: SubTS#4 trigger signal #13 source selection from FP inputs.
  Bit 11-6: SubTS#4 trigger signal #12 source selection from FP inputs.
  Bit 5-0: SubTS#4 trigger signal #11 source selection from FP inputs.

- Address offset: 0x744 (R/W): SubTS#4 GTP trigger input selection

  Bit 29-24: SubTS#4 trigger signal #5 source selection from GTP inputs.
  Bit 23-18: SubTS#4 trigger signal #4 source selection from GTP inputs.
  Bit 17-12: SubTS#4 trigger signal #3 source selection from GTP inputs.
  Bit 11-6: SubTS#4 trigger signal #2 source selection from GTP inputs.
  Bit 5-0: SubTS#4 trigger signal #1 source selection from GTP inputs.

- Address offset: 0x748 (R/W): SubTS#4 Front Panel External Sync trigger input selection

  Bit 29-24: SubTS#4 trigger signal #10 source selection from EXT inputs.
  Bit 23-18: SubTS#4 trigger signal #9 source selection from EXT inputs.
  Bit 17-12: SubTS#4 trigger signal #8 source selection from EXT inputs.
  Bit 11-6: SubTS#4 trigger signal #7 source selection from EXT inputs.
  Bit 5-0: SubTS#4 trigger signal #6 source selection from EXT inputs.

- Address offset: 0x74C (W): SubTS#4 lookup table loading

  Bit 31-0: SubTS#4 lookup table context. 1024 operations are required for one Block RAM loading.

- Address offset: 0x750 (R): SubTS#4 data readout

  Bit 31-0: SubTS#4 event data.

- Address offset: 0x754 (R): SubTS#4 Data Block available register

  Bit 31-24: SubTS#4 number of event before forming an data block.
  Bit 23-8: SubTS#4 number of blocks of data generated.
  Bit 7-0: SubTS#4 number of data blocks to be read out.

- Address offset: 0x758 (R/W): SubTS#4 Busy setting

  Bit 31-24: SubTS#4: buffer threshold for number of data blocks on TS.
  Bit 17: SubTS#4: ‘1’ enable the number of data block threshold.
  Bit 16: SubTS#4: ‘1’ enable the data fifo Programmable_almost_full backpressure.
  Bit 15-0: SubTS#4: TD_busy input 15-0 enables for SubTS#4 (or, is this TD belong to SubTS#4)

- Address offset: 0x75C (R): SubTS#4 Busy time

  Bit 15-0: SubTS#4: Busy time. Busy percentage: Bit(15-0)/0xf000; This number is updated ~every second

- Address offset: 0x00780 (R): FP input trigger scalar for #13:

  Bit 31-0: 32-bit scalar, number of FP input#13 counter
- Address offset: 0x00784 (R): FP input trigger scalar for #14:

  Bit 31-0: 32-bit scalar, number of FP input#14 counter
- Address offset: 0x00788 (R): FP input trigger scalar for #15:

  Bit 31-0: 32-bit scalar, number of FP input#15 counter
- Address offset: 0x0078C (R): FP input trigger scalar for #16:

  Bit 31-0: 32-bit scalar, number of FP input#16 counter
- Address offset: 0x00790 (R): GTP input trigger scalar for #25:

  Bit 31-0: 32-bit scalar, number of GTP input#25 counter
- Address offset: 0x00794 (R): GTP input trigger scalar for #26:

  Bit 31-0: 32-bit scalar, number of GTP input#26 counter
- Address offset: 0x00798 (R): GTP input trigger scalar for #27:

  Bit 31-0: 32-bit scalar, number of GTP input#27 counter
- Address offset: 0x0079C (R): GTP input trigger scalar for #28:

  Bit 31-0: 32-bit scalar, number of GTP input#28 counter
- Address offset: 0x007A0 (R): GTP input trigger scalar for #29:

  Bit 31-0: 32-bit scalar, number of GTP input#29 counter
- Address offset: 0x007A4 (R): GTP input trigger scalar for #30:

  Bit 31-0: 32-bit scalar, number of GTP input#30 counter
- Address offset: 0x007A8 (R): GTP input trigger scalar for #31:

  Bit 31-0: 32-bit scalar, number of GTP input#31 counter
- Address offset: 0x007AC (R): GTP input trigger scalar for #32:

  Bit 31-0: 32-bit scalar, number of GTP input#32 counter
- Address offset: 0x007B0 (R): External input trigger scalar for #25 (C1):

  Bit 31-0: 32-bit scalar, number of External trigger input#25 counter
- Address offset: 0x007B4 (R): External input trigger scalar for #26 (C2):

  Bit 31-0: 32-bit scalar, number of External trigger input#26 counter
- Address offset: 0x007B8 (R): External input trigger scalar for #27 (C3):

  Bit 31-0: 32-bit scalar, number of External trigger input#27 counter

- Address offset: 0x007BC (R): External input trigger scalar for #28 (C4):

  Bit 31-0: 32-bit scalar, number of External trigger input#28 counter
- Address offset: 0x007C0 (R): External input trigger scalar for #29 (C5):

  Bit 31-0: 32-bit scalar, number of External trigger input#29 counter
- Address offset: 0x007C4 (R): External input trigger scalar for #30 (C6):

  Bit 31-0: 32-bit scalar, number of External trigger input#30 counter
- Address offset: 0x007C8 (R): External input trigger scalar for #32 (C7):

  Bit 31-0: 32-bit scalar, number of External trigger input#31 counter
- Address offset: 0x007CC (R): External input trigger scalar for #32 (C8):

  Bit 31-0: 32-bit scalar, number of External trigger input#32 counter

- Address offset: 0x01000 (W): Global trigger (Event type) table: first 15x11 table, cell #0 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01004 (W): Global trigger (Event type) table: first 15x11 table, cell #1 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01008 (W): Global trigger (Event type) table: first 15x11 table, cell #2 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x0100C (W): Global trigger (Event type) table: first 15x11 table, cell #3 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01010 (W): Global trigger (Event type) table: first 15x11 table, cell #4 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01014 (W): Global trigger (Event type) table: first 15x11 table, cell #5 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01018 (W): Global trigger (Event type) table: first 15x11 table, cell #6 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x0101C (W): Global trigger (Event type) table: first 15x11 table, cell #7 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01020 (W): Global trigger (Event type) table: first 15x11 table, cell #8 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01024 (W): Global trigger (Event type) table: first 15x11 table, cell #9 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row

- Address offset: 0x01028 (W): Global trigger (Event type) table: first 15x11 table, cell #10 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01040 (W): Global trigger (Event type) table: second 15x11 table, cell #0 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01044 (W): Global trigger (Event type) table: second 15x11 table, cell #1 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01048 (W): Global trigger (Event type) table: second 15x11 table, cell #2 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x0104C (W): Global trigger (Event type) table: second 15x11 table, cell #3 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01050 (W): Global trigger (Event type) table: second 15x11 table, cell #4 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01054 (W): Global trigger (Event type) table: second 15x11 table, cell #5 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01058 (W): Global trigger (Event type) table: second 15x11 table, cell #6 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x0105C (W): Global trigger (Event type) table: second 15x11 table, cell #7 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01060 (W): Global trigger (Event type) table: second 15x11 table, cell #8 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01064 (W): Global trigger (Event type) table: second 15x11 table, cell #9 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01068 (W): Global trigger (Event type) table: second 15x11 table, cell #10 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row

- Address offset: 0x01100 (W): GTP Trigger table first 15x8 table, cell #0 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01104 (W): GTP Trigger table first 15x8 table, cell #1 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01108 (W): GTP Trigger table first 15x8 table, cell #2 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row

- Address offset: 0x0110C (W): GTP Trigger table first 15x8 table, cell #3 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01110 (W): GTP Trigger table first 15x8 table, cell #4 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01114 (W): GTP Trigger table first 15x8 table, cell #5 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01118 (W): GTP Trigger table first 15x8 table, cell #6 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x0111C (W): GTP Trigger table first 15x8 table, cell #7 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01140 (W): GTP Trigger table second 15x8 table, cell #0 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01144 (W): GTP Trigger table second 15x8 table, cell #1 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01148 (W): GTP Trigger table second 15x8 table, cell #2 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x0114C (W): GTP Trigger table second 15x8 table, cell #3 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01150 (W): GTP Trigger table second 15x8 table, cell #4 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01154 (W): GTP Trigger table second 15x8 table, cell #5 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01158 (W): GTP Trigger table second 15x8 table, cell #6 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x0115C (W): GTP Trigger table second 15x8 table, cell #7 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01180 (W): GTP Trigger table first 15x11 table, cell #0 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01184 (W): GTP Trigger table first 15x11 table, cell #1 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row

- Address offset: 0x01188 (W): GTP Trigger table first 15x11 table, cell #2 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x0118C (W): GTP Trigger table first 15x11 table, cell #3 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01190 (W): GTP Trigger table first 15x11 table, cell #4 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01194 (W): GTP Trigger table first 15x11 table, cell #5 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01198 (W): GTP Trigger table first 15x11 table, cell #6 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x0119C (W): GTP Trigger table first 15x11 table, cell #7 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x011A0 (W): GTP Trigger table first 15x11 table, cell #8 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x011A4 (W): GTP Trigger table first 15x11 table, cell #9 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x011A8 (W): GTP Trigger table first 15x11 table, cell #10 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x011C0 (W): GTP Trigger table second 15x11 table, cell #0 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x011C4 (W): GTP Trigger table second 15x11 table, cell #1 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x011C8 (W): GTP Trigger table second 15x11 table, cell #2 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x011CC (W): GTP Trigger table second 15x11 table, cell #3 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x011D0 (W): GTP Trigger table second 15x11 table, cell #4 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x011D4 (W): GTP Trigger table second 15x11 table, cell #5 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row

- Address offset: 0x011D8 (W): GTP Trigger table second 15x11 table, cell #6 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x011DC (W): GTP Trigger table second 15x11 table, cell #7 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x011E0 (W): GTP Trigger table second 15x11 table, cell #8 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x011E4 (W): GTP Trigger table second 15x11 table, cell #9 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x011E8 (W): GTP Trigger table second 15x11 table, cell #10 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01200 (W): External Trigger table first 15x8 table, cell #0 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01204 (W): External Trigger table first 15x8 table, cell #1 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01208 (W): External Trigger table first 15x8 table, cell #2 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x0120C (W): External Trigger table first 15x8 table, cell #3 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01210 (W): External Trigger table first 15x8 table, cell #4 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01214 (W): External Trigger table first 15x8 table, cell #5 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01218 (W): External Trigger table first 15x8 table, cell #6 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x0121C (W): External Trigger table first 15x8 table, cell #7 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01240 (W): External Trigger table second 15x8 table, cell #0 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01244 (W): External Trigger table second 15x8 table, cell #1 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row

- Address offset: 0x01248 (W): External Trigger table second 15x8 table, cell #2 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x0124C (W): External Trigger table second 15x8 table, cell #3 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01250 (W): External Trigger table second 15x8 table, cell #4 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01254 (W): External Trigger table second 15x8 table, cell #5 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01258 (W): External Trigger table second 15x8 table, cell #6 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x0125C (W): External Trigger table second 15x8 table, cell #7 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01280 (W): External Trigger table first 15x11 table, cell #0 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01284 (W): External Trigger table first 15x11 table, cell #1 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01288 (W): External Trigger table first 15x11 table, cell #2 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x0128C (W): External Trigger table first 15x11 table, cell #3 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01290 (W): External Trigger table first 15x11 table, cell #4 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01294 (W): External Trigger table first 15x11 table, cell #5 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01298 (W): External Trigger table first 15x11 table, cell #6 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x0129C (W): External Trigger table first 15x11 table, cell #7 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x012A0 (W): External Trigger table first 15x11 table, cell #8 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row

- Address offset: 0x012A4 (W): External Trigger table first 15x11 table, cell #9 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x012A8 (W): External Trigger table first 15x11 table, cell #10 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x012C0 (W): External Trigger table second 15x11 table, cell #0 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x012C4 (W): External Trigger table second 15x11 table, cell #1 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x012C8 (W): External Trigger table second 15x11 table, cell #2 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x012CC (W): External Trigger table second 15x11 table, cell #3 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x012D0 (W): External Trigger table second 15x11 table, cell #4 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x012D4 (W): External Trigger table second 15x11 table, cell #5 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x012D8 (W): External Trigger table second 15x11 table, cell #6 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x012DC (W): External Trigger table second 15x11 table, cell #7 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x012E0 (W): External Trigger table second 15x11 table, cell #8 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x012E4 (W): External Trigger table second 15x11 table, cell #9 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x012E8 (W): External Trigger table second 15x11 table, cell #10 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row
- Address offset: 0x01300 (W): FP Trigger table cell #0 loading

  Bit 31-0: 32-bit wide table loading; 1024 words in a row
- Address offset: 0x01304 (W): FP Trigger table cell #1 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row

- Address offset: 0x01308 (W): FP Trigger table cell #2 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row

- Address offset: 0x0130C (W): FP Trigger table cell #3 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row

- Address offset: 0x01310 (W): FP Trigger table cell #4 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row

- Address offset: 0x01314 (W): FP Trigger table cell #5 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row

- Address offset: 0x01318 (W): FP Trigger table cell #6 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row

- Address offset: 0x0131C (W): FP Trigger table cell #7 loading

  Bit 31-0: 32-bit wide table loading. 1024 words in a row

6.3 VME to Serial engines:

A24D32 are used for VME to serial engines. The engines include: VME to JTAG engine for the FPGA, VME to JTAG engine for the PROM, VME to I2C for the switch slot#A, VME to I2C engine for the switch slot#B. In the I2C engines design, only the lower one-byte or 2-byte are used. The higher bytes are wasted.

Address offset: 0x1XXXX: JTAG for PROM; Refer to the programming manual for VME to JTAG design for details.

Address offset: 0x2XXXX: JTAG for FPGA;

Address offset: 0x3XXXX: I2C for VXS switch slot#A; Refer to the programming manual for VME to I2C design for details.

Address offset: 0x4XXXX: I2C for VXS switch slot#B;

Address offset: 0x6XXXX: non-volatile Flash memory interface (maybe parallel interface).

6.4 VME data acquisition:

For data acquisition, the A32 block reads are used. The base address is set by a A24 register.

7 Front panel and Backplane pin out tables:

Figure 7 shows the prototype Trigger Supervisor (TS) board. The 30 trigger primitive inputs from GTP are going through the P2 VME connector. There are two external trigger input connectors with two 8-input block each on the front panel, and a generic 2x34-pin IO connector on the front panel with 16 differential inputs, 12 differential outputs and 10 single-ended outputs. The external clock input and output are through pairs of coax cables with SMA connectors. There are six quad LED packs for information display. The SMA connectors are overlapping with the two optional optical transceivers.

Figure 8 shows the TS P2 transition card (TSIO). This is the signal transition from GTP to TS. There is a differential fanout which can be used for TS to send pulsed trigger1 to TD boards, or something else. The LVCMOS to LVPECL translator can be used to interface the TS's LVCMOS signal to TD's differential signals. The direction of the signal can be selected in groups of four.

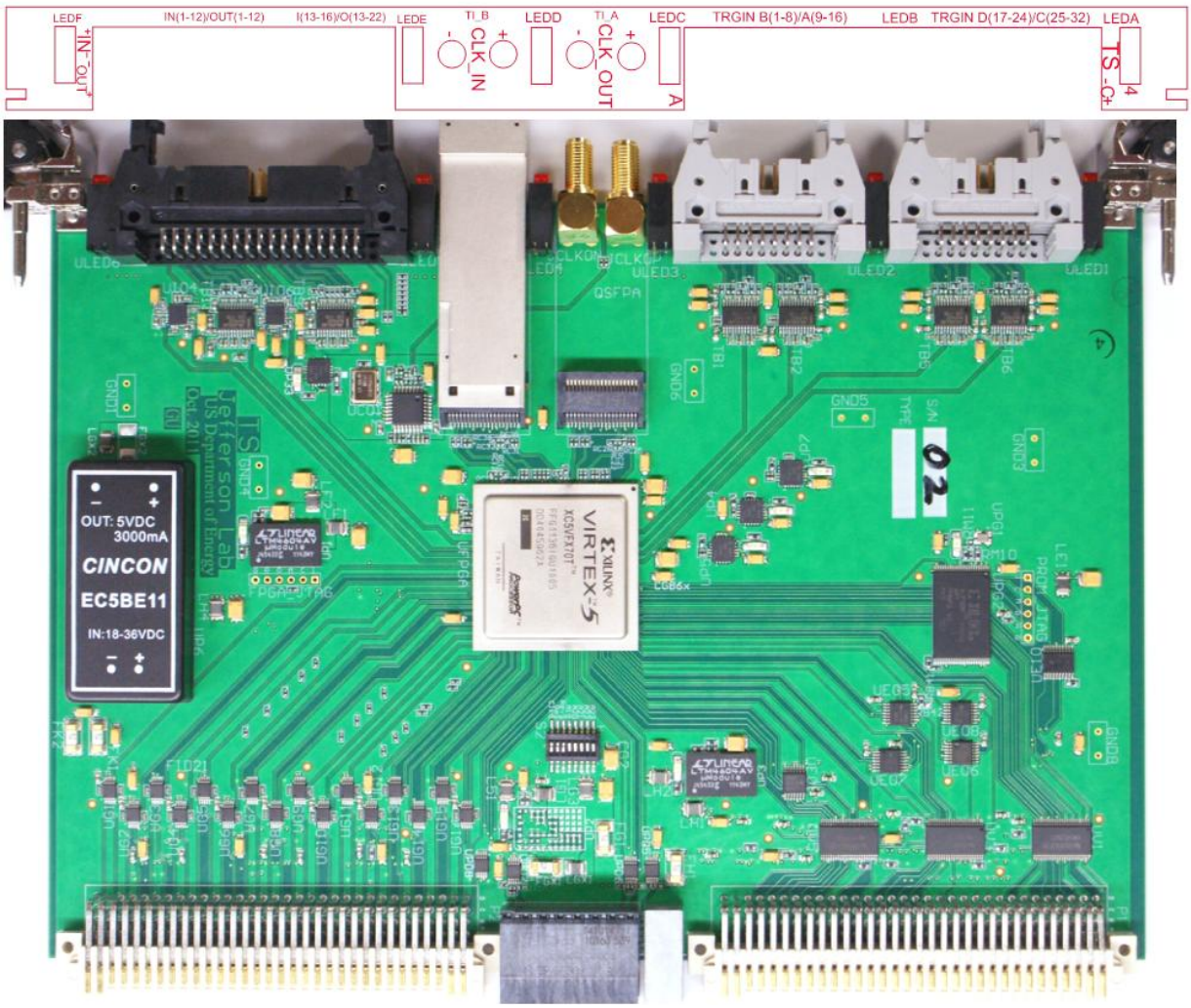

Figure 7 Trigger Supervisor (TS) PCB with its front panel drawing

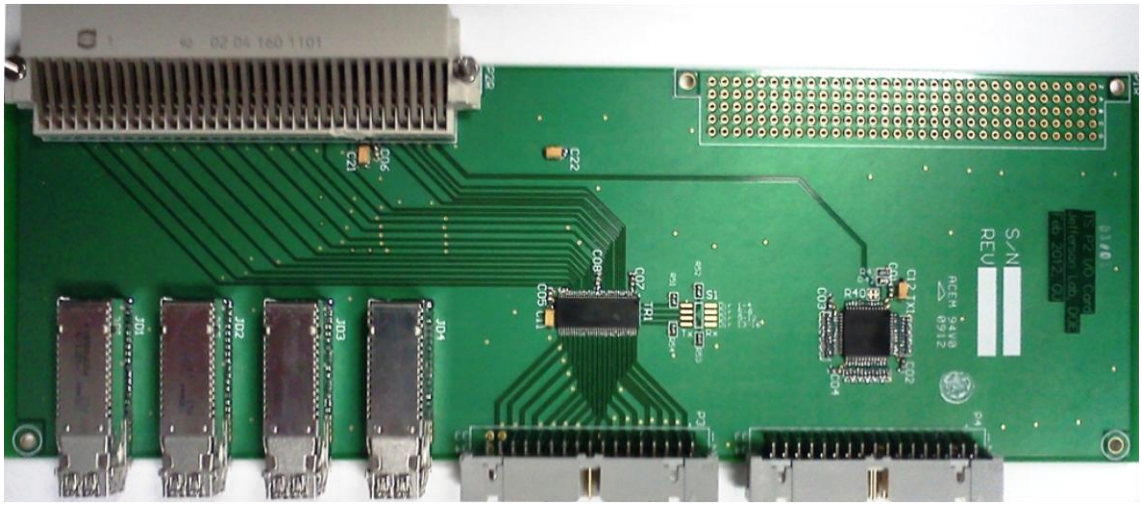

Figure 8 TSIO board, which connects to TS Via VME crate P2 connector

7.1 VXS P0 Pinout Table

Payload slot#18 for TS module			
Pin name	Signal Description	Signal Level	Direction
DP1 (A1+, B1-)	CLOCK_C	LVPECL	PP18 → SWA
DP3 (B2+, C2-)	TP2_LINK	LVDS	PP18 ← SWA
DP4 (E2+, F2-)	SYNC	LVPECL	PP18 → SWA
DP5 (A3+, B3-)	TRIGGER_1	LVPECL	PP18 → SWA
DP7 (B4+, C4-)	TP_LINK	LVDS	PP18 ←→ SWA
DP8 (E4+, F4-)	BUSY	LVDS	PP18 ← SWA
SE1 (G1)	I2C_SCL_SWA	LVTTL (pull up)	PP18 → SWA
SE2 (G3)	I2C_SDA_SWA	LVTTL (pull up)	PP18 ←→ SWA
DP23 (B12+, C12-)	CLOCK_A (250MHz)	LVPECL(DP)	PP18 → SWB
DP24 (E12+, F12-)	CLOCK_B (250MHz)	LVPECL(DP)	PP18 → SWB
DP25 (A13+,B13-)	TOKEN_OUT	LVDS(DP)	PP18 → SWB
DP26 (D13+, E13-)	SYNC	LVPECL(DP)	PP18 → SWB
DP27 (B14+, C14-)	TRIGGER_1	LVPECL(DP)	PP18 → SWB
DP28 (E14+, F14-)	TRIGGER_2	LVPECL(DP)	PP18 → SWB
DP29 (A15+,B15-)	SD_Data_Link	LVDS, 250Mbps	PP18←→SWB
DP30 (D15+,E15-)	BUSY	LVDS	PP18 ← SWB
SE7 (G13)	I2C_SCL_SWB	LVTTL (pull up)	PP18 → SWB
SE8 (G15)	I2C_SDA_SWB	LVTTL (pull up)	PP18 ←→ SWB

7.2 VME P2 Pinout Table

Payload slot#18, for TS module			
Pin name	Signal Description	Signal Level	Direction
A1-, A2+	GTP #32	LVPECL(DP)	IN
A3-, A4+	GTP #30	LVPECL(DP)	IN
A5-, A6+	GTP #28	LVPECL(DP)	IN
A7-, A8+	GTP #26	LVPECL(DP)	IN
A9-, A10+	GTP #24	LVPECL(DP)	IN
A11-, A12+	GTP #22	LVPECL(DP)	IN
A13-, A14+	GTP #20	LVPECL(DP)	IN
A15-, A16+	GTP #18	LVPECL(DP)	IN
A17-, A18+	GTP #16	LVPECL(DP)	IN
A19-, A20+	GTP #14	LVPECL(DP)	IN
A21-, A22+	GTP #12	LVPECL(DP)	IN
A23-, A24+	GTP #10	LVPECL(DP)	IN
A25-, A26+	GTP #8	LVPECL(DP)	IN
A27-, A28+	GTP #6	LVPECL(DP)	IN
A29-, A30+	GTP #4	LVPECL(DP)	IN
A31-, A32+	GTP #2	LVPECL(DP)	IN
C1-, C2+	GTP #31	LVPECL(DP)	IN
C3-, C4+	GTP #29	LVPECL(DP)	IN
C5-, C6+	GTP #27	LVPECL(DP)	IN
C7-, C8+	GTP #25	LVPECL(DP)	IN
C9-, C10+	GTP #23	LVPECL(DP)	IN
C11-, C12+	GTP #21	LVPECL(DP)	IN
C13-, C14+	GTP #19	LVPECL(DP)	IN
C15-, C16+	GTP #17 CLOCK	LVPECL(DP)	IN (Clock)
C17-, C18+	GTP #15	LVPECL(DP)	IN
C19-, C20+	GTP #13	LVPECL(DP)	IN
C21-, C22+	GTP #11	LVPECL(DP)	IN
C23-, C24+	GTP #9	LVPECL(DP)	IN
C25-, C26+	GTP #7	LVPECL(DP)	IN
C27-, C28+	GTP #5	LVPECL(DP)	IN
C29-, C30+	GTP #3	LVPECL(DP)	IN
C31-, C32+	GTP #1 CLOCK	LVPECL(DP)	IN (Clock)
D6, D7, D8, D9, D10	Power output	+3.3V	Out
D21, D22, D23, D24, D25	Power output	-5V	Out
D1+, D2-	Trigger1	LVDS	Out
Z1 (50 Ohm to FPGA)	TD1BP	LVTTL	IN/OUT
Z3 (50 Ohm to FPGA)	TD2BP	LVTTL	IN/OUT
Z5 (50 Ohm to FPGA)	TD3BP	LVTTL	IN/OUT

Z7 (50 Ohm to FPGA)	TD4BP	LVTTL	IN/OUT
Z9 (50 Ohm to FPGA)	TD5BP	LVTTL	IN/OUT
Z11 (50 Ohm to FPGA)	TD6BP	LVTTL	IN/OUT
Z13 (50 Ohm to FPGA)	TD7BP	LVTTL	IN/OUT
Z15 (50 Ohm to FPGA)	TD8BP	LVTTL	IN/OUT
Z17 (50 Ohm to FPGA)	TD9BP	LVTTL	IN/OUT
Z19 (50 Ohm to FPGA)	TD10BP	LVTTL	IN/OUT
Z21 (50 Ohm to FPGA)	TD11BP	LVTTL	IN/OUT
Z23 (50 Ohm to FPGA)	TD12BP	LVTTL	IN/OUT
Z25 (50 Ohm to FPGA)	TD13BP	LVTTL	IN/OUT
Z27 (50 Ohm to FPGA)	TD14BP	LVTTL	IN/OUT
Z29 (50 Ohm to FPGA)	TD15BP	LVTTL	IN/OUT
Z31 (50 Ohm to FPGA)	TD16BP	LVTTL	IN/OUT

7.3 Front panel General IO Pinout Table (lower 34-pin connector)

Payload slot#18 for TS module			
Pin name	Signal Description	Signal Level	Direction
L1-,L2+	Inhibit (BUSY)	Differential (V: -2V ~ 3V)	IN
L3-,L4+	Async FP_Trig#1	Differential (V: -2V ~ 3V)	IN
L5-,L6+	Async FP_Trig#2	Differential (V: -2V ~ 3V)	IN
L7-,L8+	Async FP_Trig#3	Differential (V: -2V ~ 3V)	IN
L9-,L10+	Async FP_Trig#4	Differential (V: -2V ~ 3V)	IN
L11-,L12+	Async FP_Trig#5	Differential (V: -2V ~ 3V)	IN
L13-,L14+	Async FP_Trig#6	Differential (V: -2V ~ 3V)	IN
L15-,L16+	Async FP_Trig#7	Differential (V: -2V ~ 3V)	IN
L17-,L18+	Async FP_Trig#8	Differential (V: -2V ~ 3V)	IN
L19-,L20+	Async FP_Trig#9	Differential (V: -2V ~ 3V)	IN
L21-,L22+	Async FP_Trig#10	Differential (V: -2V ~ 3V)	IN
L23-,L24+	Async FP_Trig#11	Differential (V: -2V ~ 3V)	IN
L25-,L26+	Async FP_Trig#12	Differential (V: -2V ~ 3V)	IN
L27-,L28+	Async FP_Trig#13	Differential (V: -2V ~ 3V)	IN
L29-,L30+	Async FP_Trig#14	Differential (V: -2V ~ 3V)	IN
L31-,L32+	Async FP_Trig#15	Differential (V: -2V ~ 3V)	IN
L33-,L34+	GND		
Payload slot#18 for TS module			
Pin name	Signal Description	Signal Level	Direction
R1+,R2-	Output#1	ECL	OUT

R3+,R4-	Output#2	ECL	OUT
R5+,R6-	Output#3	ECL	OUT
R7+,R8-	Output#4	ECL	OUT
R9+,R10-	Output#5	ECL	OUT
R11+,R12-	Output#6	ECL	OUT
R13+,R14-	Output#7	ECL	OUT
R15+,R16-	Output#8	ECL	OUT
R17+,R18-	Output#9	ECL	OUT
R19+,R20-	Output#10	ECL	OUT
R21+,R22-	Output#11	ECL	OUT
R23+,R24-	Output#12	ECL	OUT
R25	Output#S1	LVCOMS (50Ohm//0.1uf)	OUT
R26	Output#S2	LVCOMS (50Ohm//0.1uf)	OUT
R27	Output#S3	LVCOMS (50Ohm//0.1uf)	OUT
R28	Output#S4	LVCOMS (50Ohm//0.1uf)	OUT
R29	Output#S5	LVCOMS (50Ohm//0.1uf)	OUT
R30	Output#S6	LVCOMS (50Ohm//0.1uf)	OUT
R31	Output#S7	LVCOMS (50Ohm//0.1uf)	OUT
R32	Output#S8	LVCOMS (50Ohm//0.1uf)	OUT
R33	Output#S9	LVCOMS (50Ohm//0.1uf)	OUT
R34	Output#S10	LVCOMS (50Ohm//0.1uf)	OUT

* L: means left side 34-pin connector; R: means right side 34-pin connector.

7.4 Front panel External Trigger Input Table (upper two 2x16 pin connector)

Pin name	Signal Description	Signal Level	Direction
UL1+, UL2-	CLOCK Ext_Trig#17 (D1)	Differential (V: -2V ~ 3V)	IN
UL3+, UL4-	Ext_Trig#18 (D2)	Differential (V: -2V ~ 3V)	IN
UL5+, UL6-	Ext_Trig#19 (D3)	Differential (V: -2V ~ 3V)	IN
UL7+, UL8-	Ext_Trig#20 (D4)	Differential (V: -2V ~ 3V)	IN
UL9+, UL10-	Ext_Trig#21 (D5)	Differential (V: -2V ~ 3V)	IN
UL11+, UL12-	Ext_Trig#22 (D6)	Differential (V: -2V ~ 3V)	IN
UL13+, UL14-	Ext_Trig#23 (D7)	Differential (V: -2V ~ 3V)	IN
UL15+, UL16-	Ext_Trig#24 (D8)	Differential (V: -2V ~ 3V)	IN
UR1+, UR2-	Ext_Trig#25 (C1)	Differential (V: -2V ~ 3V)	IN
UR3+, UR4-	Ext_Trig#26 (C2)	Differential (V: -2V ~ 3V)	IN
UR5+, UR6-	Ext_Trig#27 (C3)	Differential (V: -2V ~ 3V)	IN
UR7+, UR8-	Ext_Trig#28 (C4)	Differential (V: -2V ~ 3V)	IN
UR9+, UR10-	Ext_Trig#29 (C5)	Differential (V: -2V ~ 3V)	IN
UR11+, UR12-	Ext_Trig#30 (C6)	Differential (V: -2V ~ 3V)	IN

UR13+, UR14-	Ext_Trig#31 (C7)	Differential (V: -2V ~ 3V)	IN
UR15+, UR16-	Ext_Trig#32 (C8)	Differential (V: -2V ~ 3V)	IN
LL1+, LL2-	CLOCK Ext_Trig#1 (B1)	Differential (V: -2V ~ 3V)	IN
LL3+, LL4-	Ext_Trig#2 (B2)	Differential (V: -2V ~ 3V)	IN
LL5+, LL6-	Ext_Trig#3 (B3)	Differential (V: -2V ~ 3V)	IN
LL7+, LL8-	Ext_Trig#4 (B4)	Differential (V: -2V ~ 3V)	IN
LL9+, LL10-	Ext_Trig#5 (B5)	Differential (V: -2V ~ 3V)	IN
LL11+, LL12-	Ext_Trig#6 (B6)	Differential (V: -2V ~ 3V)	IN
LL13+, LL14-	Ext_Trig#7 (B7)	Differential (V: -2V ~ 3V)	IN
LL15+, LL16-	Ext_Trig#8 (B8)	Differential (V: -2V ~ 3V)	IN
LR1+, LR2-	Ext_Trig#9 (A1)	Differential (V: -2V ~ 3V)	IN
LR3+, LR4-	Ext_Trig#10 (A2)	Differential (V: -2V ~ 3V)	IN
LR5+, LR6-	Ext_Trig#11 (A3)	Differential (V: -2V ~ 3V)	IN
LR7+, LR8-	Ext_Trig#12 (A4)	Differential (V: -2V ~ 3V)	IN
LR9+, LR10-	Ext_Trig#13 (A5)	Differential (V: -2V ~ 3V)	IN
LR11+, LR12-	Ext_Trig#14 (A6)	Differential (V: -2V ~ 3V)	IN
LR13+, LR14-	Ext_Trig#15 (A7)	Differential (V: -2V ~ 3V)	IN
LR15+, LR16-	Ext_Trig#16 (A8)	Differential (V: -2V ~ 3V)	IN

* UL: Upper Left connector, UR: Upper Right connector;

* LL: Lower Left connector, LR: Lower Right connector.

8. Citations:

Works Cited

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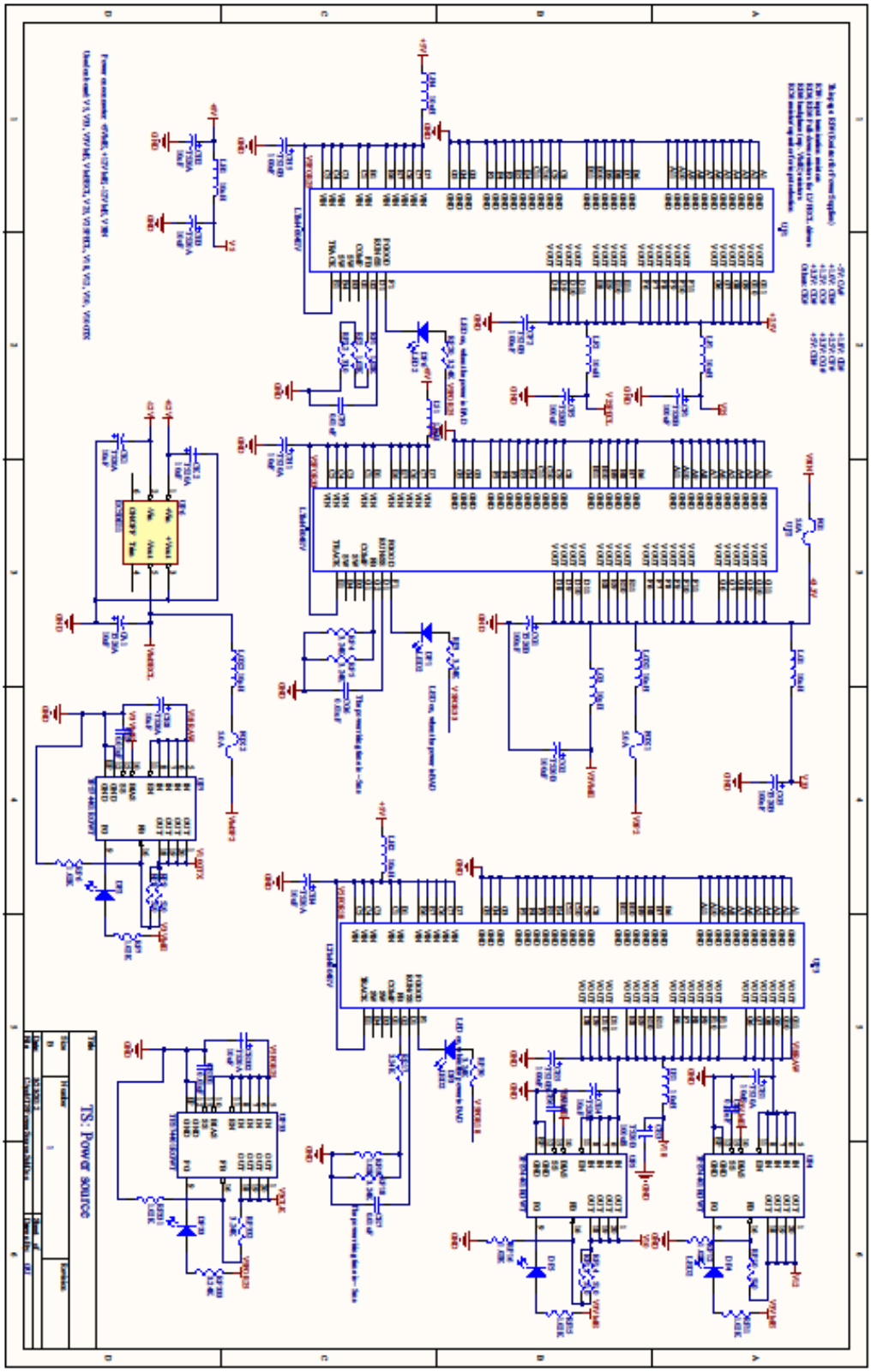
experiments, C. (1990). CEBAF experiements. *journal* , 1-10.

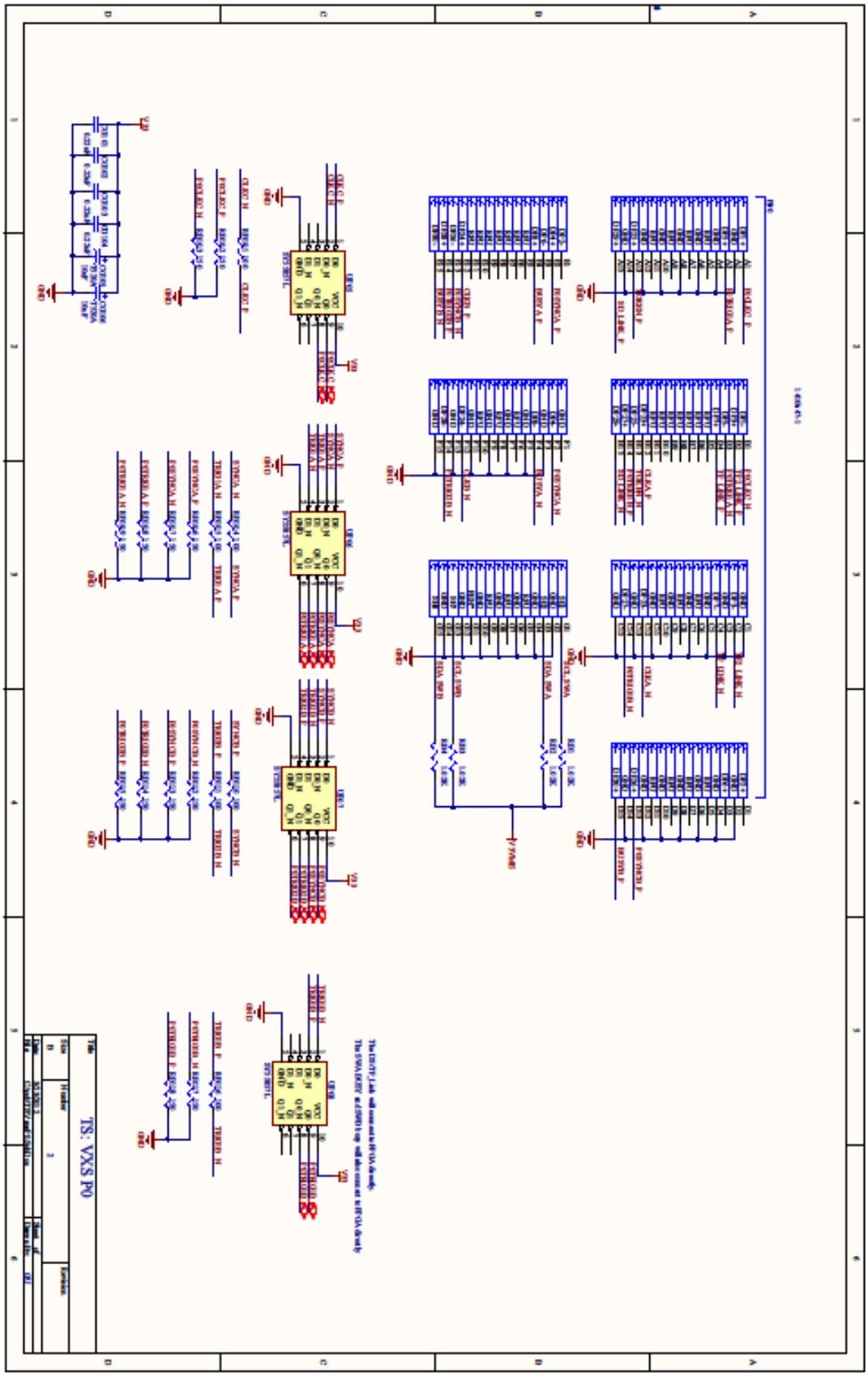
GU, J. W. (2010, August). *VME to I2C engine.* Retrieved from JLAB: http://www.jlab.org/~jgu/works/VMEtoI2C.pdf

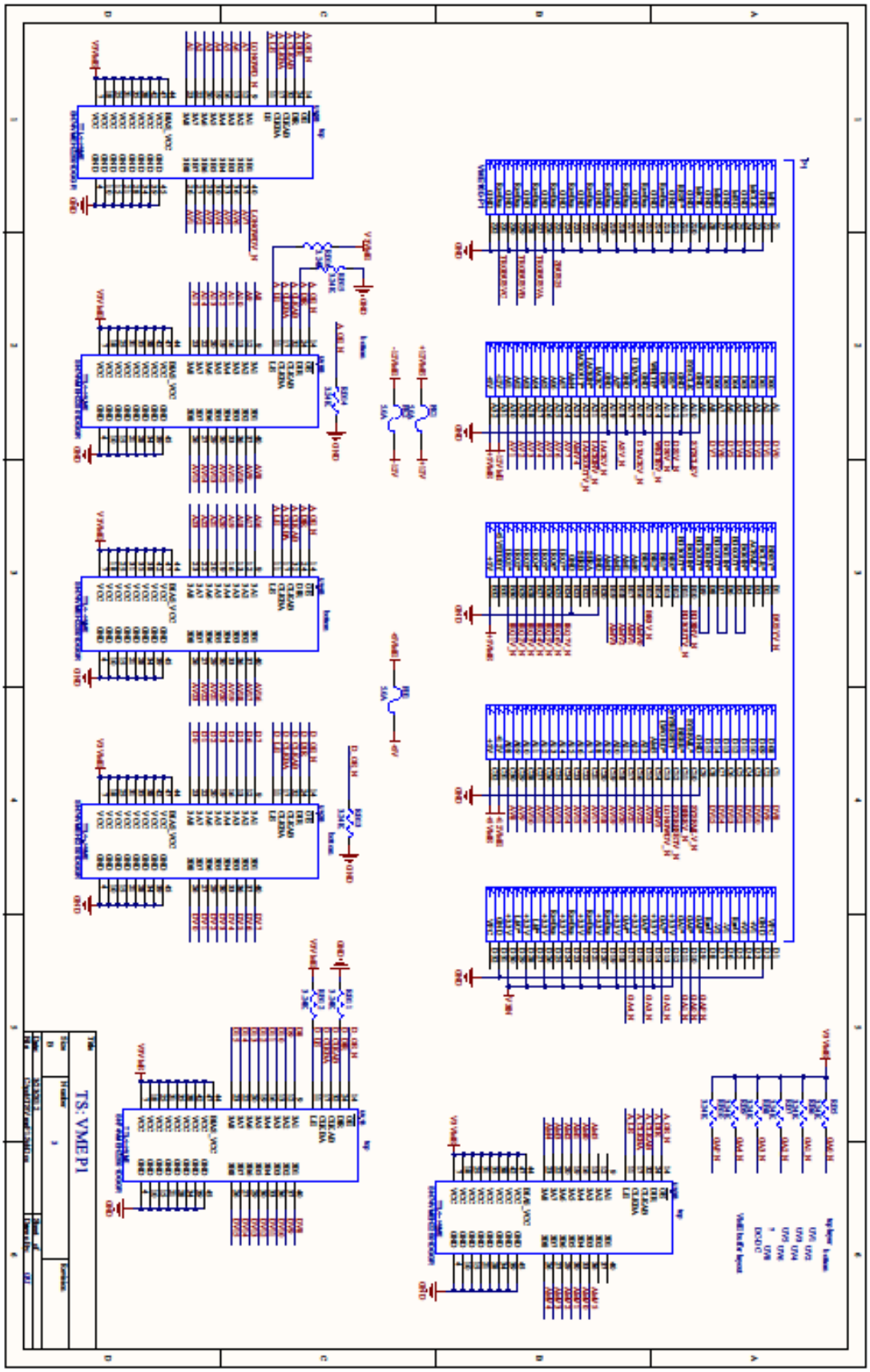
GU, (2010). VME to JTAG implementation

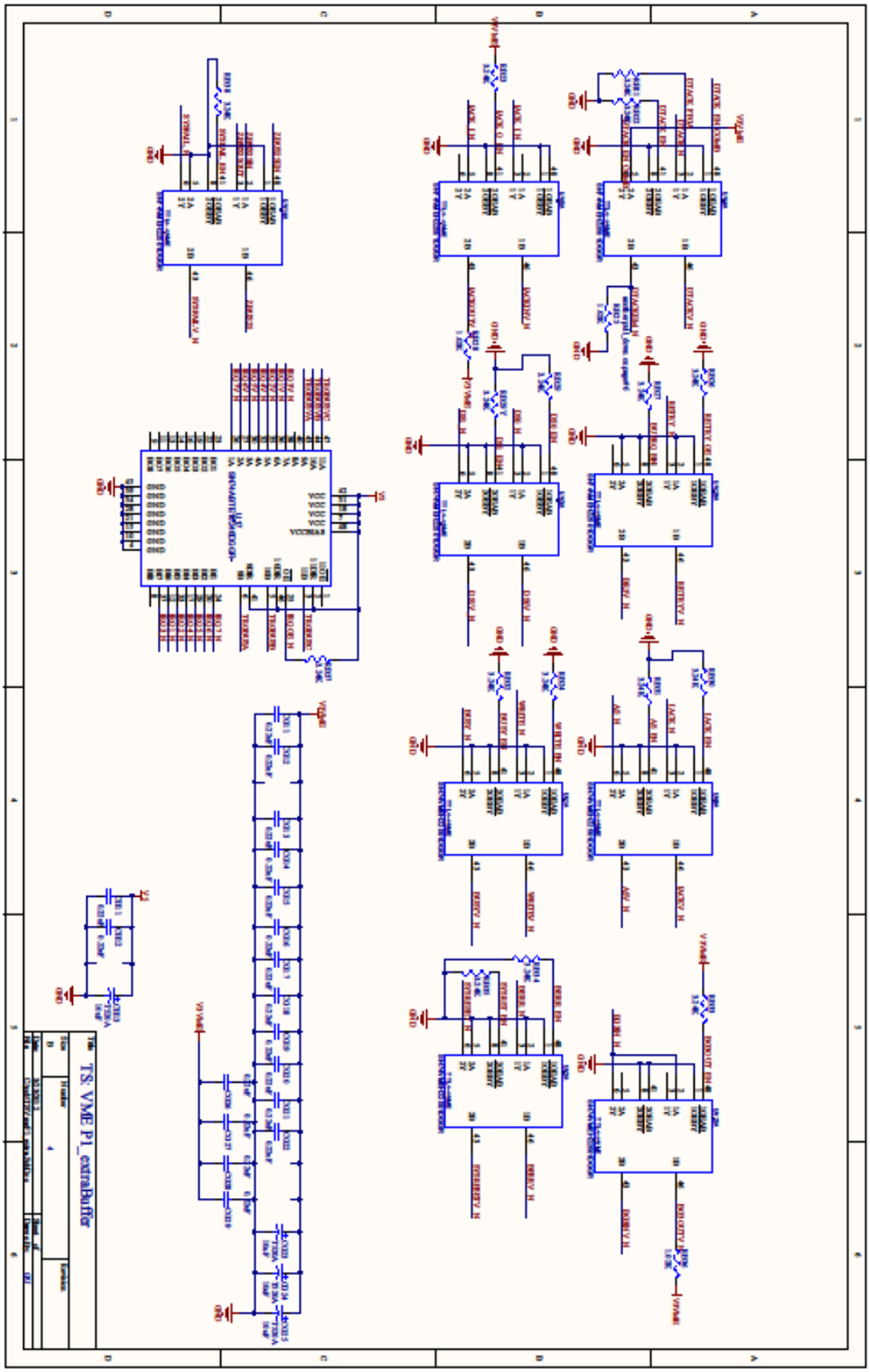
GU, (2010). VME to I2C implementation

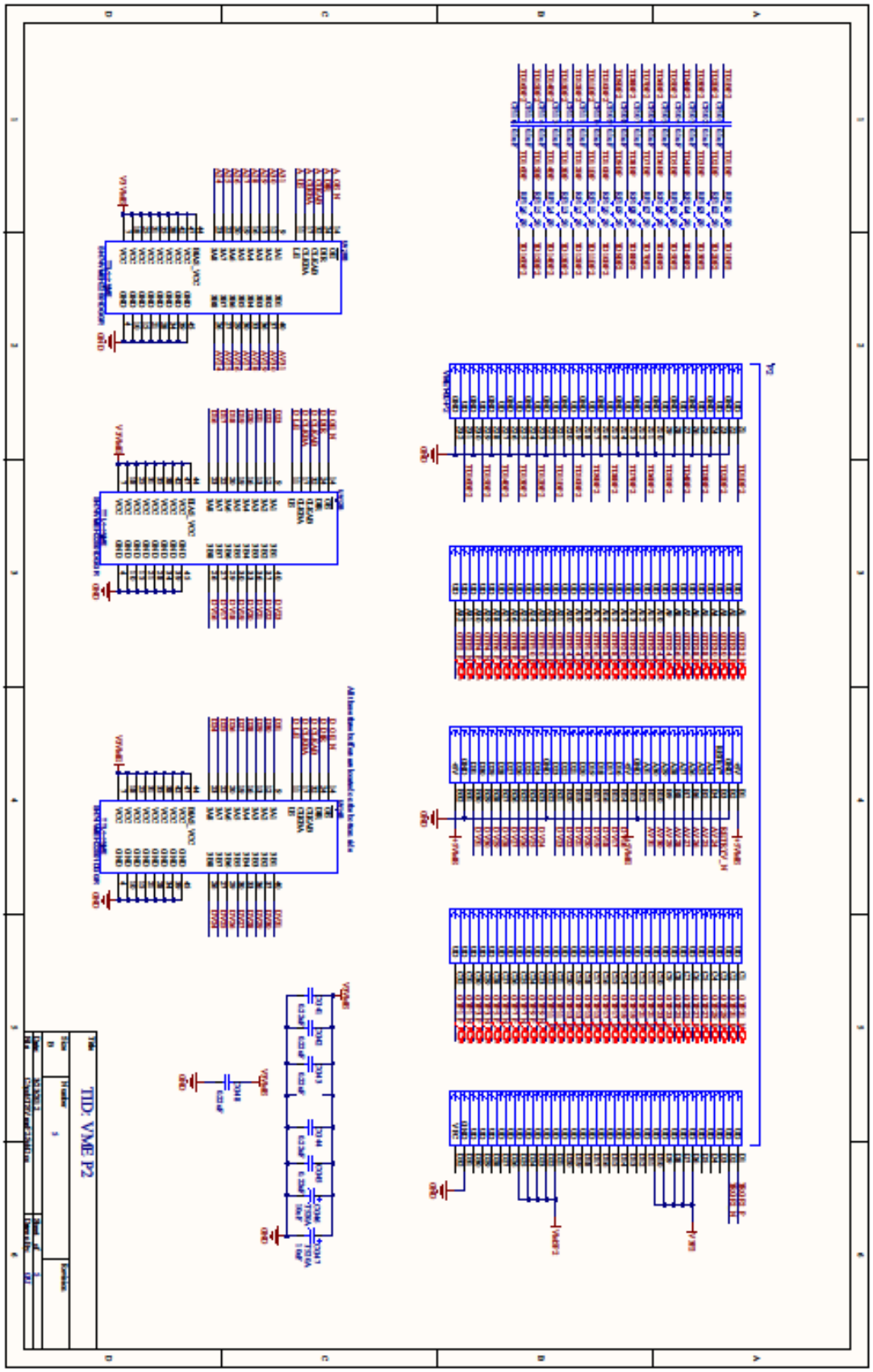
Appendix A: [TS schematics in PDF format]

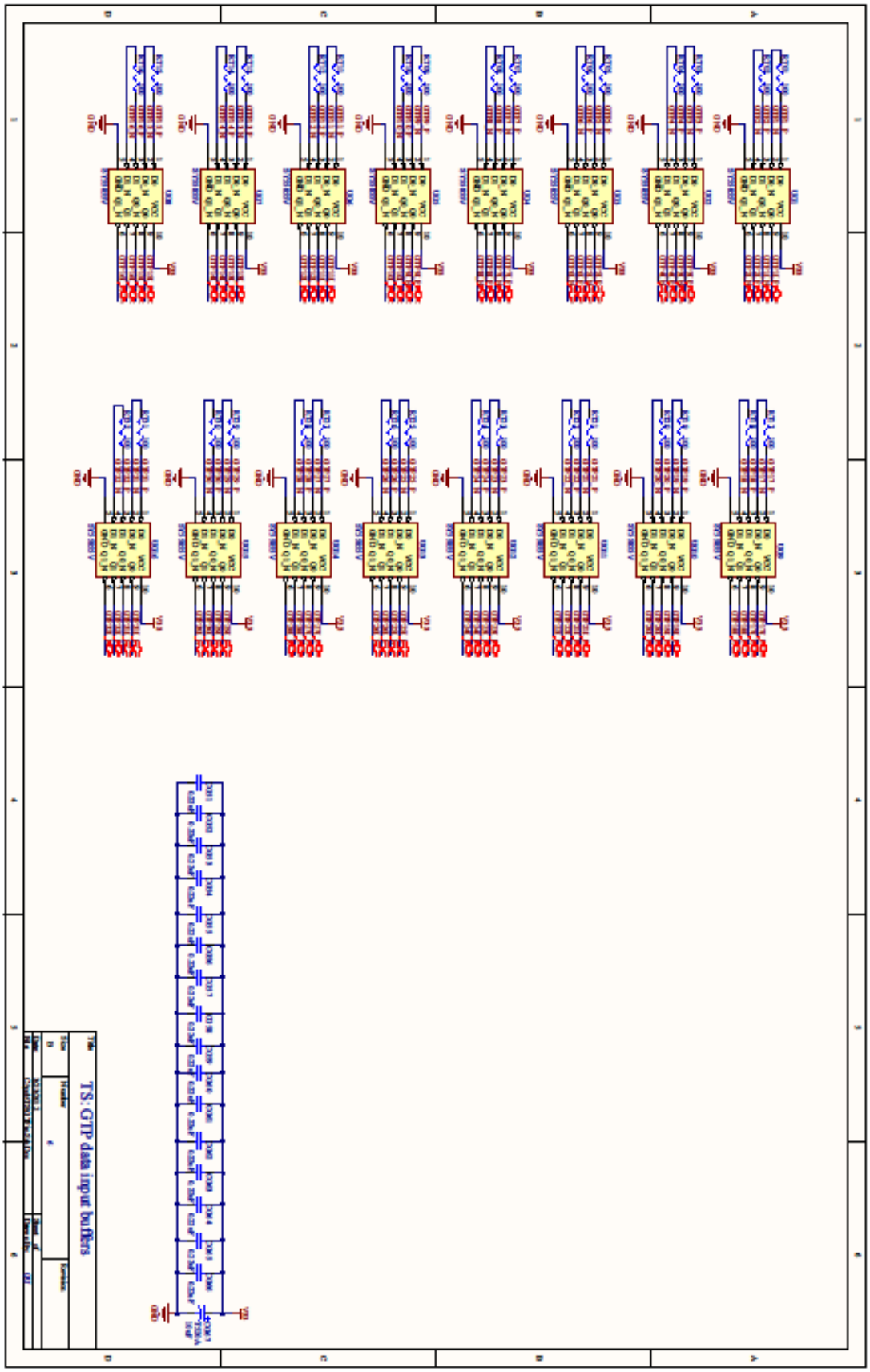


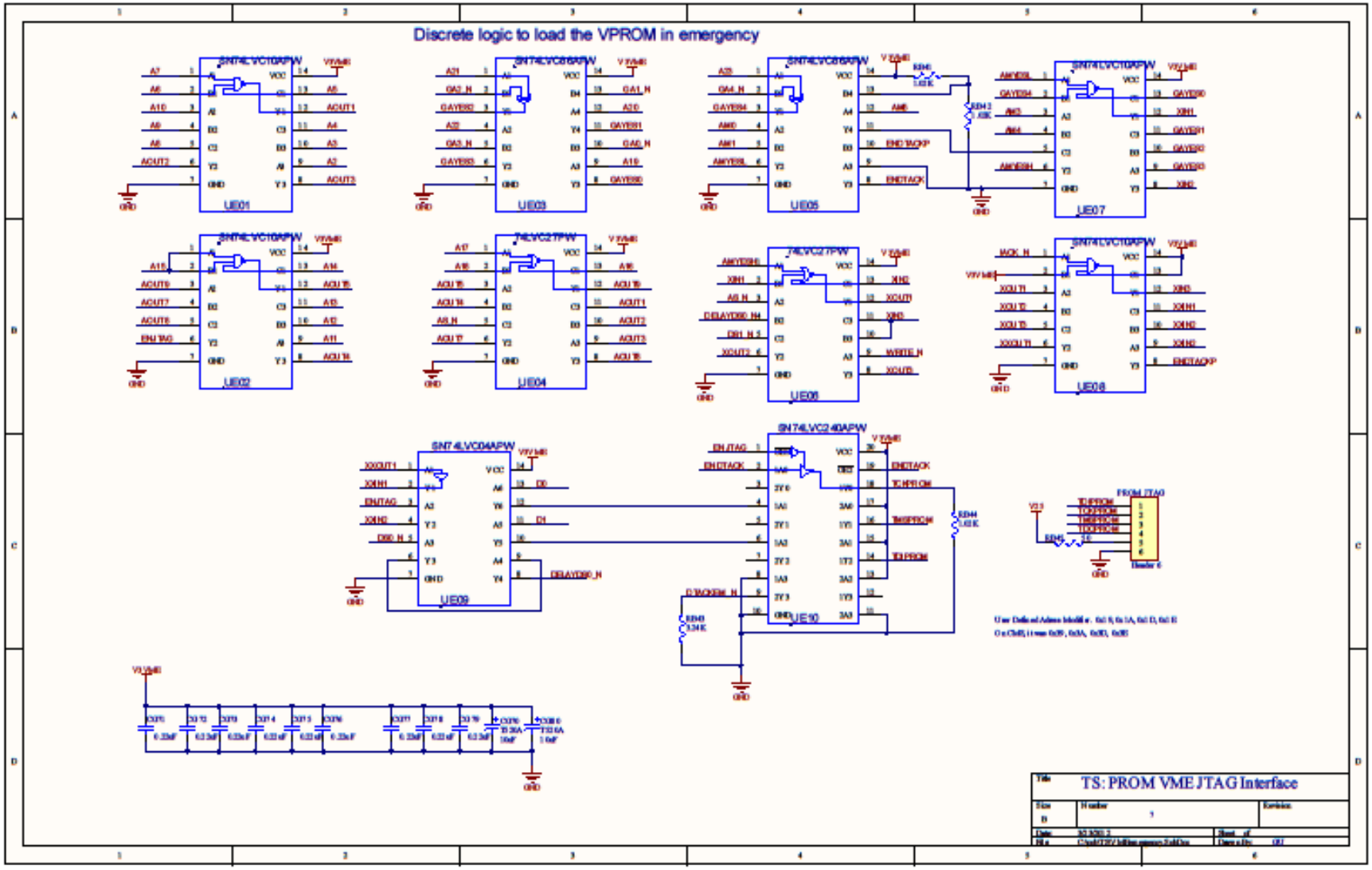

TS: VXS P0

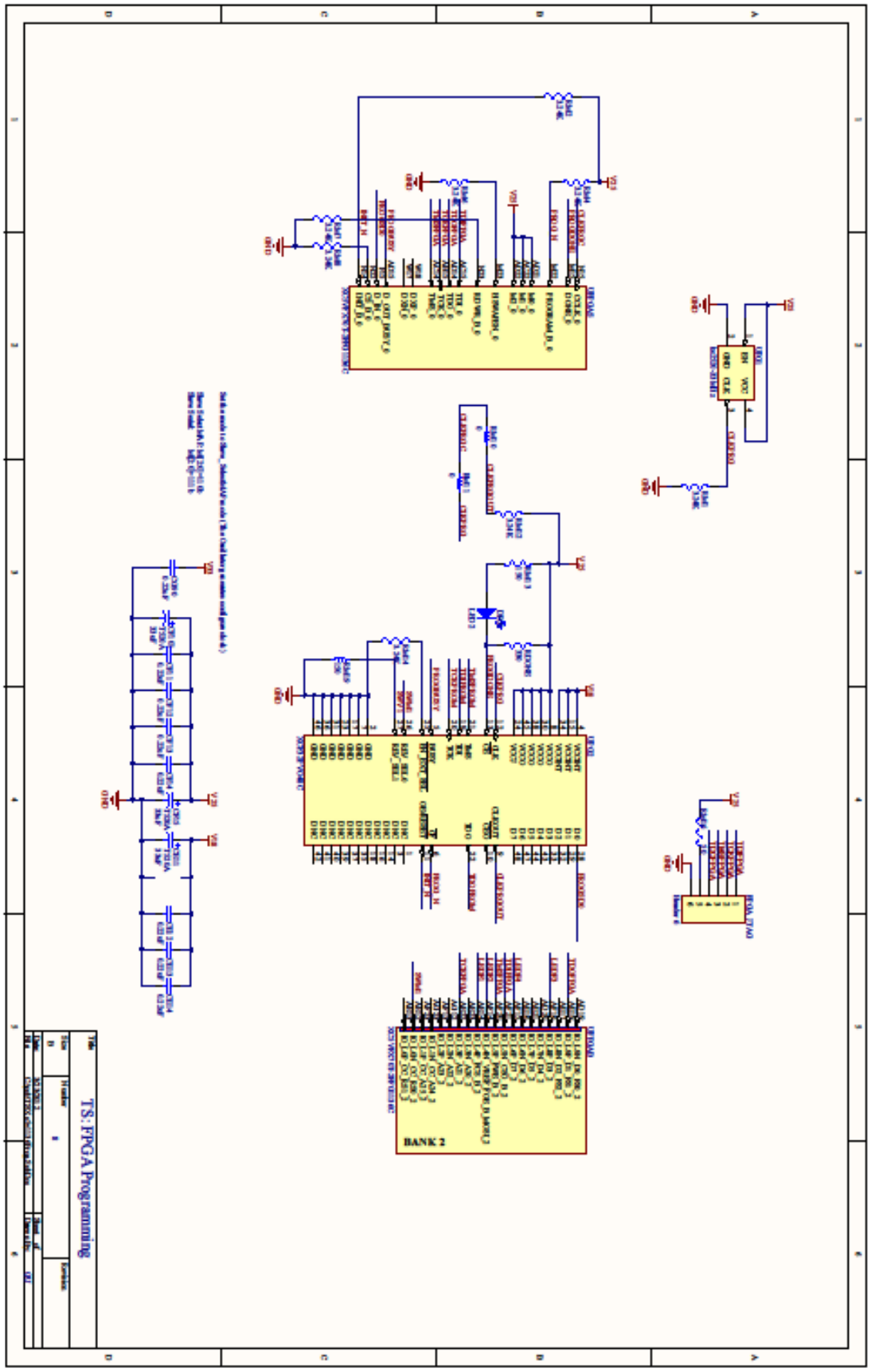

TS: VME P1

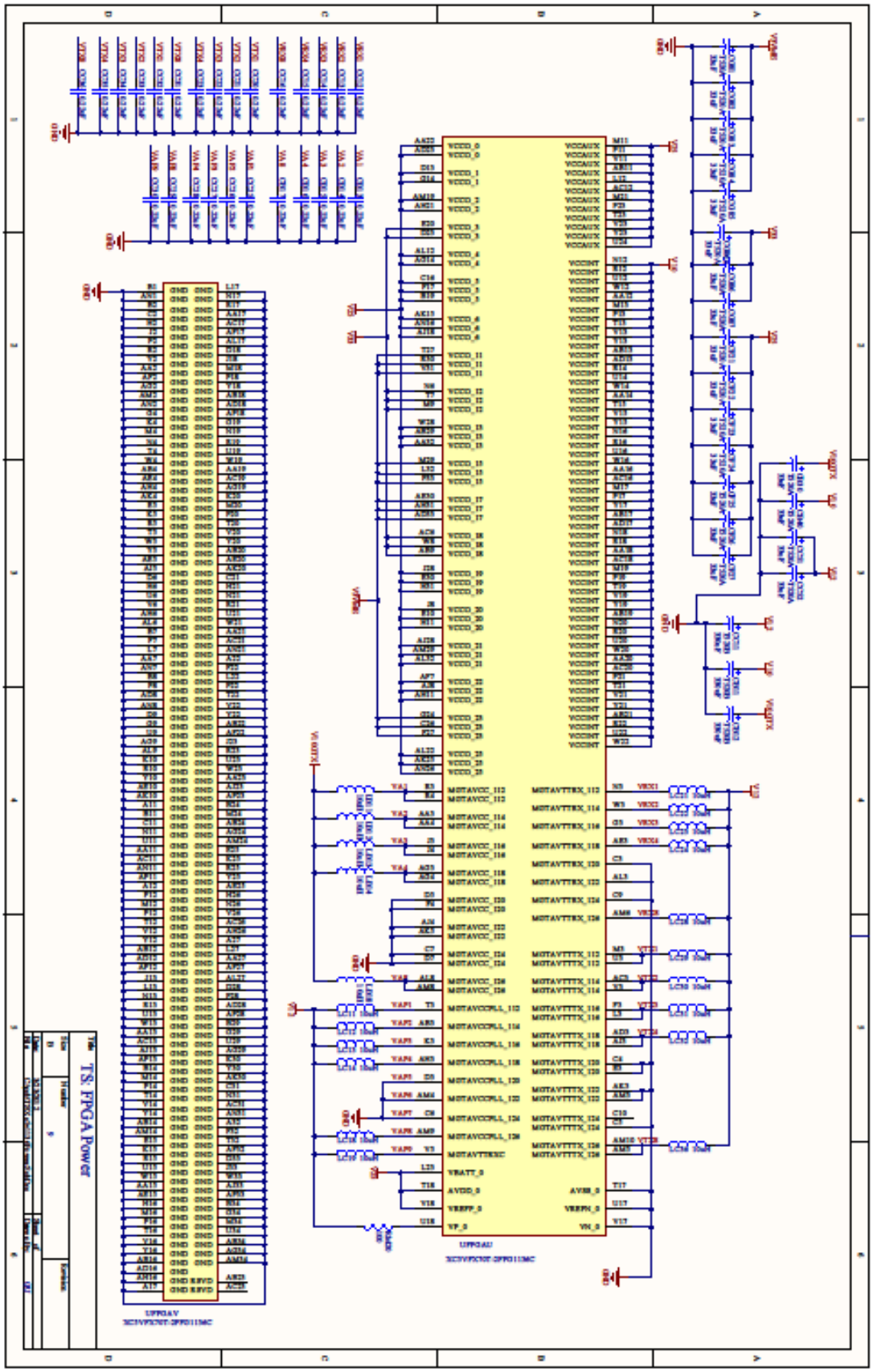

TS: VME P1_extraBuffer

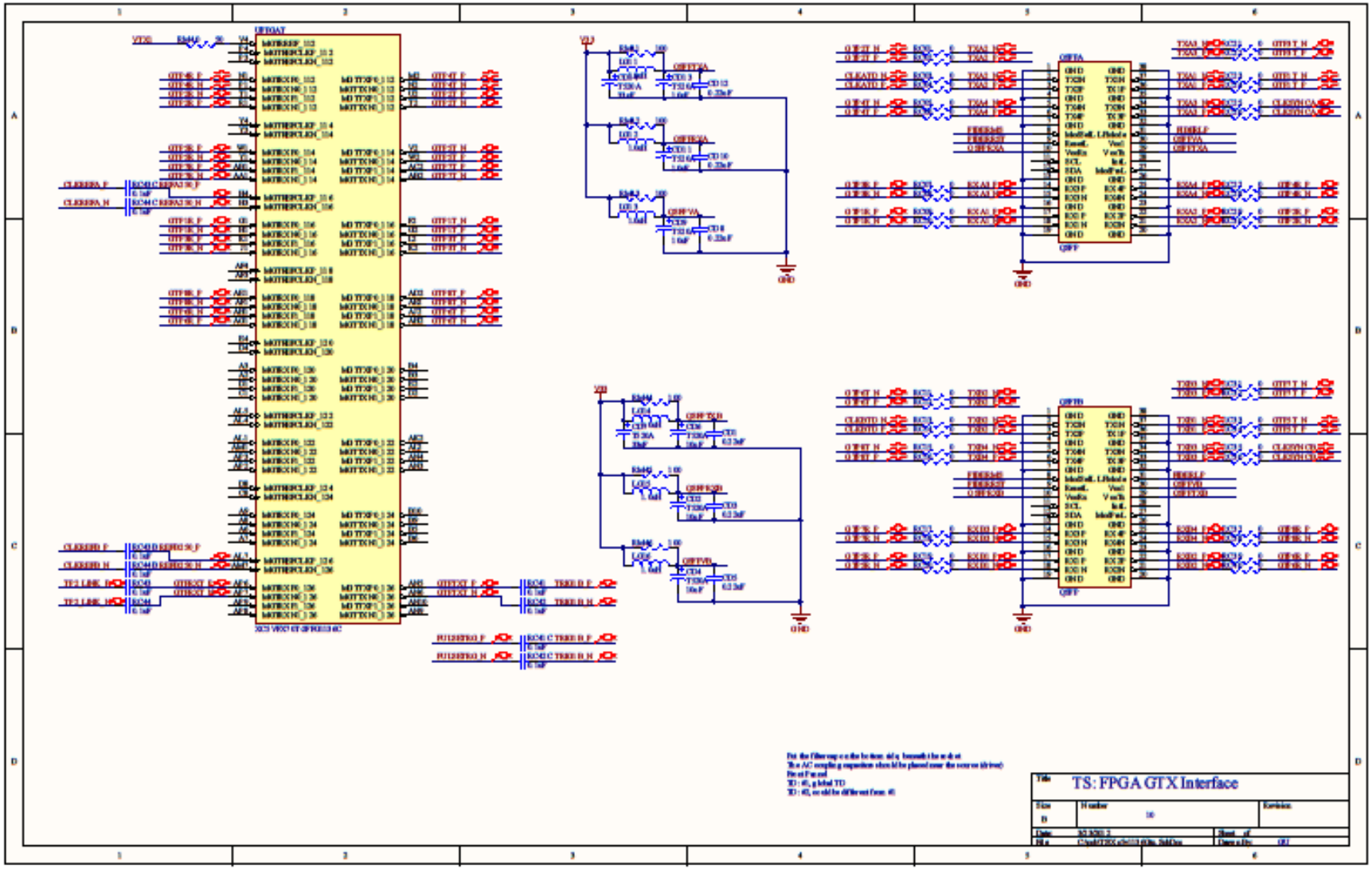

TID VME P2

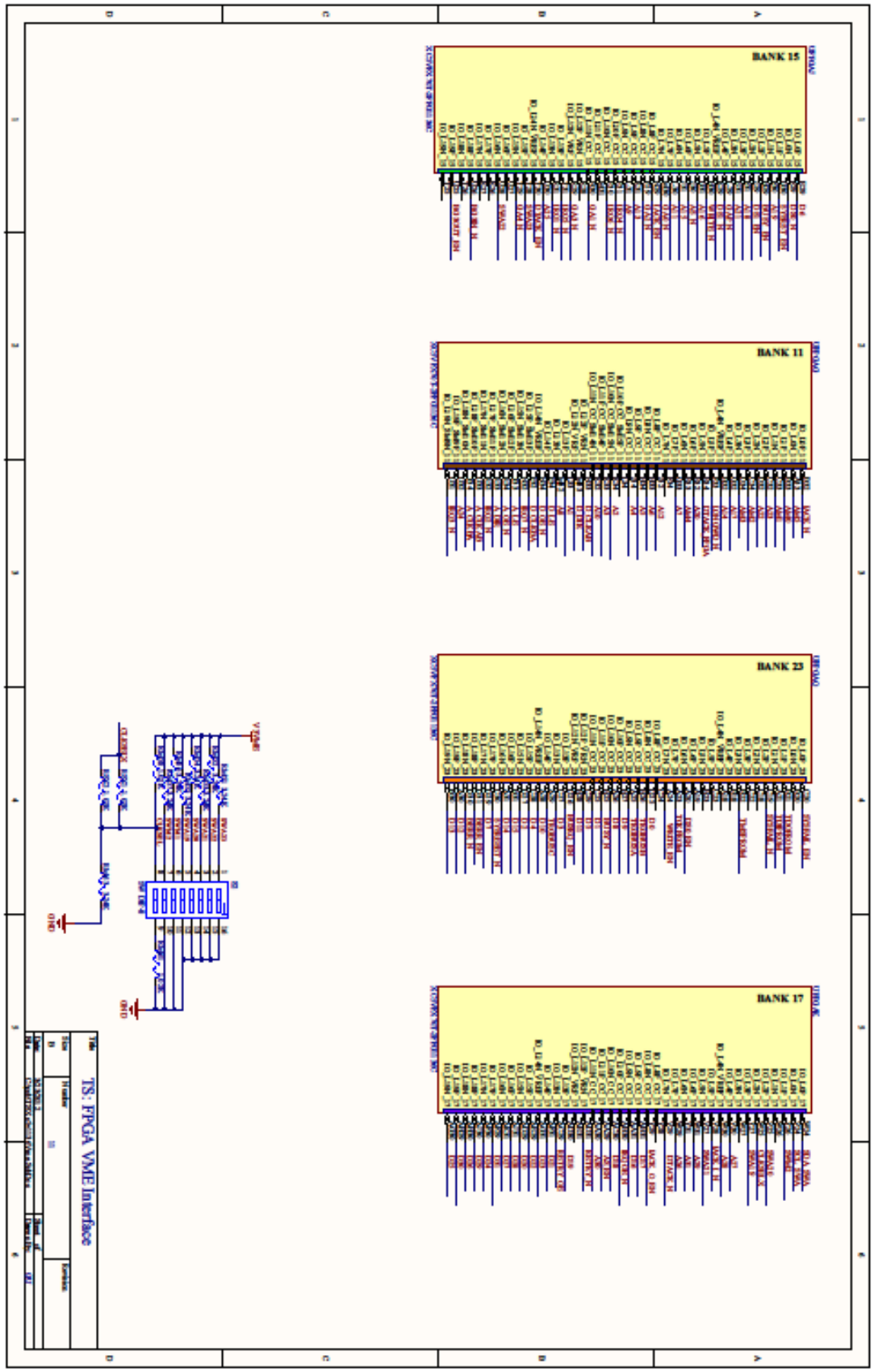

TS: GTP data input buffers

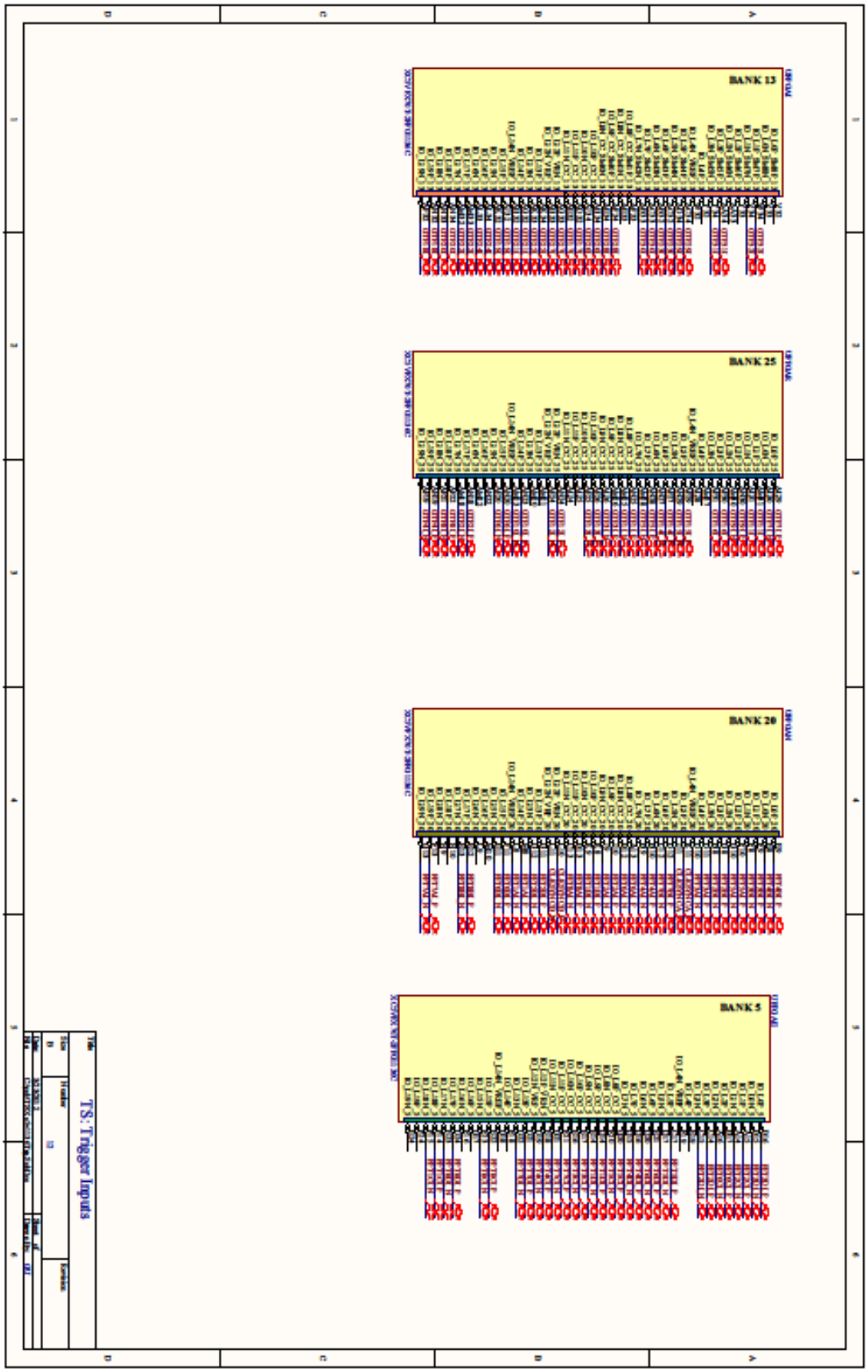

Discrete logic to load the VPROM in emergency
SN74LVC10APW
UE01
UE02
UE03
UE04
UE05
UE06
UE07
UE08
UE09
UE10
SN74LVC04APW
SN74LVC240APW
74LVC27PW
FROM JTAG
TS: PROM VME JTAG Interface

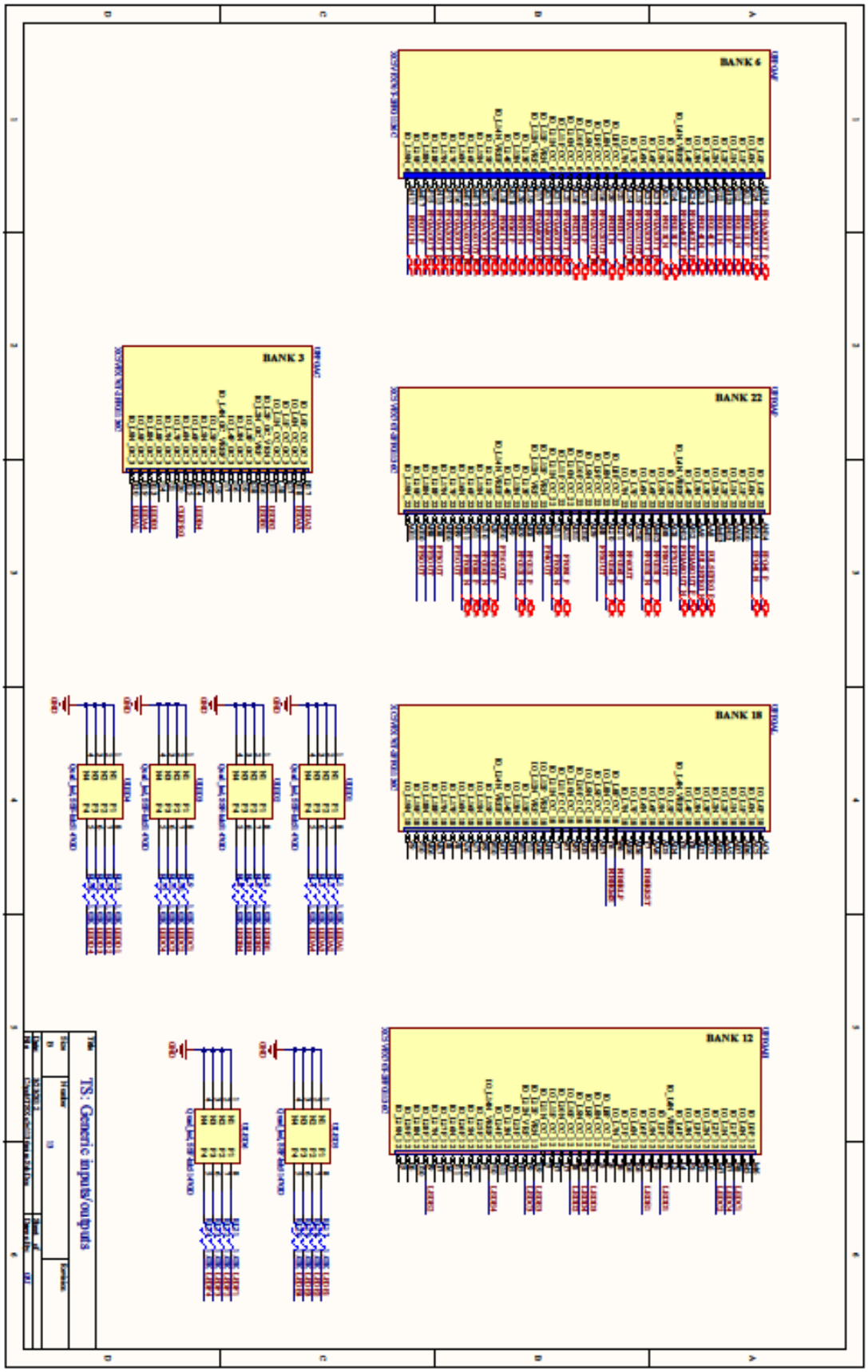

TS:FPGA Programming
BANK 2

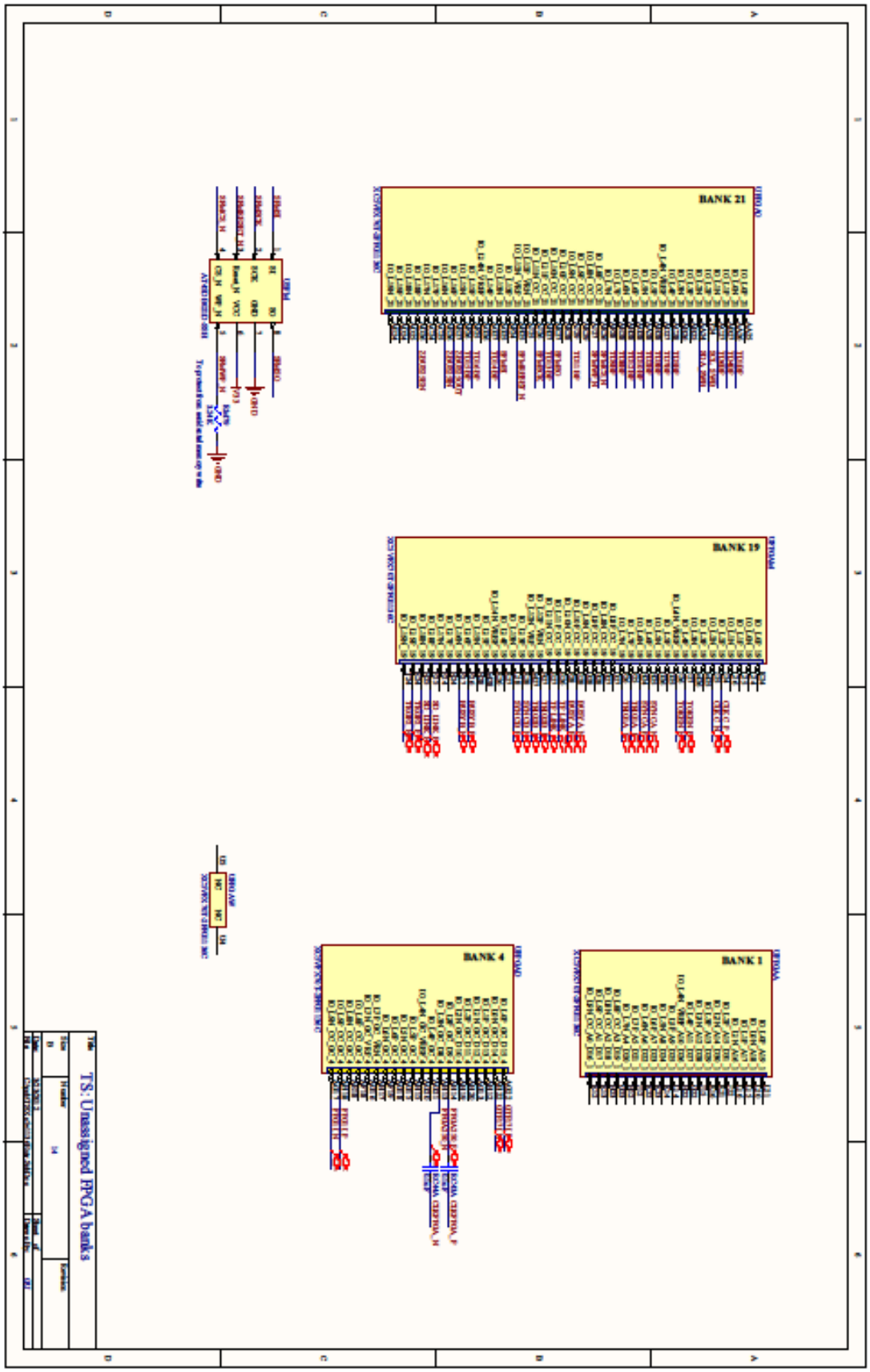

TS: FPGA Power

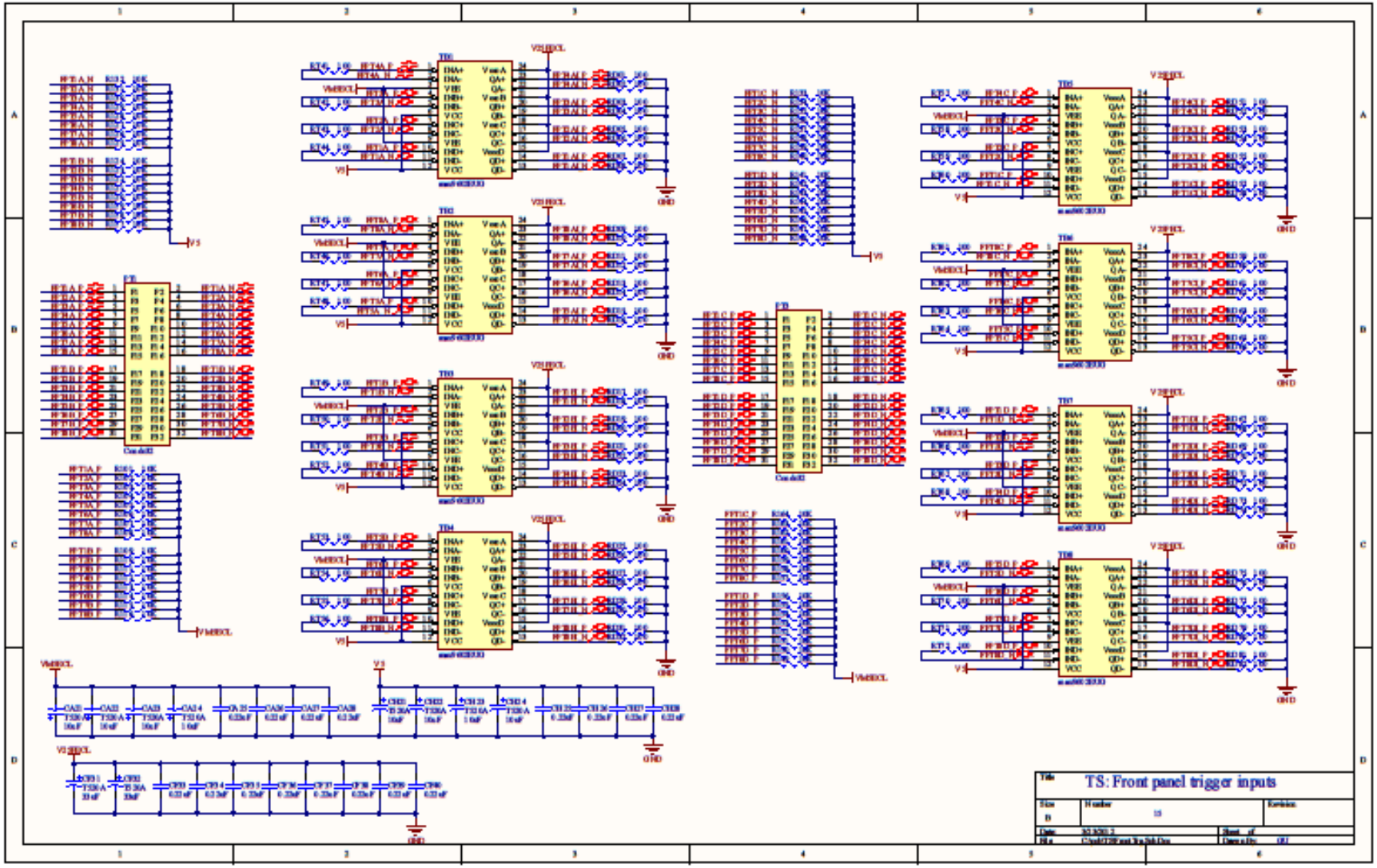

TS: FPGA GTX Interface

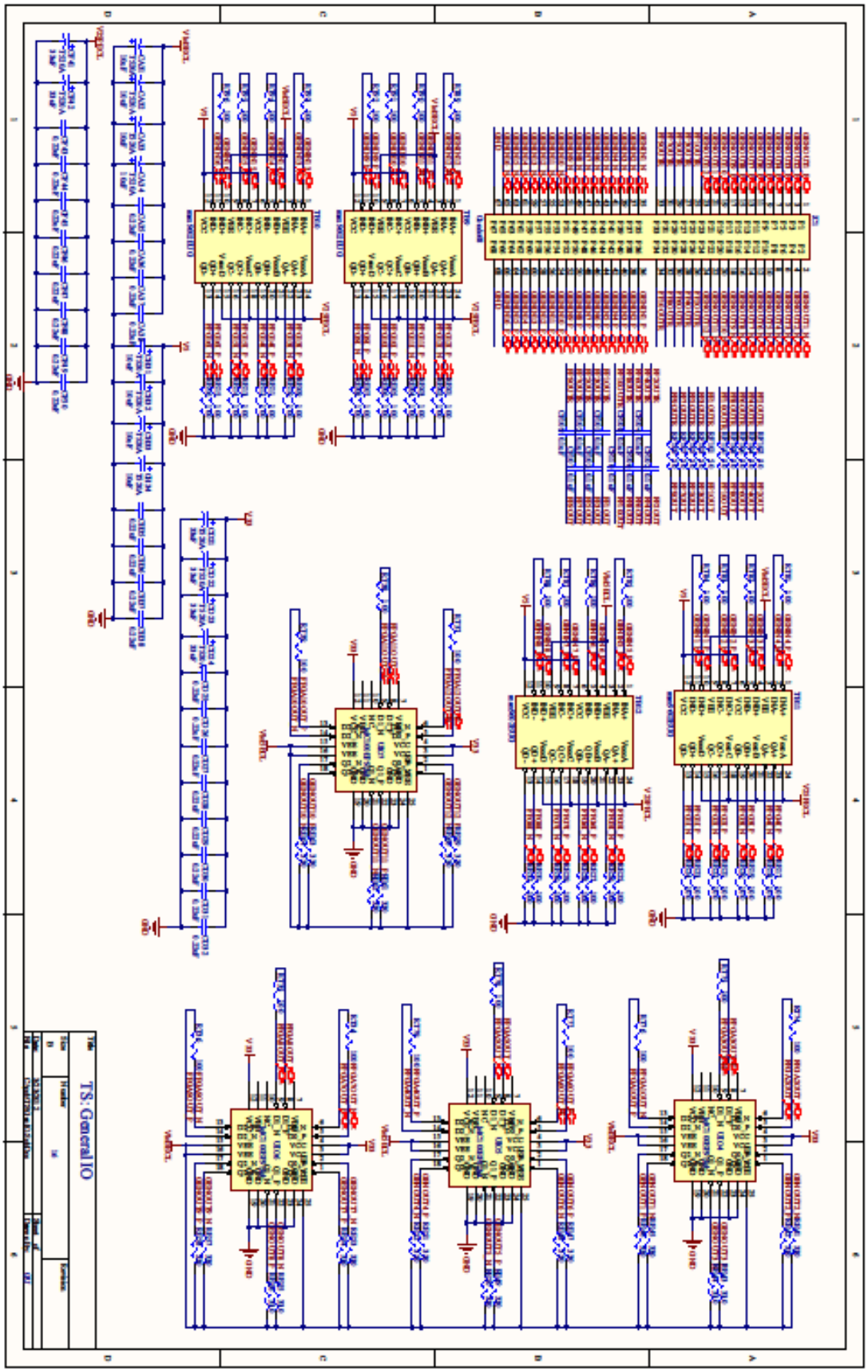

BANK 15
BANK 11
BANK 23
BANK 17
TS: FPGA VME Interface

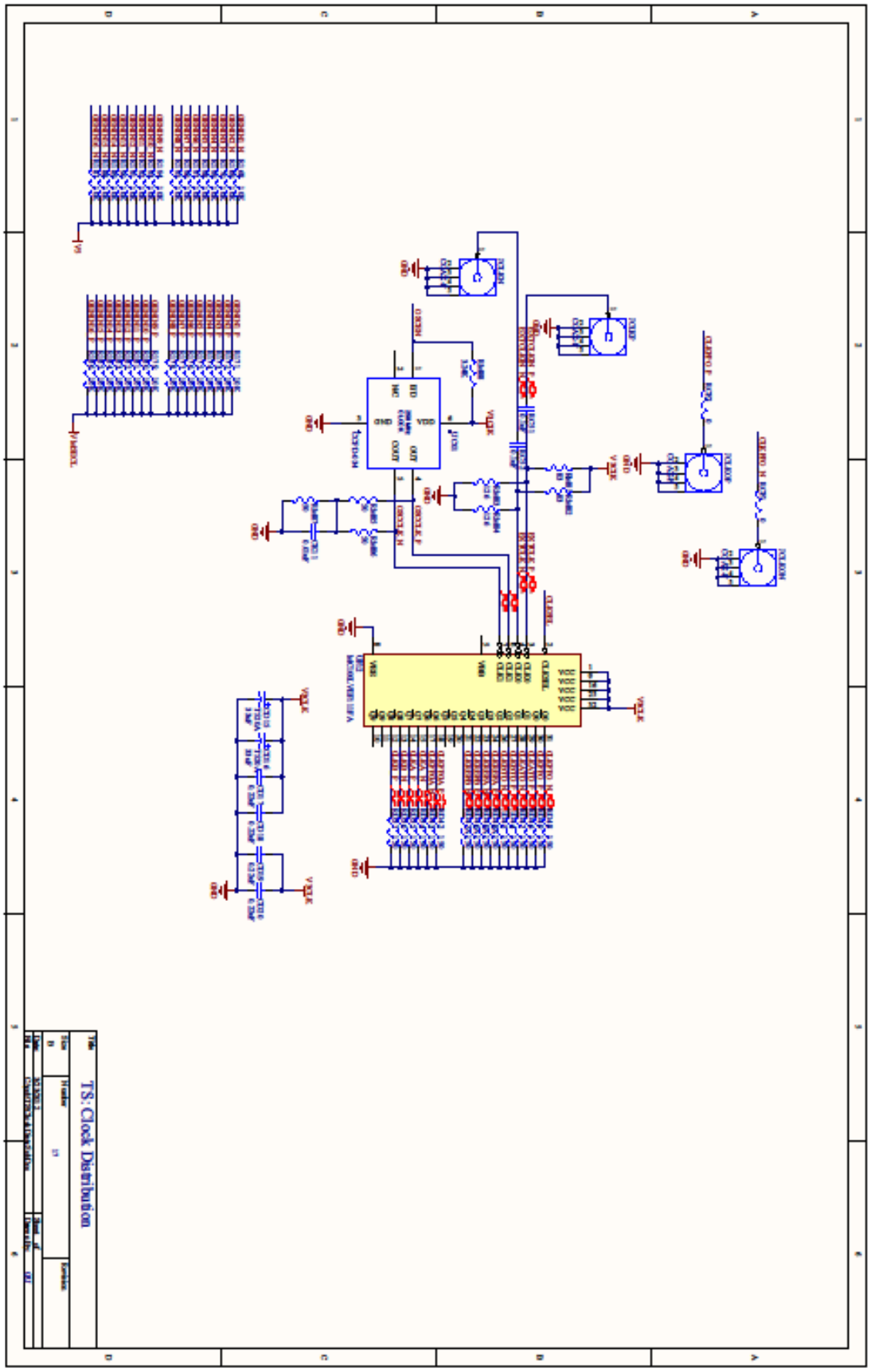

BANK 13
BANK 25
BANK 20
BANK 5
TS: Trigger Inputs

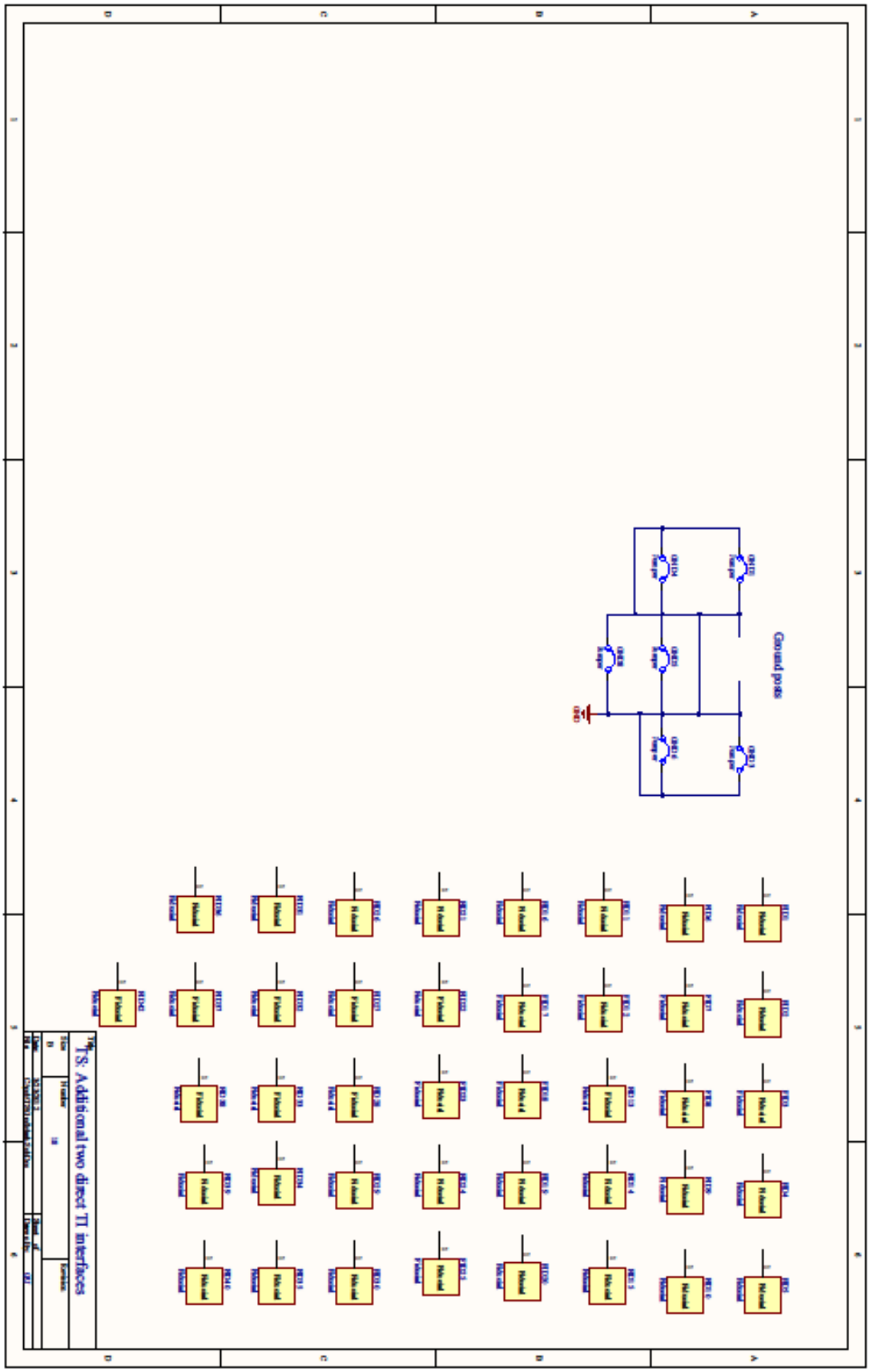

BANK 6
BANK 3
BANK 22
BANK 18
BANK 12
TS: Generic inputs/outputs


BANK 21
BANK 19
BANK 4
BANK 1
TS: Unassigned FPGA banks

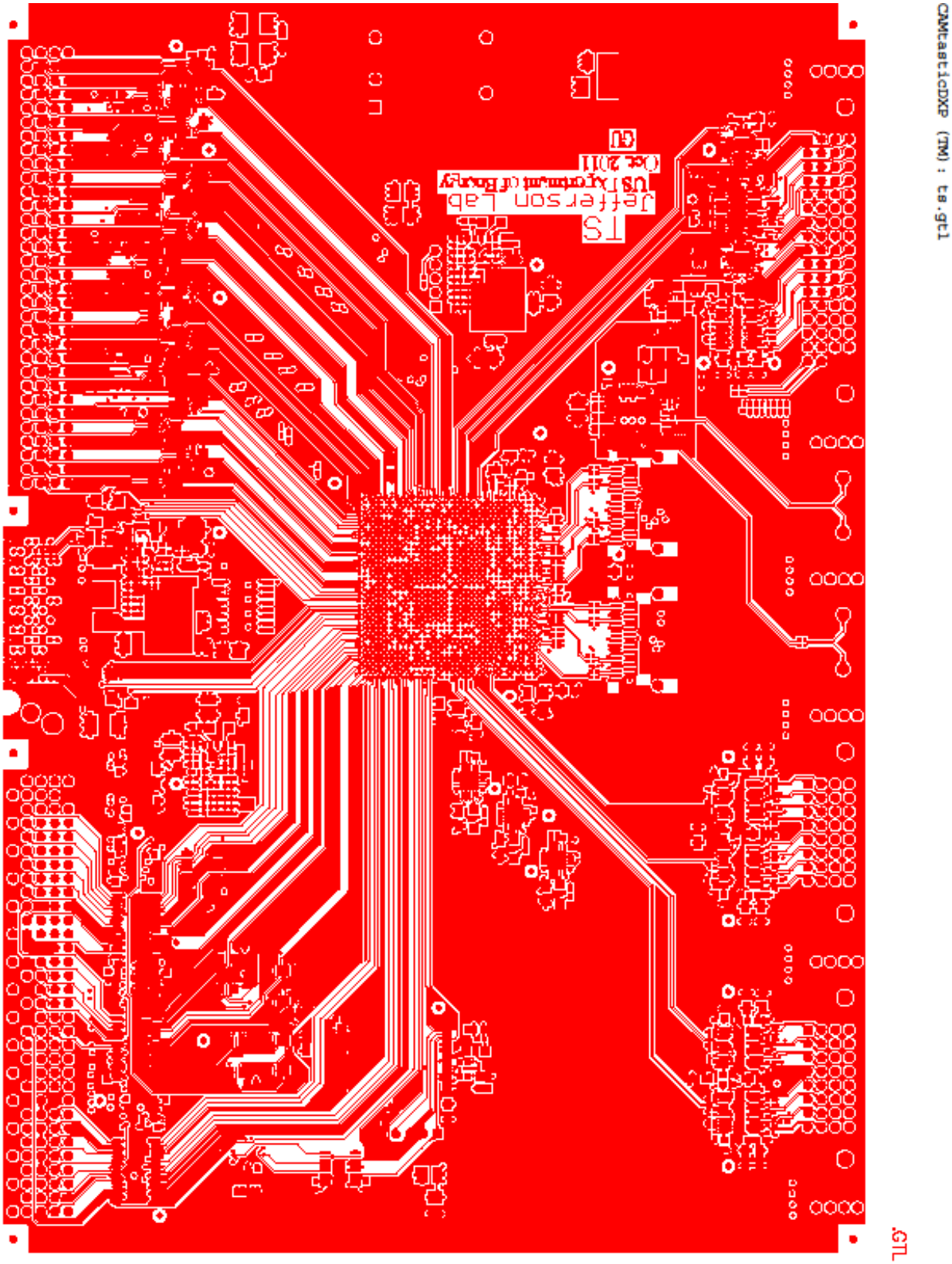

TS: Front panel trigger inputs


TS_GeneralIO


TS: Clock Distribution


Ground pins
TS: Additional two direct TI interfaces

Appendix B: TS Gerber files in PDF format



CAMtasticDXP (TM) : ts.gbl
TS, VER 4, REV. 1
.GBL

Appendix C: Bill of Material

Comment	Description	Footprint	Quantity	Manufacture Part Number
T520A	Solid Tantalum Chip Capacitor, Standard T491 Series - Industrial Grade	A	78	Kemet T520A336M006ATE070
0.22uF	Capacitor, Ceramic Chip Capacitor - Standard	0603	137	TDK C1608X7R1C224K
T520B	Solid Tantalum Chip Capacitor, Standard T520 Series - Industrial Grade	B	12	Keme T520B227M006ATE070
0.01uF	Capacitor (Semiconductor SIM Model)	0402	8	TDK C1005X7R1C103M
0.1uF	Capacitor	0402	40	TDK C1005X7R1C104K
LED2	Typical RED, GREEN, YELLOWGaAs LED	3.2X1.6X1.1	8	Lite-On LTST-C150CKT
5.0A	FUSE 5A SLO BLO NANO 2 SMD	NANO_FUSE	6	TE Connectivity, 1206SFF500F/32-2
Fiducial		fiducial	41	
Header 6	Header, 6-Pin	HDR1X6	2	
Jumper	Jumper Wire	RAD-0.2	6	
Condo68		Condo68	1	3M, x3431-D302xx
COAX-F	RF Coaxial PCB Connector, MCX;	MCX5.08-H5	4	Amphenol, 132203-12
HC_3A	Inductor	1210	11	Taiyo Yuden, BRL3225T1R0M
HF_0.5A	Inductor	0603	21	
1.0uH	INDUCTOR 1.0UH 300MA 20% 0805	0805	6	
VME160-P1	VME160-P1	VME160	1	Harting, 02 01 160 1101
VME160-P2	VME160-P2	VME160	1	Harting, 02 01 160 1101
1410147-1	P0-PL-VXS	P0-105_P0-PL-VXS	1	Tyco, 1410147-1
Condo32		Condo32	2	3M, x3408-D302xx
QSFP		QSFP38	2	FCI, 10099113-101LF socket; 10099114-001LF Cage; Avago, AFBR-79Q4Z Transceiver
10K	RES 0 OHM 1/16W 1% 0402 SMD	0402	96	
1.02K	Resistor	0603	48	
3.24K	Resistor	0603	56	
50	RES 0 OHM 1/16W 1% 0402 SMD	0402	32	
100	RES 0 OHM 1/16W 1% 0402 SMD, RES 100 OHM 1/16W 1% 0402 SMD	0402	201	
150	RES 0 OHM 1/16W 1% 0402 SMD, 5% Tolerance, 0402 Size, 0.063 W	0402	30	
0	RES 0 OHM 1/16W 1% 0402 SMD, 5% Tolerance, 0402 Size, 0.063 W	0402	44	
330	RES 0 OHM 1/16W 1% 0402 SMD	0402	26	
83	RES 0 OHM 1/16W 1% 0402 SMD	0402	2	
126	RES 0 OHM 1/16W 1% 0402 SMD	0402	2	
510	RES 0 OHM 1/16W 1% 0402 SMD	0402	5	
SW DIP-8	DIP Switch, 8 Position, SPST	SW16_L	1	
max9602EUG		MTC24_N	12	maxim, MAX9602EUG
SN74ABTE16246DGGR	IC 11-BIT I-WS BUS TXRX 48-TSSOP	TSSOP50P610-48AL	1	
CCPD-034	CCPD-034	SO6-5X7	1	
SN74LVC10APW		TSSOP14	4	
SN74LVC86APW		TSSOP14	2	
74LVC27PW		TSSOP14	2	
SN74LVC04APW		TSSOP14	1	
SN74LVC240APW		TSSOP20	1	
MC100LVEP111FA	Low-Voltage 1:10 Differential LVECL/LVPECL/LVEPECL/HSTL Clock Driver	873A-02_N	1	
XC5VFX70T-2FFG1136C	Xilinx Virtex-5 FXT Platform FPGA, 1136-Ball FFBGA, Speed Grade 2, 640 User I/Os, Commercial Grade, Pb-Free	FFG1136	1	Xilinx, XC5VFX70T-2 FFG1136C
SY55855V	Dual LVPECL to LVDS translator	TSSOP50P490-10AN	16	
MC100EP91M	On Semiconductor, Any level positive to ECL translator	QFN50P400X400-24W4M	4	
Quad_led, SSF-lxh5147GD	LUMEX, Quad pack LEDs	LED14	6	
LTM4604EV	LTM4604EV	LGA-66_LTM4604EV(Primary)	3	Linear Technology, LTM4604AEV#PBF
TPS74401RGWT	IC LDO REG 3.0A W/SS 20-VQFN	QFN-20	4	
SY55857L	Micrel dual Anylevel to LVPECL translator	TSSOP50P490-10AN	4	
EC5BE11		EC5BE17	1	
kc2520-33MHz	Miniature Oscillator	CFPX-5	1	
XCF32PVO48C	XCF00P Series, Platform Flash In-System Programmable Configuration 1.8V PROM, 48-Pin TSSOP, 32-Megabit, Commercial Grade	VO48	1	
AT45DB021D-SSH	Atmel flash memory	8S1_N	1	
SN74VMEH22501DGGR	IC UNIV BUS TXRX TRI-ST 48-TSSOP	TSSOP50P610-48AL	9	

Revision history:

First version on Oct. 21st, 2010

Nov. 8, 2010: updated to reflect the recent discussions and comments

Sept. 30, 2011: Updated according to the PCB design

Mar. 21, 2012: Major updates to reflect the hardware/firmware development

May 9, 2012: minor updates on A24 registers

Aug. 23, 2012: Major updates, with the addition of TS partitioning (Sub_TS#1, #2, #3 and #4).