Nuclear Physics Division

Data Acquisition Group

Description and Technical Information for the VME Trigger Interface (TI) Module

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1 Introduction

The Trigger Interface (TI) module is being designed for the Jefferson Lab 12GeV upgrade, mainly for HallD [(Collaboration G. , 2009)] and Hall-B [(Collaboration C. , 2009)], with other experimental Halls [(experiments, 1990)] compatibility. The TI boards are located in data acquisition frontend crates, and are responsible for providing a low-jitter system clock, sync signals and fixed latency trigger signals for the Front-end readout boards in the crates. The modules also merge the front-end crate status and generate a BUSY signal to request the Trigger Supervisor (TS) to pause the trigger. For the detailed description, refer to the Trigger Distribution system design document [Trigger Distribution]. Figure 1a shows the placement of the TI modules in the global trigger distribution scheme in experiment setup. Figure 1b shows the crate level diagram

Figure 1a:

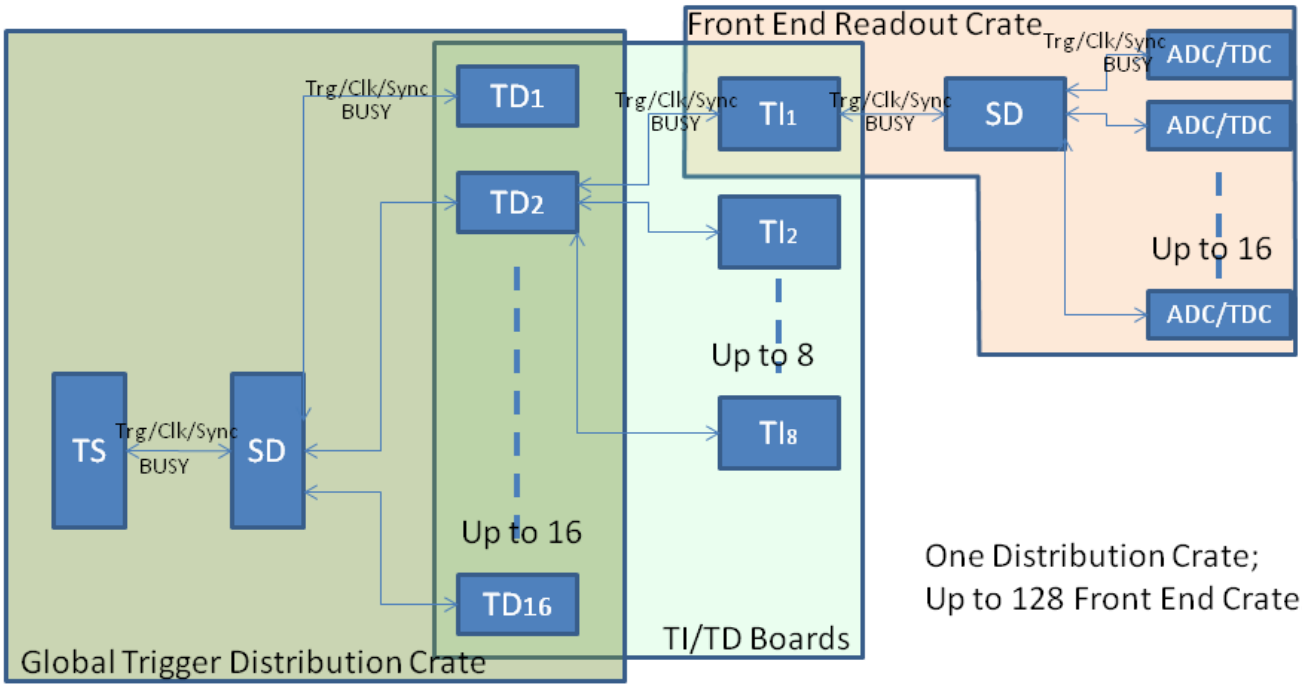
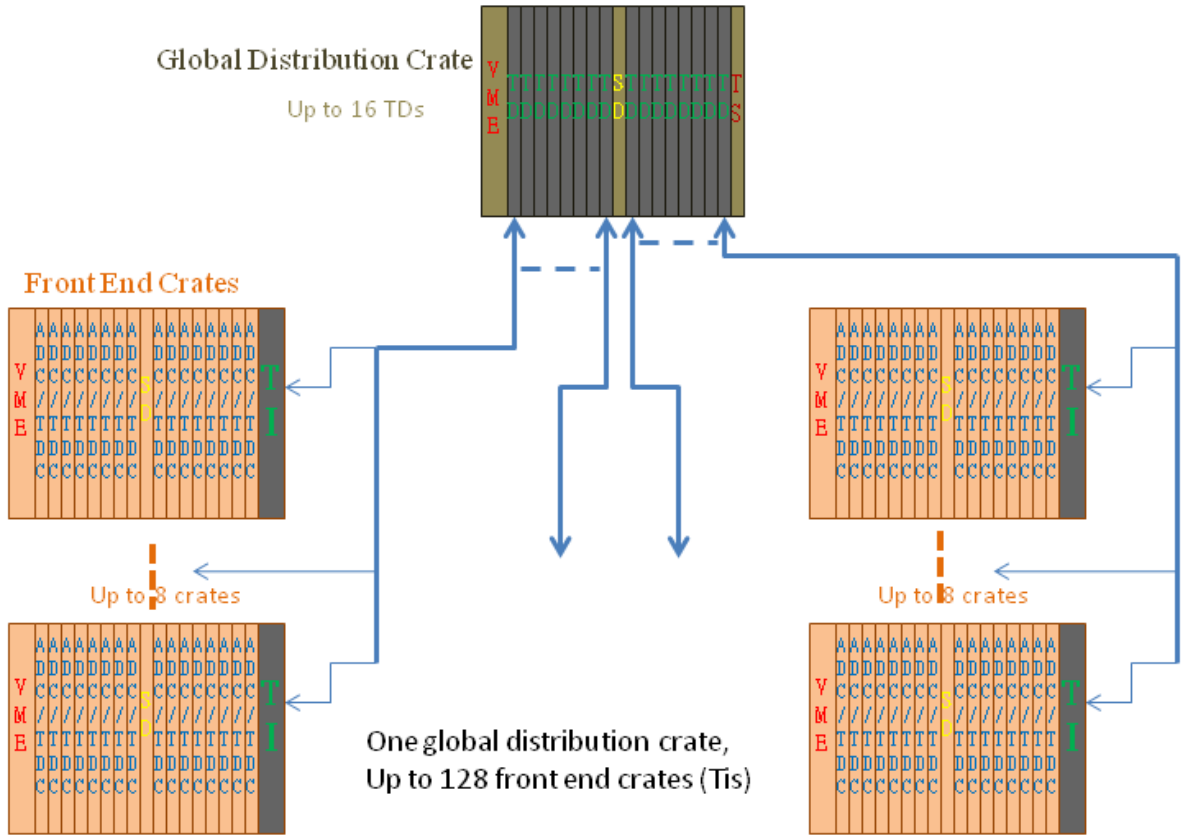


Figure 1b:



The TI shares the same PCB design as the Trigger Distribution (TD) board. The TI board has simple Trigger Supervisor (TS) functions built in. The TI can act as a subsystem trigger supervisor when used independently. The TI board can have optionally eight optic fibers populated, and distribute Trigger/Clock/Sync to another 8 (eight) TI boards. A subsystem with up to nine crates can be setup without a real TS module. The TI also has the flexibility to select the trigger and clock inputs from central trigger system or local (sub-system) trigger system.

2 Purpose of the module

TI board is positioned in the last slot of the front-end data acquisition crate, and connects to a TD module in the global trigger distribution crate. This is done using a four channels full-duplex fiber link, which provides a gigabit trigger link, global 250MHz clock and synchronization link to phase lock the trigger and initialize the system. The trigger link uses a reference clock derived from the 250MHz global pipeline clock allowing a trigger word to be distributed every 4 global pipeline clock cycles. Depending on the trigger word type the TI can issue a crate level trigger condition through the VXS switch port B. The trigger bits are sent to a Signal Distribution (SD) module that distributes these signals to all front-end modules in the crate. The TI also accepts status signals from the SD module, which is the logical OR of the status signals from all the other front-end modules. These status signals can be transmitted back to the TS through the fiber link to slow down or inhibit further distribution of triggers until the status has been resolved. For now, the status includes a BUSY only. When the BUSY is set, the front end boards are requesting for trigger inhibit. The assertion of a status signal will create a dead-time in the data acquisition system which should be a rare occurrence since the data acquisition is being designed to handle the full trigger rate that can occur from the physics events. The dead time will be monitored and recorded by the Trigger Supervisor board.

The TI can also perform simple Trigger Supervisor functions. In test setup or commissioning setup, the TI can perform as a TI Master (TM). In this case, it can take inputs from its front panel and generate trigger/clock like a TS, it can sends the trigger, clock, and SYNC to the backplane (P0 and P2) like a TI, and it can send the trigger, clock and SYNC to the front panel fibers like a TD. With the TM, a test setup can include up to nine (9) crates. Figure 2a shows the setup. Figure 2b shows the crate level diagram.

Figure 2a

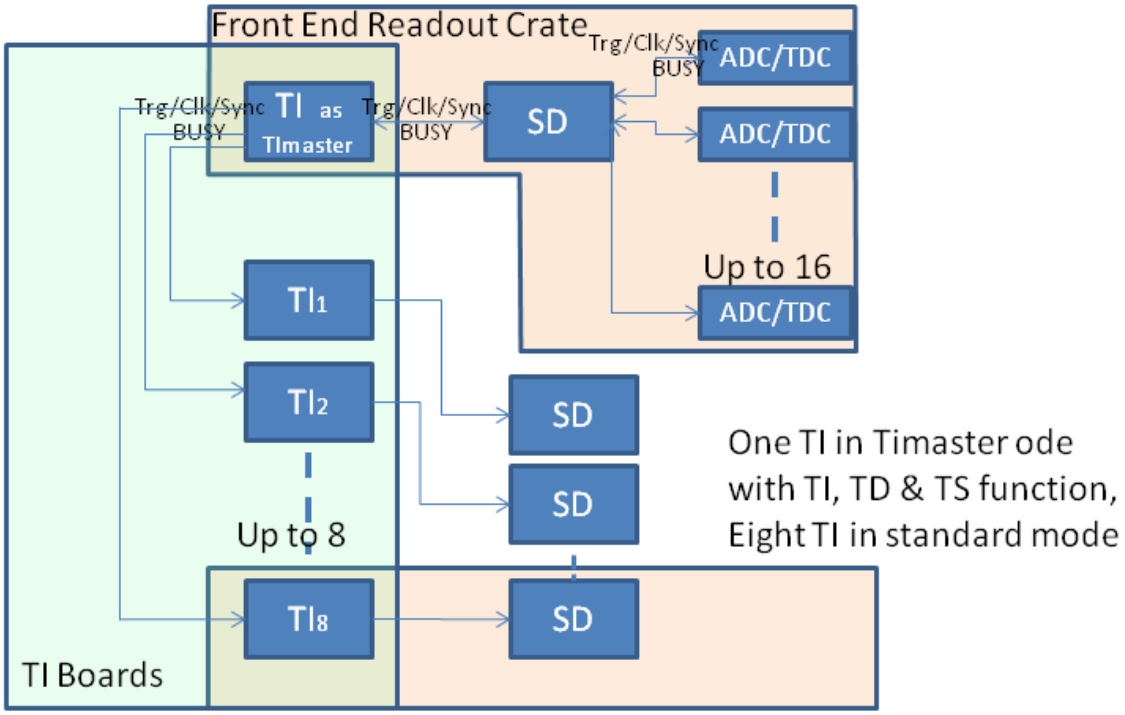
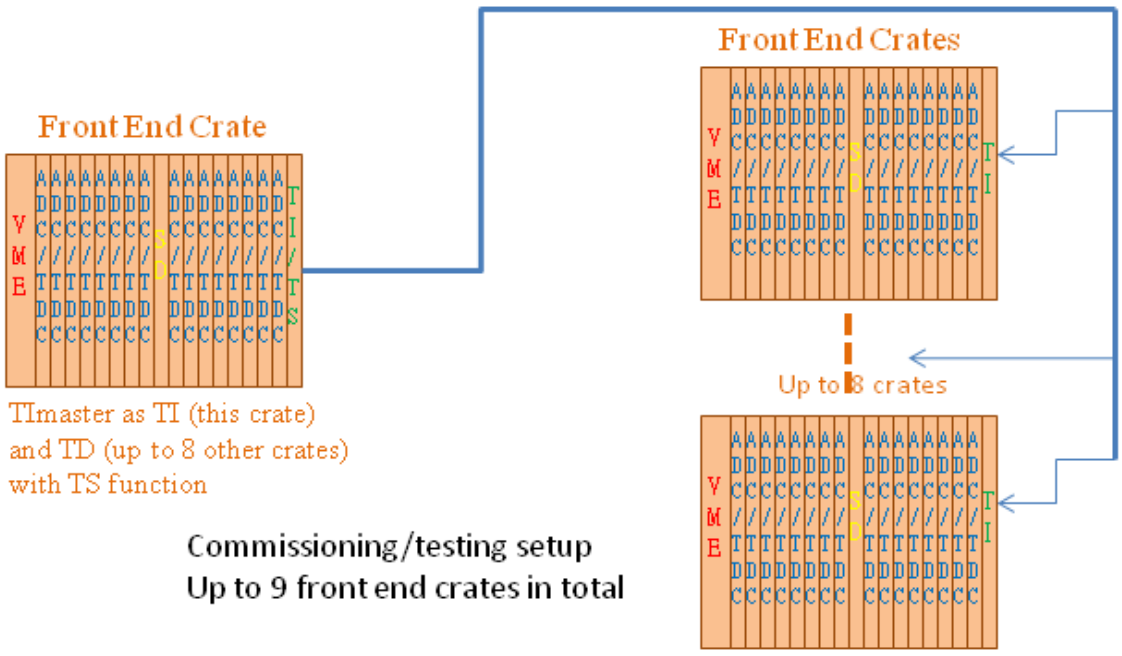


Figure 2b



The TI FPGA firmware is compatible with the TImaster mode and the standard TI mode. The firmware senses the TI clock setting. If the TI clock source is set to onboard oscillator or front panel ECL input, the TI is in TM mode, or else, the TI is in standard mode. For the TM mode, the TRG/SYNC used in the TM is similar to the TRG/SYNC sent in the optical transceiver. The TRG/SYN is looped back within the FPGA and decoded the same way as a standard TI board. Some registers are valid on the TM only, as these registers are specific to the TS function. The TM can be used by itself in the setup. It can also drive another up to eight TIs if the setup needs be expanded.

When the TI is in standard TI mode, it can have two HFBR-7924 modules stuffed. In this case, one can receive trigger from system TS, while the other can receive trigger from a sub-system TS. One TID can be located in any payload slots in a front-end crate, and configured as a subsystem TS. This configuration requires an extra optical transceiver on the TI module, and an extra TID board be configured as a subsystem TS with fiber outputs. Each optical transceiver module costs about $400. For a subsystem with eight crates, the extra cost is about $10K (extra optic fiber included). The benefit is that the subsystem can have independent control without affecting the other subsystem. That is a lot of flexibility: independent subsystem control, independent subsystem calibration etc. This is called a luxury option. Refer to figure 3a for the setup. Figure 3b shows the crate level diagram

Figure 3a:

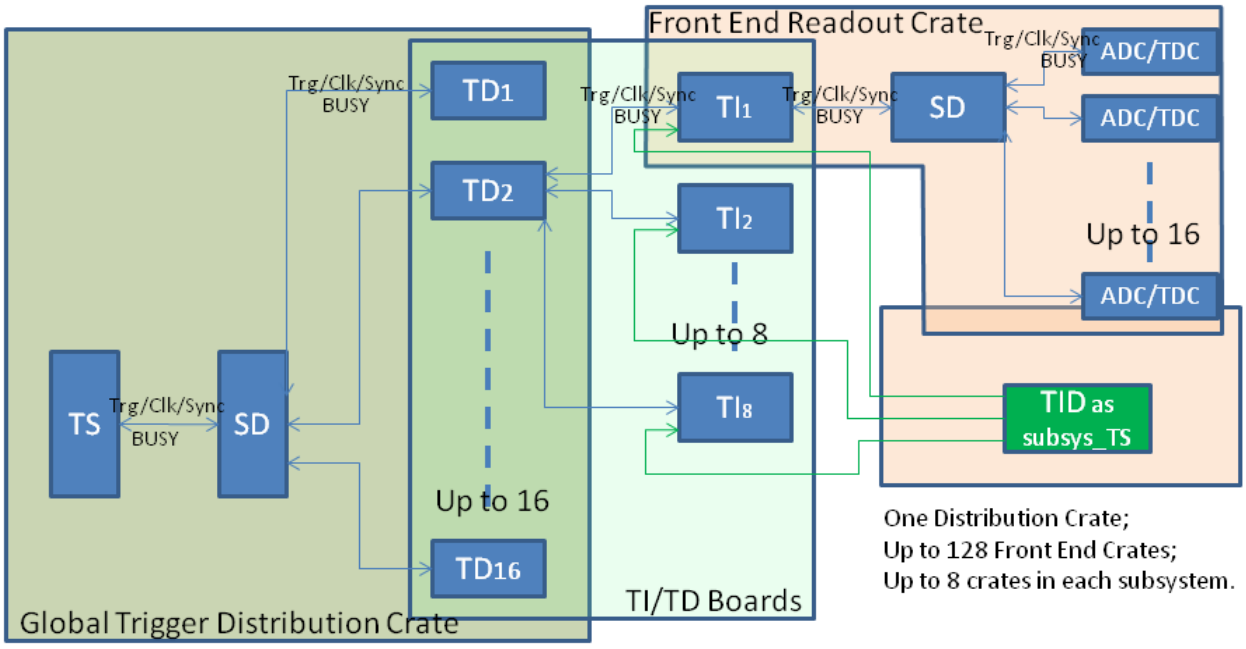
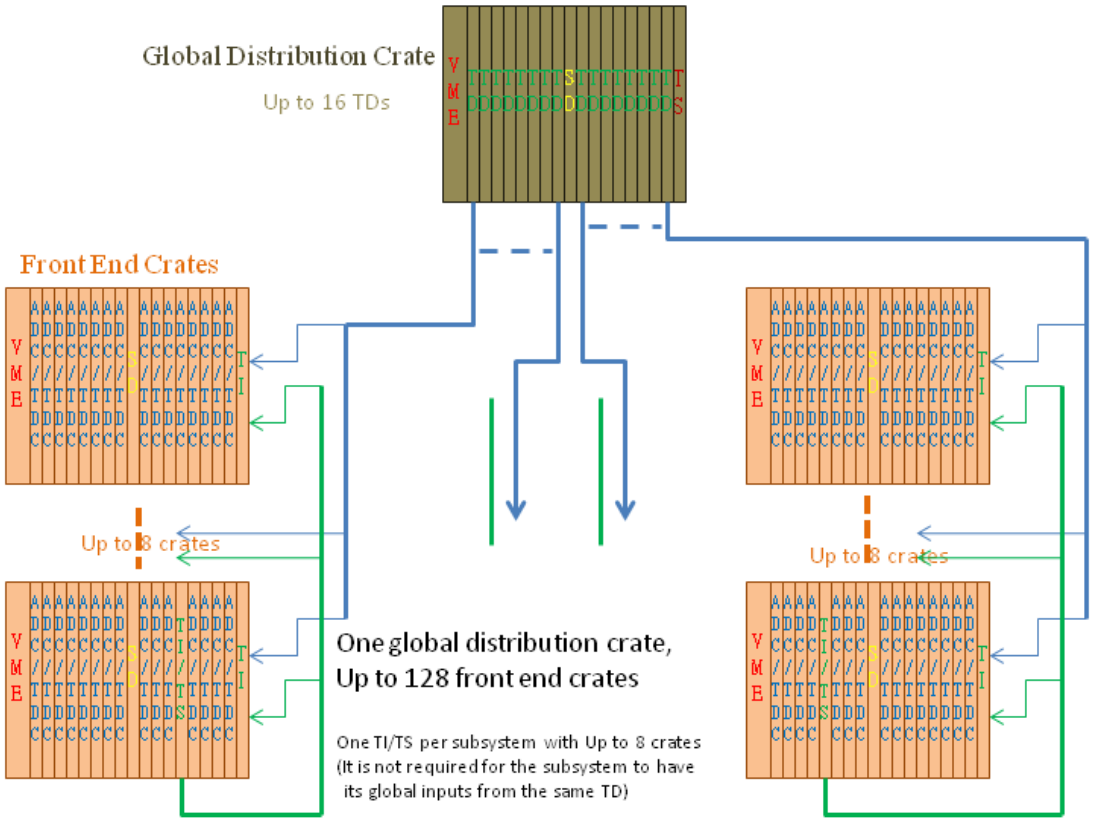


Figure 3b:



There is another direct connection between the TI and switch slot A board (CTP or GTP) and switch slot B board (SD). This link can be used to transfer data between the TI board and the switch slot boards. It is natural to implement the link at 250 Mbps using the system clock, or 500 Mbps with DDR technique. If the Data acquisition function is built in the SD, the SD can collect and assemble events at the trigger by trigger basis, which provides a redundant data readout path. The SD/CTP can send their data to the TI, and the TI combines the data with its own data event by event. The data can be readout through VME (there is no direct VME access to the switch slot A and switch slot B)

With a mezzanine board, the TI is backward compatible with Trigger Supervisor Rev2 module. The TI with the mezzanine card will behave the same way as TI_Rev2 (produced in the year of 2001) board with added functionality.

For non-VXS crate (or non-VXS data acquisition modules), the TI will send trigger/clock/Sync to Row-C on VME P2 connector. With a fan out board, the trigger/clock/SYNC are distributed to the frontend data acquisition modules (CAEN VX1290 TDC for example), and the BUSY from these modules are summed in the fan out module, and sent back to the TI.

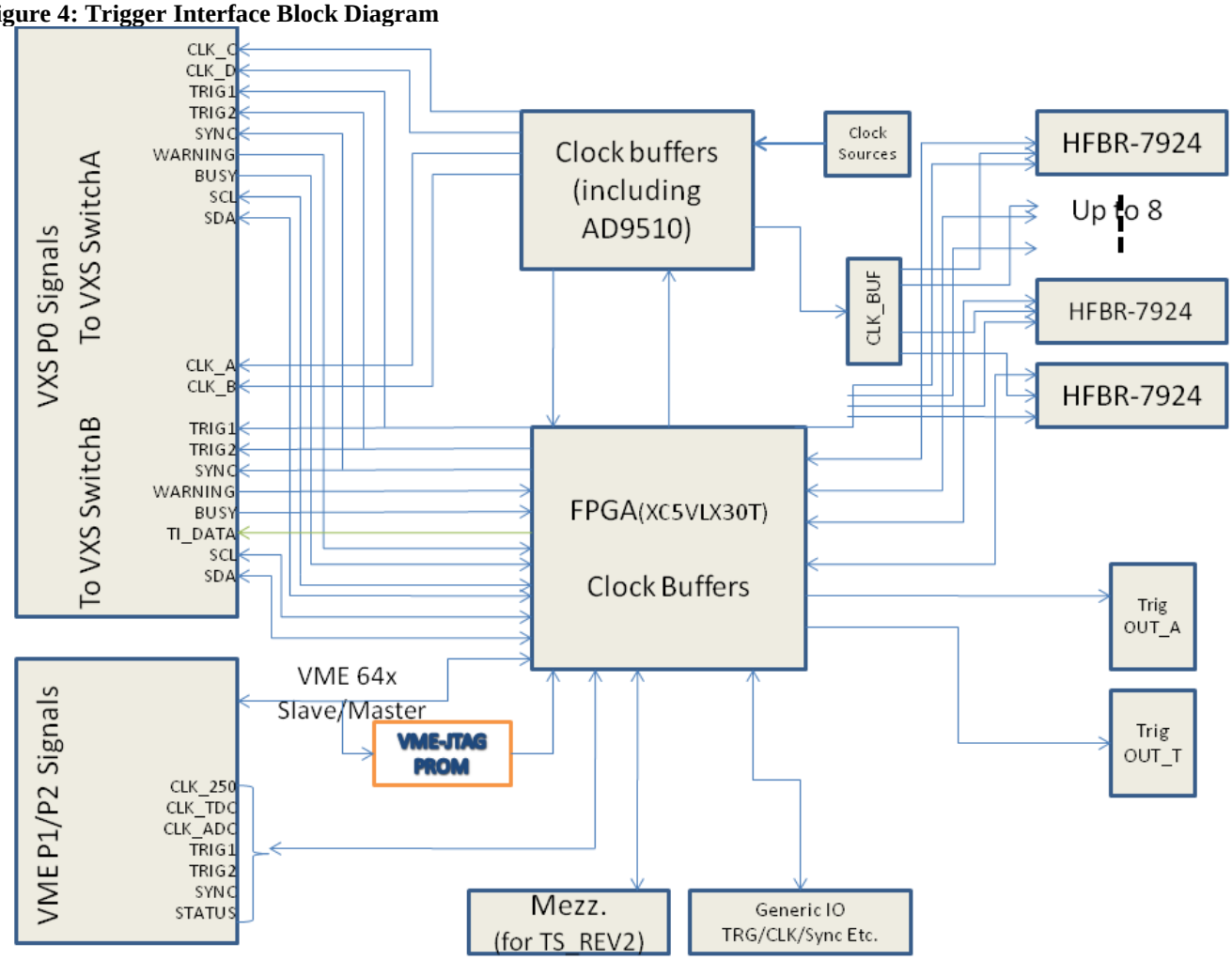
3 Functional Descriptions

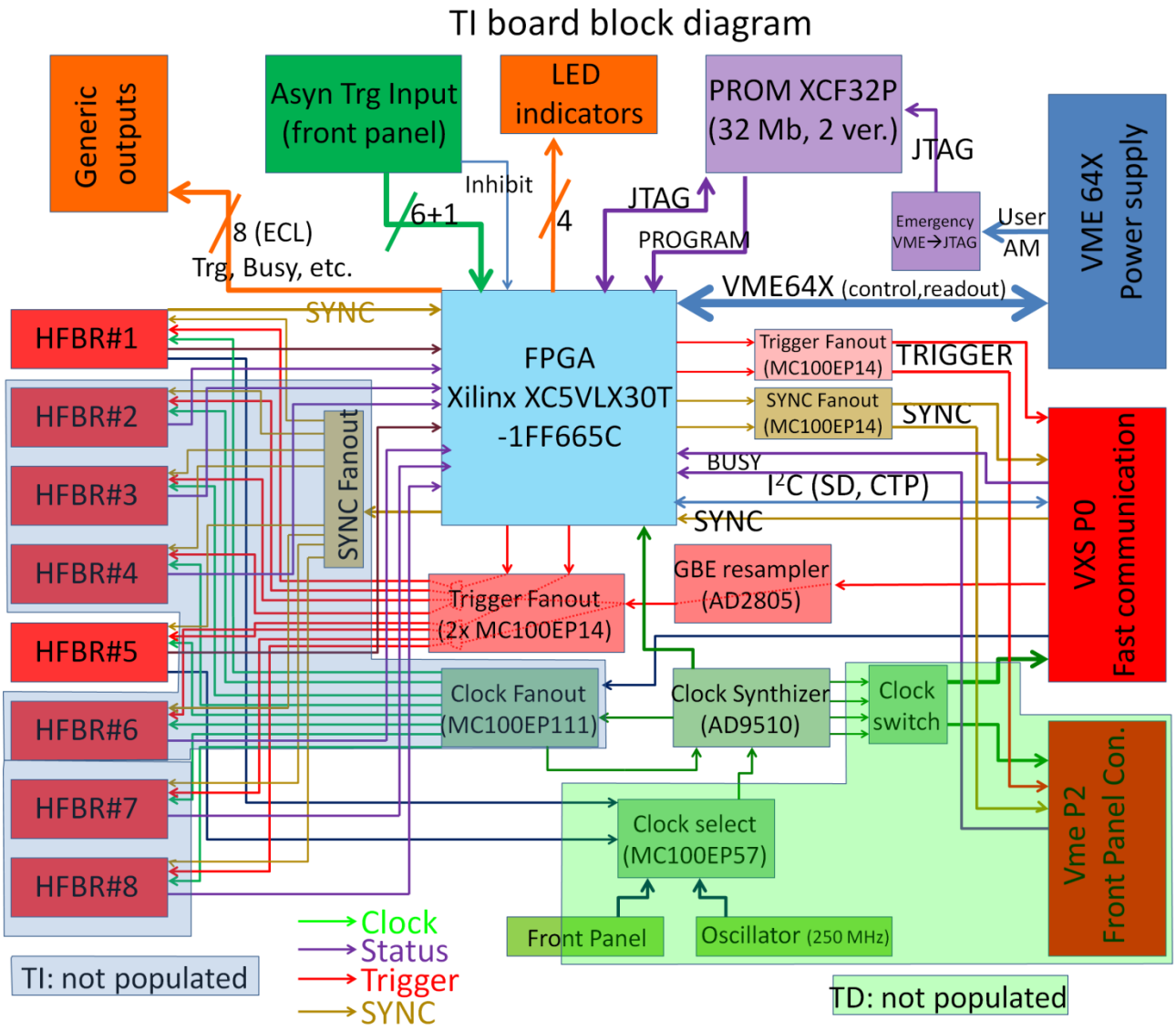
3.1 General description

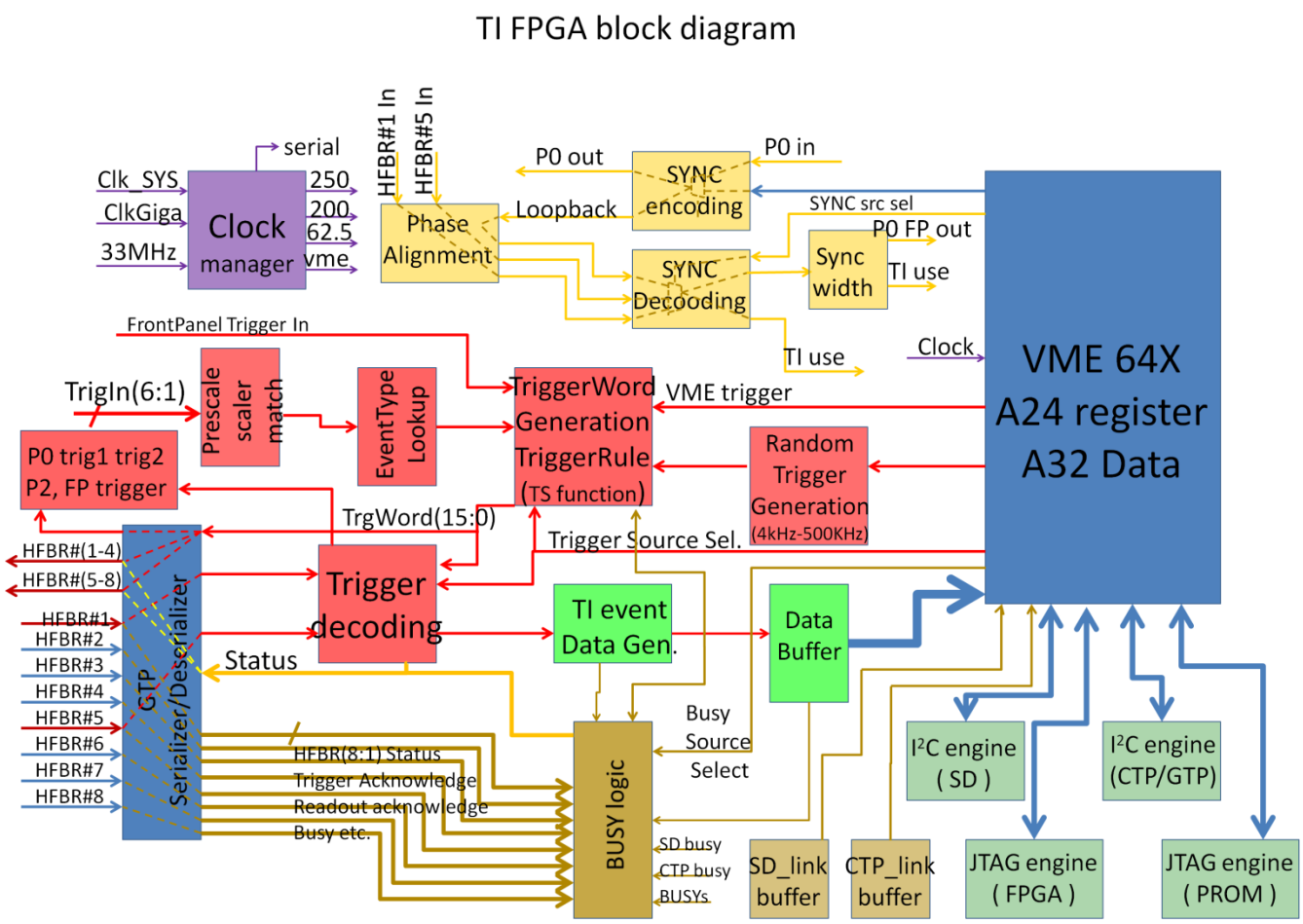
Figure 4 shows the block diagram of the TI module, indicating the major components used in the design. The HFBR-7924 is the multi-channel (4 Rx, 4 Tx) fiber link that the TI fans out/receives a low-jitter (<3ps RMS) 250MHz global pipeline clock, serialized 16bit trigger words, and a sync signal used in producing a synchronized trigger. The AD9510 is the main clock driver and gets synchronized lower frequency clocks. The Xilinx

XC5VLX30T is used to encode/decode the trigger words at 16ns, to interface with the VME, to control the working mode etc. The P0 is compatible with the VXS payload slots, which matches with GTP, CTP, SD positioned in switch slots.

Figure 4: Trigger Interface Block Diagram




TI board block diagram
Generic outputs
Asyn Trg Input (front panel)
LED indicators
PROM XCF32P (32 Mb, 2 ver.)
JTAG
VME 64X Power supply
Inhibit
6+1
4
JTAG
PROGRAM
Emergency VME→JTAG
User AM
8 (ECL) Trg, Busy, etc.
VME64X (control,readout)
SYNC
HFBR#1
HFBR#2
HFBR#3
HFBR#4
HFBR#5
HFBR#6
HFBR#7
HFBR#8
SYNC Fanout
FPGA Xilinx XC5VLX30T -1FF665C
Trigger Fanout (MC100EP14)
TRIGGER
SYNC Fanout (MC100EP14)
SYNC
BUSY
I²C (SD, CTP)
SYNC
VXS P0 Fast communication
GBE resampler (AD2805)
Trigger Fanout (2x MC100EP14)
Clock Fanout (MC100EP111)
Clock Synthizer (AD9510)
Clock switch
Clock select (MC100EP57)
Vme P2 Front Panel Con.
Front Panel
Oscillator (250 MHz)
Clock
Status
Trigger
SYNC
TI: not populated
TD: not populated



3.2 Fiber links

The HFBR-7924 is the multi-channel (4 Rx, 4 Tx) fiber optic link for the TI. For some TImaster boards, all the eight HFBR-7924 transceivers will be installed, so each can support another eight front end data acquisition crates. For the standard TI in the front end crates and global trigger crate, One (maybe two) HFBR-7924 transceiver will be installed, to receive the trigger/clock/sync from central trigger (and subsystem trigger).

The HFBR_7924 is chosen over the HFBR-7934, because the HFBR-7924 is about $100 cheaper per piece, and there is no visible performance degradation comparing with HFBR-7934. [GU, 2010]

The first pair (Tx/Rx) is used to transfer trigger words from TD to TI, and status from TI to TD. The second pair is used to transmit the 250MHz clock from TD to TI. The third pair is used to transmit the SYNC from TD to TI. The TI to TD links on second pair and third pair are not used.

The fourth pair (Tx/Rx) is looped back on the TD for fiber length (latency) measurement. The fiber numbers #2, #3, #4, #6, #7 and #8 on TImaster are looped back by a short trace on the PCB between the HFBR Tx and Rx pads. The fiber#1 and #5 are controlled by the FPGA. For TImaster, the FPGA loops back the signals; for standard TI, the FPGA generates a pulse and receives the loopback pulse. By measuring the delay, the fiber delay is measured.

3.3: Clock Distribution

One of the TI's major functions is the pipeline clock distribution. There are four possible sources for the 250MHz clock: 'onboard oscillator', 'external clock input from twisted pair cable', 'optical fiber input from central trigger HFBR#1' and 'optical fiber input from subsystem trigger HFBR#2'. The five clock sources will be multiplexed. There will be only one 250MHz clock running on the TI. The clock is multiplexed by a MC100EP57 chip and go to the AD9510 CLK1 input, and the output of the AD9510 drives all the outputs. In TImaster mode, The clock is fanned out by the MC100LVEP111 2:1:10 clock driver to the optic transceivers.

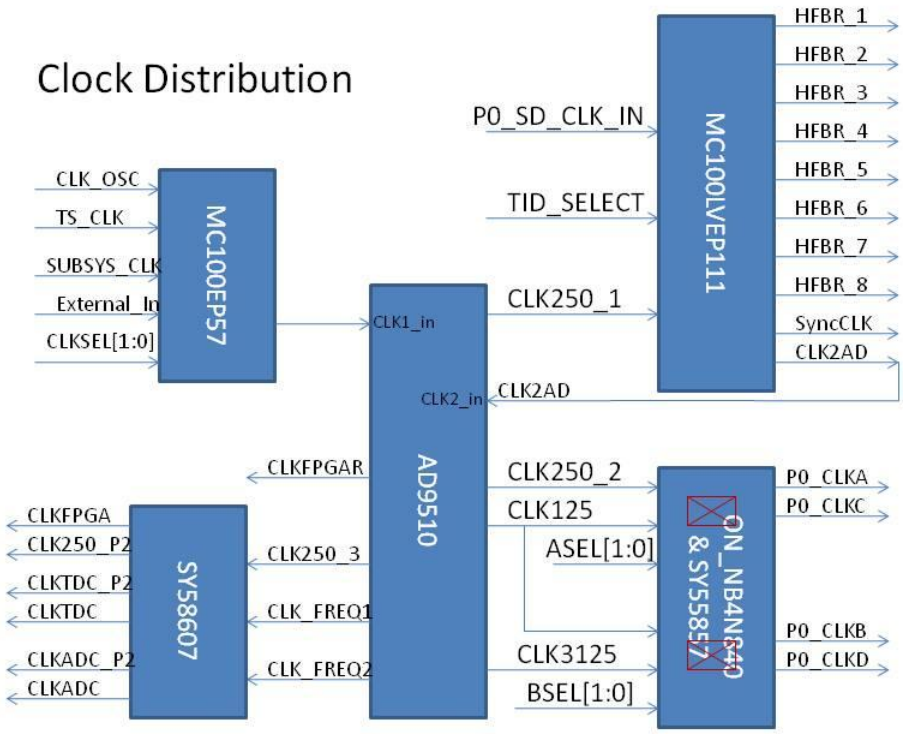
Three clocks (with frequencies of 250 MHz, 125 MHz, and 31.25 MHz) are distributed to the P0 backplane. One On-Semiconductors' NB4N840M and two NB6L72 are used to switch the clocks, so that, the switch slot #A and switch slot #B can get two clocks. Each clock could be any of the three frequencies. The NB6L72 is also used as a level shifter from CML to LVPECL.

The clock is also distributed to the front panel connectors via ECL on twisted pair cables and VME P2 backplane user defined pins for VME ADC or TDC modules, which are NOT VXS compatible.

The CAEN V1290 TDC will get a synchronized 41.67MHz clock through TID P2 connector via a fan out board in the crate, instead of the nominal 40MHz onboard oscillator frequency, because there will be too much effort involved to generate a system wide synchronized 40MHz clock, and the V1290 can be calibrated to accept the 41.67 MHz clock.

An eight-bit on board switch will be used to select the clock sources except for the AD9510, which will be set by the switch, but the setting can be over written by the FPGA firmware (and software).

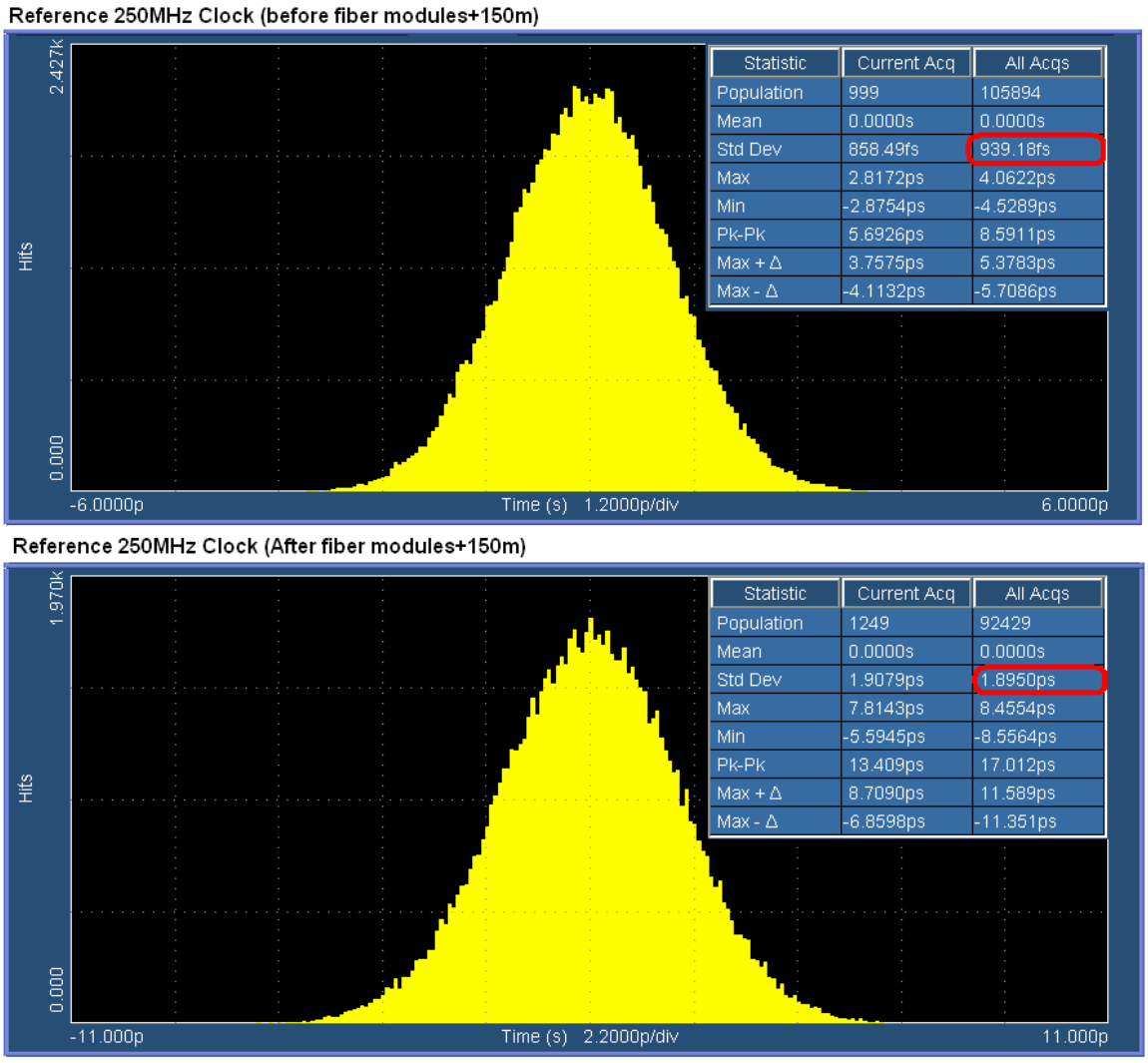
Figure 5 shows the TID clock distribution diagram:



The clock is distributed in (LVP)ECL levels to keep the low jitter and low skew (faster propagation). The LVDS clock is used to drive the FPGA for easy termination.

The global 250MHz clock signal received over the fiber runs the L1 trigger pipeline electronics and nearly all of the front-end modules. Several front-end modules require this clock to have low-jitter and so the clock signal is buffered with components that contribute low-jitter, including the fiber driver and receiver. Figure 3c shows a measurement of the jitter contribution from the fiber driver/receiver pair, including a small increase in clock jitter (roughly 1.6ps additive jitter from the fiber driver/receiver with 150m of fiber between them) by GU et al. [(GU, 2010)]. Careful component selection, signaling, and layout techniques are employed to minimize overall clock jitter. The SD board can further clean up the jitter by its PLL chips.

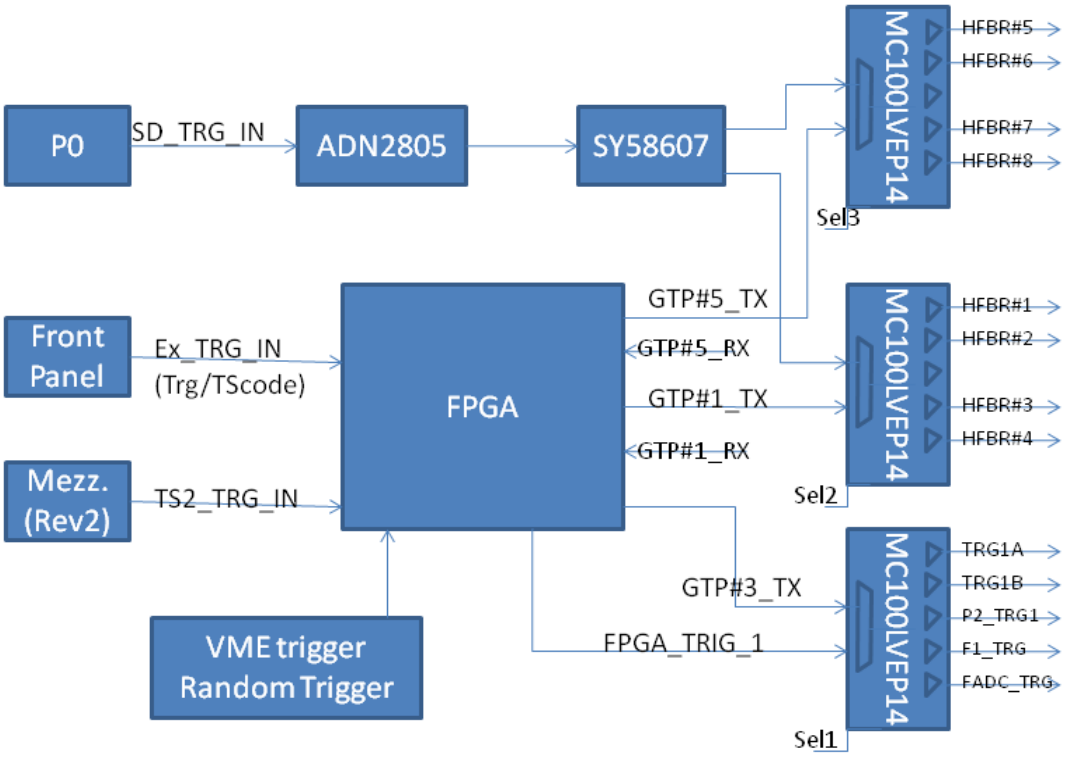
Figure 6: Global Clock (250 MHz) Jitter



3.4 Trigger distribution:

Figure 7 shows the trigger distribution on TI. The TI receives the trigger signal by the optical fiber and decoded by the FPGA. The trigger is sent to the fan out buffer then to the P0 backplane and other connectors. When the TI is in TImaster mode, the TM takes the trigger from the front panel input and send to the SD in gigabit serial mode (encoded) or pulse mode, and it also sent to the fiber in encoded format, though the HFBR#1, #2, #3 and #4 are identical, and HFBR#5, #6, #7 and #8 are identical. (Surely, these two groups can be the same too). The independent choices of the trigger enable the versatile functions of the TI.

Figure 7, Trigger distribution



3.5: Encoded Trigger Word

A 1.25Gbps serial link operating over the fiber is used for distributing a 16bit trigger word every 16ns. There is also a link going in the opposite direction, allowing status words to be sent back to the trigger distribution crate. The 16bit trigger words are decoded as follows (TS->TD->TI flow):

Trigger strobe word – generated by the TS in response to the acceptance of a level 1 trigger. Upon receipt, the TI drives prompt trigger signals to the front-end modules. The TS transmits these with fixed latency relative to the accepted trigger. This word is distributed every 16ns, so the trigger is distributed every 16ns. The timing information is added in the trigger word to distinguish which quadrant of the 16 ns period the trigger is generated to be fully compatible with the 4ns pipeline design architecture. The TI can distribute trigger signal in 4ns precision. This could potentially reduce the FADC readout window width, and reduce the event size.

Trigger content word – additional information about the trigger for use by the ROCs. It is queued in a FIFO and sent in any frame not used by a trigger strobe word. The TI matches the trigger strobe and trigger content words by the order of their reception.

Control Word – request status, or other command (VME trigger for example). They can be queued in a FIFO and sent in any frame not used by a trigger strobe word or trigger content word.

Master Time Word – to fully use the trigger link, bits [13:2] of the TS time is transmitted whenever no other word types are available. By continuously receiving bits [13:2] of the TS time, each TID can promptly detect if its frontend crate has lost global synchronization (i.e. compare the global time with its own time). Otherwise, the loss of synchronization could only be detected at the event building stage. The continuous transmission of 'known' (i.e. predictable) data also allows one to monitor the integrity of the link.

This table shows the format of the trigger word.

Bit13	Bit12	Word Type	Meaning of Bit[11:0]

0	0	Time	Lower 12 bits of TS time
0	1	Control	Control or Command
1	0	Trigger Strobe	Trigger type/Trigger quadrant
1	1	Trigger Content	Additional Trigger data

Bits [15,14] are used on TS to further distinguish the trigger types and TS partitioning.

The following defines the data format for the opposite direction of the link (TI->TD->TS flow):

Bit [15] parity bit;
Bit [14:12] 000 right now;
Bit [11] TI (including the front end crate) BUSY: '1' = busy, '0' = not busy;
Bit [10] Trigger_1 acknowledge;
Bit [9] Trigger_2 acknowledge;
Bit [8] one block of triggers received;
Bit [7] ROC readout acknowledge (one block of trigger is readout and acknowledge by ROC);
Bit [6:0] status.

3.6: Fixed Latency SYNC

The SYNC signal is a 250Mbps serial line operating in synchronous mode. This serial link allows a 4bit command to be sent at chosen 4ns points in time. SYNC is synchronized to a slower clock (62.5 MHz) derived from the 250 MHz master clock and is sampled every 4 ns. The line is considered to be idle when more than 4 samples in a row are read '1'. A command is sent between idle times by sending first a '0' followed by the 4bits that comprise the command, LSB first. After the command has been sent, a final '1' is sent so that the line will return to the IDLE state. The encoding portion of this serial protocol is performed on the TS (or the TS function of the TImaster). Since the TD distributes this serial line over the fiber module, additional encoding (Manchester) is performed to balance the 1's and 0's of the line and to keep the maximum run length of the signal below the requirements of the fiber module. The TID decodes the SYNC signal (Manchester and command). Careful design in minimizing SYNC to the distributed master CLK250 skew guarantees a fixed latency link.

The SYNC is fiber delay adjusted on each TI. The fiber latency is measured using the fourth pair of the fiber. The SYNC is delayed so that all the TI modules will execute the SYNC command at exactly the same time (within the skew of the global 250MHz clock distribution).

The SYNC link is used in conjunction with a synchronous FIFO to enforce a fixed latency on the serial trigger link. The TD uses LVPECL buffers to fan out the trigger signal and the Sync signal, which is encoded (Manchester encoding) in the FPGA, to the HFBR_7924 transceivers. In the TI, the trigger word is clocked into a FIFO using the FPGA built in MGT transceivers and clocked out of the FIFO using a 62.5MHz clock derived from (and in phase with) the 250 MHz system clock. At startup, the FIFO is reset (0 words) and reading the FIFO is disabled. No words are written into the FIFO since the TS is not yet transmitting data words on the trigger link (i.e. received data valid signal is not asserted). Acceptance of triggers by the TS is also disabled. The TS starts transmission (time words) on the trigger link, and after a fixed number of 62.5MHz clock cycles issues a trigger start command on the SYNC line. In response to the trigger start command, the TI enables continuous readout of the FIFO. There must always be a non-zero number of words in the FIFO to maintain a fixed latency link. This will be true if the number of words pre-filled into the FIFO x 16 ns is greater than the latency uncertainty of the link. In the case of the MGT, several words (e.g. 3 or 4) are enough when the latency is set to minimum, as the elastic buffer is not necessary as all the clocks are the same or derived from the same 250MHz clock (no clock frequency difference). The TS must always be transmitting valid data to maintain the fixed latency of the link. This is illustrated in figure 8:

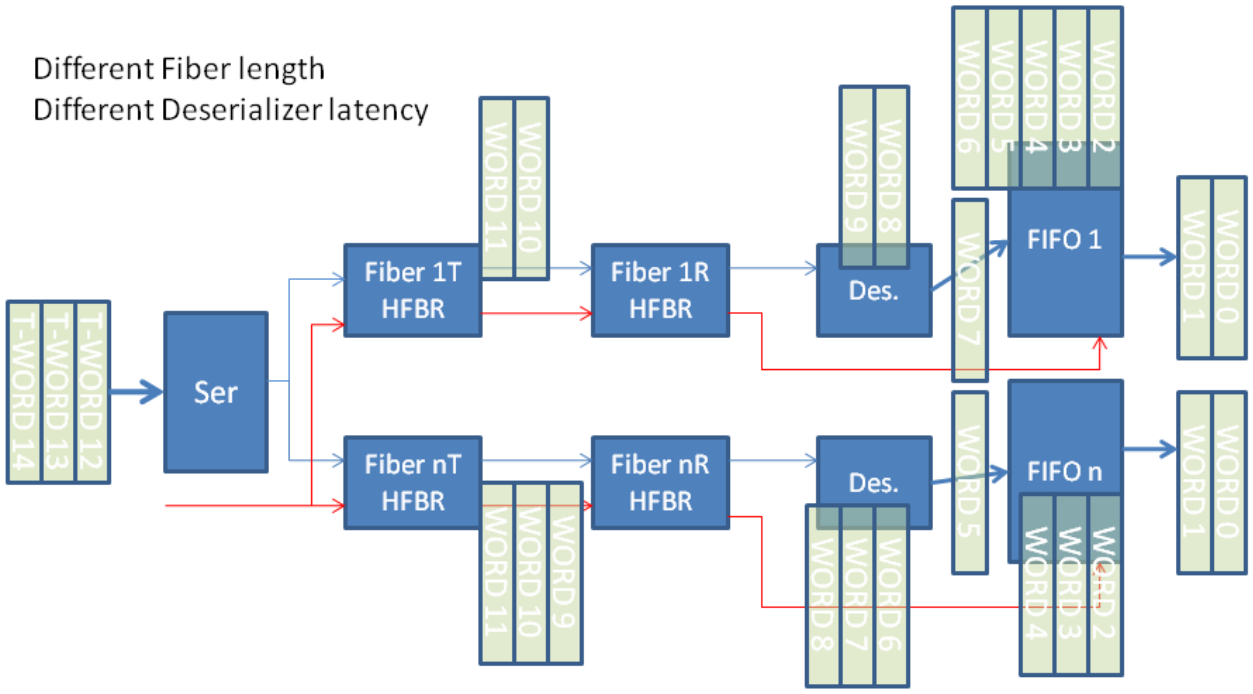
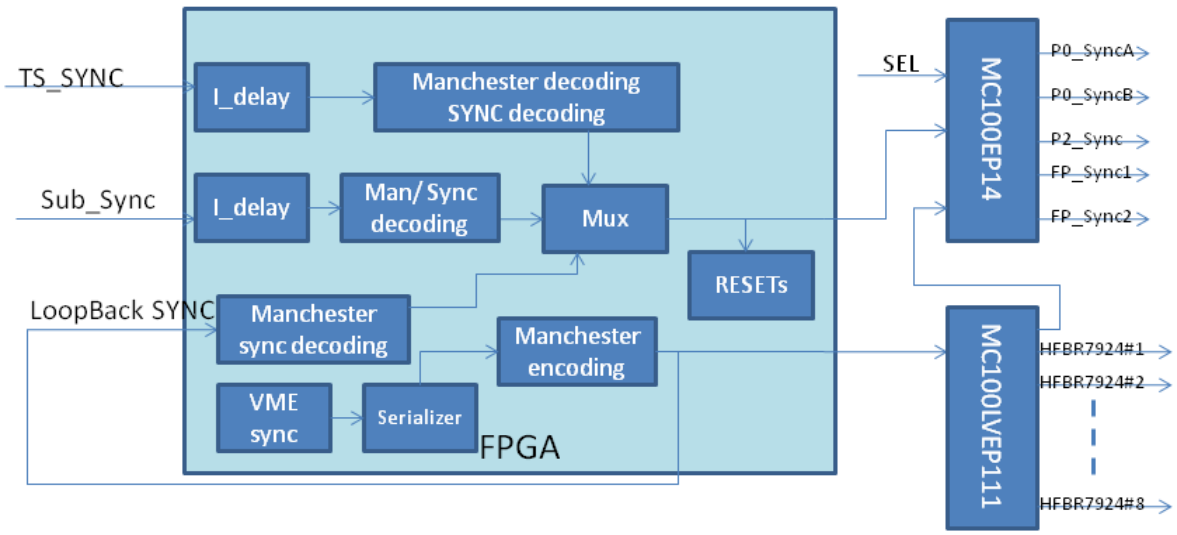


Figure 8: Illustration of the Trigger synchronization process

The SYNC link is also useful in ensuring that the lower frequency clocks derived in the TI from the distributed system clock (CLK250) have the same phase across all TI modules in the front-end data acquisition system. At startup, the TS issues a SYNC command CLKRESET. This resets the clock distribution chip (AD9510) in each TI on the same CLK250 edge, assuring that the lower frequency clocks (125MHz, 62.5MHz, 41.67MHz and 31.25MHz) are in phase across the entire system. This command is sent before the TI sync command. The delay between them is determined by the maximum MGT reset recovery time, as the MGT clock is changed (AD9510 clock reset) during clock reset. The time is several milliseconds.

Figure 9 shows the block diagram of the SYNC distribution on the TI board:



3.7 VME interface

The TI board is a VXS payload slot board. It is compatible with VME64x backplane. Normally, it is a VME slave board, with interrupt capability.

The TI can also be a master VME board. It supports single level bus request (BR3, level 3) only, as we do not expect many boards to be a VME master in the crate.

For simplicity, three kinds of VME address modifier codes are implemented. (1), User defined address modifier. (0x19,0x1A, 0x1C and 0x1D) This is similar to the A24 address modifier. It is used to load the PROM by the emergency logic. (2), Standard A24 address modifier. This is used to readout the registers on the FPGA, slow controls of the TI peripherals, and to request data from other boards in the crate when in master mode. (3), A32 BLT data transfer. This is used to transfer data to the ROC (Read Out Controller). This is implemented the same way as other ADC/TDC board, so the ROC needs only one read to get all the front end boards' data out for higher efficiency.

3.8: The Xilinx PROM programming.

The Xilinx XCF32P PROM is used to program the FPGA. It can save two different versions of the FPGA (XC5VLX30T) firmware when used in non-compression mode. It can save four different versions of the firmware when bit stream compression is used, in which case, only the slave serial and slave SelectMAP modes are supported. The PROM is programmed using VME with emergency logic decoding. It can be addressed in the VME64x crates by its geographical address. If it is in the crate without geographical address, only one TI in the crate should be addressed as geographical slot#0. To avoid conflict with other VME addressing, the user-defined address modifiers are used for the PROM loading. The emergency logic supports A24 user defined address modifier codes: 0x19, 0x1A, 0x1D and 0x1E (Similar to 0x39, 0x3A, 0x3D and 0x3E). Out of the data, bit[1] is used for TDI, bit[0] is used for TMS, and all the other bits are unused. The emergency loading is tested. With M6100 controller, the 32 Mbit PROM (XCF32P) can be loaded in less than five minutes. The emergency loading provides VME remote firmware re-loading and broadcast firmware loading even if the FPGA is not working. One 33 MHz on-board oscillator is used to program the FPGA in slave mode, and used by the FPGA for slow control, for example, the VME to AD9510 serial control engine. The PROM is in master mode with external clock. This is set when producing the SVF download file.

The PROM can also be programmed by the on-board JTAG connector and VME-JTAG engine (after the FPGA is programmed and working) in the FPGA. The JTAG engine in the FPGA provides VME remote firmware loading when the FPGA is working with more efficient VME data transfer (32 bits versus 1 bit).

3.9: Status passing

The TI can merge the status together and pass on to upper level. Specifically, the TI can merge the status from the CTP and SD via P0 backplane and pass on to TD in the global trigger/clock distribution crate via optical links. Right now, only the BUSY is defined as status. We have the capability to add a less severe state, WARNING, to the status.

The TI in the front end crate can send its timing information back to the TD in the trigger distribution crate. This information can be used to check the system synchronization status. Here is how this will work.

On the start of the run, a global sync command will reset all the counters synchronously. Each TI will have its own clock counter, that count how many clock cycles since the sync reset. As the trigger is synchronized on all the TIs, all the TI should receive the same trigger at the same clock cycle. The TI in the front end crate will send the clock counter, recorded when it receives the trigger, to the TD in the distribution crate along with the trigger acknowledge. This signal may be received asynchronously as a status word (ref to section 3.5), but all the eight words should match on the TD. The TD check the difference between the trigger sent and the trigger acknowledge received. The TD also checks the trigger acknowledge timing. If the TD received un-matching numbers from front-crate, it is most likely a trigger loss if the timing difference is large; it is most likely a clock loss if the difference is small. In this way, the trigger synchronization can be checked at the hardware level.

3.10: Serial data communication with SD

The TI can send data to the SD via a 250Mbps link, (it is possible to increase it to 500 Mbps using DDR techniques). This can be implemented using the Xilinx SelectIO standard differential IO pin pair. In this case, the SD can be implemented as a data concentrator card to collect data from the VXS crate (the payload modules include FADC, FTDC, TI, etc.). The TI will send data to SD on every trigger (event). This is another data readout path in addition to the standard VME readout. The maximum data rate is 50 MB/sec per slot. The full crate can reach up to 900 MB/sec assuming all 18 payload slots are used. The data from SD is event based, and there is no need to re-format the data as needed by the VME readout (block readout is used for high efficient usage of the VME bus data transfer).

The SD can also send data to TI using this link, though there are not much useful per event data from SD anyway. The direction of the data link depends on the firmware (TI and SD) implementation.

3.11: legacy compatibility

A mezzanine board is used to interface with the TS_rev2 module directly for backward compatibility, which may still be used in the experiment halls. The Mezzanine board has the same connector as the TI_rev2 board (matching with Trigger Supervisor rev2). With the mezzanine board plugged in, the TI will behave like a TI_rev2 board (produced in 2001) to interface with TS_rev2 board.

3.12 Other functions

The TI has a generic IO 34 pins connector, which can accept one external trigger input, and six trigger input codes. It can also accept external clocks and trigger inhibit. Using these, some of the Trigger Supervisor functions can be implemented in the TI. The TI can serve as a subsystem trigger supervisor board. A nine crates setup can be implemented by TIs for (sub)system commissioning and subsystem test setups.

3.13: Readout Synchronization

In addition to the event number and trigger time stamp, the readout can be forced to get synchronized by synchronization events (SyncEvent). There are two ways to generate the SyncEvent.

First, the SyncEvent can be generated periodically by TS (or TImaster). The last event of the every N blocks is generated as the SyncEvent. (for now, the block level, or number of event per block, is up to 255) The N is any value between 1 and 65535, which is set and enabled by A24 register offset 0xD4. When the periodic SyncEvent is marked, the original event type is kept.

Second, the SyncEvent can be forced by VME command to the TS (or TImaster). This event may be any event in the trigger block. It is an added event with event type “00000000”. The forced SyncEvent can be generated by VME A24 register offset 0x100, bit#20. It is also possible that the SyncEvent is generated by a front panel signal input.

The TS (or TImaster) will assert a short BUSY (3us) after generating the SyncEvent, and stop further triggers. After receiving the SyncEvent, the TI will generate BUSY, and set the SyncEvent marker in the ROC polling register A24 offset 0x34. The BUSY of TI will propagate back to the TS through fibers and P0 backplane. The latency of this should be less than 3us, so that it will overlap with the short BUSY on TS. After the front end data is cleared, and the Readout acknowledge will clear the BUSY on the TI. In pipeline readout mode, If there are more than one trigger blocks to be read out, the very last acknowledgement clears the SyncEvent BUSY on the TI. After all the TI boards clear their BUSY, the TS will distribute trigger again. Depending on the data acquisition mode and the amount of data backed up on the frontend, this process may take tens of microseconds to many milliseconds.

Upon SyncEvent, the trigger distribution will be paused. Users can change the DAQ settings during this time. If no reset in this time period, the event number and trigger time be continued.

4. Specification Sheet

4.1 Mechanical

- Single width VITA 41 Payload Module. It will be positioned in PP18 in front-end data acquisition crate and global trigger crate; it can also be plugged into any slots in standard VME crates without VXS. In system commissioning, it can be in PP18 and support up to 9 crates with some TS functions. In luxury setup (optional), it can be in any payload slots (except PP18) of the subsystem crates, and serve as a subsystem Trigger Supervisor, which can group up to 8 crates together as a subsystem.

4.2 High speed serial P0 and P2 inputs:

- BUSY LVDS signals on P0;
- BUSY ECL signals on P2;
- I^2C to VXS Switch A & B;

4.3 High speed serial P0 and P2 outputs:

- Any two of these clocks (250MHz, 125MHz, and 31.25MHz) to Switch slot #A and Switch slot #B.
- Trig 1 LVPECL Trigger Signal
- Trig 2 LVPECL Trigger Signal
- Sync LVPECL Trigger Signal
- 250/500 Mbps data (LVDS) to/from SD at per event basis

4.4 Front panel inputs and outputs:

- 250MHz ECL Clock Input & Output
- Trig 1 ECL Trigger Input & Output
- Trig 2 ECL Trigger Input & Output
- Sync ECL Trigger Input & Output
- Busy ECL Input & Output
- Up to eight HFBR-7924 transceivers for TImaster; up to two HFBR-7924 transceivers for standard TI in front-end data acquisition crate.

4.5 Fiber channel signals:

- SYNC Fixed Latency Link
  - 250Mbps Serial Communication
  - Manchester Encoded
  - SYNC to CLK skew variation adjusted at FPGA receiver.
- TRIGLINKTX/TRIGLINKRX
  - 1.25Gbps Trigger Word Line
  - Provides 16bit parallel data every 16ns
  - A BUSY status word in the opposite direction.
- CLK
  - 250MHz Clock <3ps RMS Jitter

4.6 LED Indicators: Front Panel:

- Bit 1 (close to the PCB): FPGA programmed and the clock (DCM locked) is ready;
- Bit 2: VME DTACK, VME activity;
- Bit 3: Trigger_1 is sent out;
- Bit 4: HFBR MGT Rx error;

On board:

- Power OK near each regulator or DC-DC converter (LED is OFF when the power is OK);
- FPGA program DONE (LED is OFF when programmed);
- Fiber optical transmitter FAULT and receiver SIGNAL_DETECTED near each HFBR-7924 module.

4.7 Programming:

- VME to JTAG A24D32 with user defined AM (Address Modifier) for remote loading with redundant On board JTAG connector;
- Custom VME to JTAG engine implemented in the FPGA using A24D32 for firmware loading;
- Up to four revisions of the firmware can be stored in the PROM simultaneously.

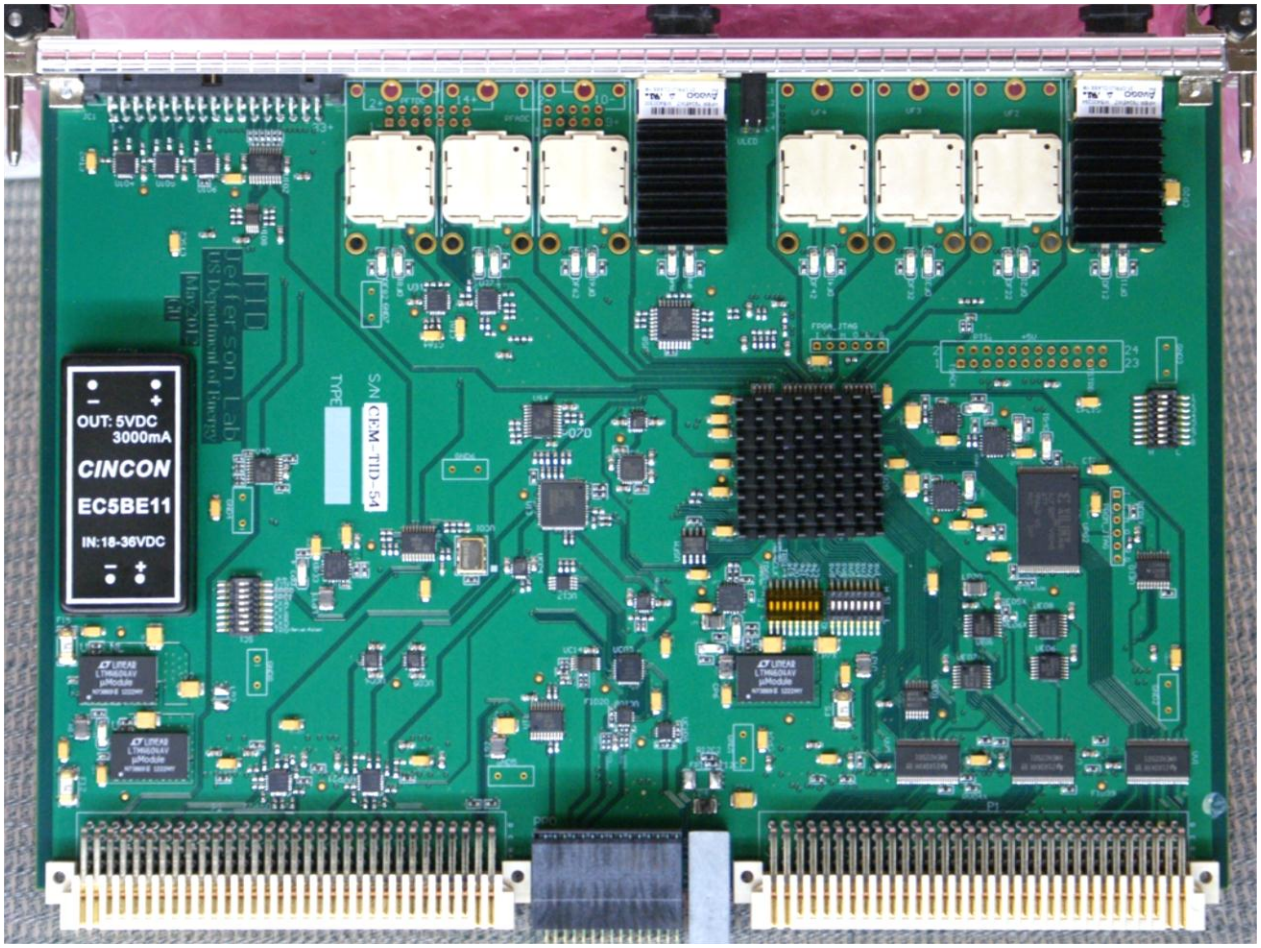
4.8 Power requirements:

- +5v @ 4 Amps; -12V @ 0.25 Amp; +12V @0.25 Amp (From Backplane)
- Optional DC-DC converters for +3.3V, and Local regulators for other required voltages: +1.0V, +1.2V, +1.8V, +2.5V, +3.3V, and -5V.

4.9 Environment:

- Forced air cooling: Weiner standard VME64x/VXS
- Commercial grade components (0-75 Celsius)

Figure 10 shows a typical TI board :



5 TI operation procedures:

The TI needs be properly set, and plugged into the proper crate and slot. Damage may happen to the TI, the crate, or other PCBs in the crate if the right procedure is not followed.

5.1 TI Power supply:

The TI can use +3.3V directly from VME64x crate. It can also generate its own +3.3V supply by a DC-DC converter. Another dedicated +3.3V DC-DC converter can be used to power the optical transceivers (HFBR-7924). The HFBR_7924 can also be powered by the main +3.3V supply for the board. Proper settings are needed to avoid damage to the board or backplane.

If the dedicated +3.3V DC-DC converter is used to power the HFBR-7924:

(1). Make sure that the DC-DC converter LTM4604, UP01, is stuffed.

(2). Inductor, LP3 is removed.

If the TI main +3.3V power is used to power the HFBR-7924:

(1). Make sure that UP1_NL is NOT stuffed,

(2). Inductor LP3 is stuffed.

If the VME64x crate +3.3V power is used for the TI:

(1). The fuse, FP1 is stuffed;

(2). The DC-DC converter UP1 is removed.

If the VME64x crate +3.3V power is not used for the TI:

(1). The fuse, FP1 is removed;

(2). The UP1 is stuffed.

5.2 Hardware setting (Switch etc.):

The TI drives signals to the P0 connector. This is set by three pairs of resistors or capacitors. If the 0 Ohm resistors are used, the signals are DC coupled, if 0.047uF capacitors are used, the signals are AC coupled. When in Subsystem TS mode, stuff C0001/C0002, C0003/C0004, and C0007/C0008; when in TI mode (including TImaster), stuff C0011/C0012, C0013/C0014, and C0017/C0018. This will avoid driving conflict with SD.

There are four 8-bit switches on the TI, and marked as: S1, S2 (VME address space setting switches), SC01 (TI mode setting) and SC1 (TI clock setting). Some switches are LVTTL, some are LVPECL. When the switch is ON, the switch is LOW, (0V for LVTTL, and 1.4V for LVPECL); when the switch is OFF, the switch is HIGH, (3.3V for LVTTL, and 2.5V for LVPECL). Here are the details of the switch setting:

5.2.1. SC1 setting:

Bit1: LVPECL, open=high, trigger_1 source selection. When low, the trigger_1 source is FPGA MGT_112 output (serialized trigger data); when high, the trigger_1 source is standard FPGA differential output (pulse);

Bit2-5: LVTTL, open=high, P0 CLK_A, CLK_B, CLK_C, CLK_D selection. Clk_A is the same as CLK_C and CLK_B is the same as CLK_D. The clocks are selected in two stages:

Switch \ clock out	Clock_X	Clock_Y
Bit3=0; bit5=0	250	31.25
Bit3=1; bit5=0	250	125
Bit3=0; bit5=1	125	31.25
Bit3=1; bit5=1	125	125

Switch \ clock out	Clock_A, Clock_C	Clock_B, Clock_D
Bit2=0; bit4=0	Clock_X	Clock_X
Bit2=1; bit4=0	Clock_X	Clock_Y
Bit2=0; bit4=1	Clock_Y	Clock_X
Bit2=1; bit4=1	Clock_Y	Clock_Y

Bit[7:6]: LVPECL, open=HIGH, closed = LOW: TID 250MHz clock source selection. When bit7=0&bit6=0, on-board oscillator is selected; when bit7=1&bit6=0, TD input from optical transceiver #1 is selected; when bit7=0&bit6=1: subsystem clock input from optical transceiver#5 is selected; when bit7=1&bit6=1: front panel generic connector inputs is selected; For FPGA control, refer to A24 register offset 0x2C bit(1:0).

Bit8: LVPECL, open=high, TI connectors' sync signal source selection. When low, Sync_reset is selected; when high, Manchester encoded SYNC signal is selected.

5.2.2 SC01 setting:

Bit[2:1]: LVTTL, open=high. Firmware revision selection. When Bit2=0&Bit1=0, select firmware Rev0; when Bit2=0&Bit1=1, select firmware Rev1; when Bit2=1&bit1=0, select firmware Rev2; when Bit2=1&Bit1=1, select firmware Rev3. If the program bits are not compressed, the PROM XCF32P can only fit two revisions of the firmware.

For TImaster5 firmware (not the latest TIFPGA firmware), the Bit(4:3) are decoupled from Bit(2:1). The Bit(2:1) controls the firmware revision, while the Bit(4:3) is a firmware variable. If Bit(4) = 1, the CLK1 input of AD9510 is selected, which is the mux of four independent 250MHz clocks. If Bit(4)=0, the CLK2 input of AD9510 is selected, which is the clock from P0 backplane. If Bit(4)=1

and Bit(3)=0, the FiberMode=1, which will power down the HFBR#2, #3, #4, #6, #7 and #8. When the FiberMode=1, the TID is in pure TI mode.

Bit[6]: LVTTL, open = high. Connector output clock frequency selection. When high, the clocks are 41.667 MHz, used for CAEN TDC; when low, the clocks are 250 MHz, used for FADC250 fan-out

Bit[7,8]: LVTTL, open = high. This is to control the SD_link and CTP_link loopback test. When high, the driver is disabled, and the TI is the receiver for SD_link and CTP_link. When low, the driver is enabled, and the TI is the receiver and the driver. (loopback if no SD/CTP in the crate).

5.2.3 S1 setting:

Bit[1:3]: These three bits are used to control the OUTPUT(5:2) of the front panel 34-pin connector. The switches are used to multiplex the eight FPGA internal monitoring sources (32 signals) on the four output pins.

Bit[4]: Add an extra word if the total number of words in a block is odd. '1' to enable, '0' to disable;

Bit[8]: keep high, for TID_rev1, this pin is used as IACK input to the FPGA;

Bit[8:7]: keep high, for TID_rev2, these two pins are used as clock source selection output from the FPGA;

Bit[5:6]: not used.

5.2.4 S2 setting:

Bit[1:5]=A[23:19], VME address space in A32 or A24 mode. Be careful about the bit order. When in VME64x crate, these addresses should be set the same as its geographical address.

Bit6: LVPECL, open=high. The HFBR#1, #2, #3 and #4 trigger source selection. When low, the source is P0 (from SD), when high, the source is FPGA GTP_116.

Bit7: LVPECL, open=high. The HFBR#1_8 fan out clock source selection. When low, the fan out source is P0 (from SD), when high, the source is on-board clock manager AD9510. This should be consistent with the bit(4:3) of SC01 switch setting.

Bit8: LVPECL, open=high. The HFBR#5, #6, #7 and #8 trigger source selection. When low, the source is P0 (from SD), when high, the source is FPGA GTP_114.

5.3 Software setting:

After the board is properly set, and plugged in the right slot, some software setting needs be applied for the board to work. Some parts of the board needs be powered down to reduce the power consumption. The FPGA GTP transceivers will be automatically powered depending on the mode setting (TI or TImaster).

The delay settings will be automatically loaded by fiber measurement. This information could be saved in the Serial Flash Memory (SFM). The parameters (delay etc.) can be set by the VME, and stored in the SFM. We expect the parameter to be stable, but adjustment may be necessary when moving the board (different fiber connection etc.)

In the test setup and commissioning test, some delay parameters (especially the TImaster) needs be manually set.

6. VME Programming Requirements (This part will be updated as the firmware develops)

There are three categories of Address Modifier codes are supported on the TI: the user-defined codes (A24) for emergency firmware loading; Standard A24 for FPGA register read/write and slow control; A32 block transfer for VME data readout.

6.1 VME to JTAG emergency loading:

The AM[5:0] user defined codes are used for this logic. This works even before the FPGA is programmed and working. It is almost the same as A24D32 mode. The valid AM codes are: 0x19, 0x1A, 0x1D and 0x1E. These AM codes are user defined, and similar to the AM codes 0x39, 0x3A, 0x3D and 0x3E.

The valid address bits are A[31:24] do not care; A[23:19]=GA[4:0] for VME64x crates, or A[23:19]=0 for non-VME64x crates; A[18:2]=b'00011111111111111.

Data bit[1] is TDI; data bit[0] is TMS.

For example, if the board is in slot#5 (that is ~GA(4:0)= 11010), you need write to A(23:0)=0x28fffc. If data(1:0)=00, both TMS and TDI will be low; if data(1:0)=01, TMS is high, TDI is low; if data(1:0)=10, TMS is low, TDI is high; if data(1:0)=11, both TDI and TMS are high. The normal A24 address should try to avoid this address (0x0fffc).

A more advanced example: Instruction register shift (8-bit, shift in 0x5a) starting from/end up at the 'reset idle' mode: 14 consecutive writes to the address 0x28fffc with AM=0x19, 1a, 1d or 1e, the data are 1, 1, 0, 0, 0, 2, 0, 2, 2, 0, 2, 1, 1, 0 respectively.

Data	1	1	0	0	0	2	0	2	2	0	2	1	1	0
TMS	H	H	L	L	L	L	L	L	L	L	L	H	H	L
TDI	0x	0x	0x	0x	0	1	0	1	1	0	1	0	0x	0x

- "TMS H" means logic High, "TMS L" means logic Low, "TDI 0" means 0 or Low, "TDI 1" means 1 or High, and "TDI 0x" means DO NOT CARE by the JTAG, but the set value is 0.

6.2 Configuration Registers:

A24D32 are used for register read/write. Similar to the emergency loading logic, the base address is determined by the Geographic Address in VME64x crate, and external switch for non-VME64x crate. That is, A[23:19]=GA[4:0], or SW[5:1].

- Address offset: 0x00000: Board ID:

  Bit 7-0 (R/W): Crate ID; Reset default 0x00; [0x00, BIT(7:0)]
  Bit 12-8 (R): A24 address, higher 5 bits; Reset default 000 [0x54, BIT(4:0)]
  Bit 13 (R): '1': TS is in running mode, it is GA parity bit for TI;
  Bit 15-14 (R): '10': TS is in running mode (no more register changes), others: TS not in running mode;
  Bit 23-16 (R): PCB related setting, 0x01: production board, 0x00; prototype board;
  Bit 31-24 (R): Board type: 0x71: TI, 0x75: TS, 0x7D: TD. [0x54, BIT(31:16)]

- Address offset: 0x00004: Optic transceiver enable:

  Bit 7-0 (R/W): on TI: HFBR#8, #7, … #1 Enable, Reset default 0xFF all enabled. [0x04, BIT(7:0)]
  Bit 0: '1' enable HFBR#1, '0' disable HFBR#1; ('disable' means 'power down')
  Bit 1: '1' enable HFBR#2, '0' disable HFBR#2;
  Bit 2: '1' enable HFBR#3, '0' disable HFBR#3;
  Bit 3: '1' enable HFBR#4, '0' disable HFBR#4;
  Bit 4: '1' enable HFBR#5, '0' disable HFBR#5;
  Bit 5: '1' enable HFBR#6, '0' disable HFBR#6;
  Bit 6: '1' enable HFBR#7, '0' disable HFBR#7;
  Bit 7: '1' enable HFBR#8, '0' disable HFBR#8;

Bit8: Enable the P0 (SW#A, SW#B), Front panel connectors, and VmeP2 trigger and SyncReset signals, default is 1 to enable; When disabled, the trigger/SyncReset stay LOW.
Bit 23-16 (R): if '1', the HFBR#8, #7, … #1 is connected to a TI (serial Link synchronized);
Bit 31-24 (R): if '1', the HFBR#8, #7,…#1 connected TI has its trigger source enabled.

- Address offset: 0x00008: Interrupt setting:

Bit 7-0 (R/W): Interrupt ID; Reset default 0xC8 [0x08, BIT(7:0)]
Bit 10-8 (R/W): Interrupt level; Reset default 5; [0x08, BIT(10:8)]
Bit 16 (R/W): IRQ enable. Reset default: 0; [0x04, BIT(13)]

- Address offset: 0x0000C: Trigger delay and Pulse width:

Bit 7-0 (R/W): Trigger_1 delay, (n+1)*4 ns; Reset default 0x07; [0x0C, BIT(7:0)]
Bit 15-8 (R/W): Trigger_1 Pulse width (n+1)*4 ns; Reset default 0x07; [0x0C, BIT(15:8)]
Bit 23-16 (R/W): Trigger_2 delay, (n+1)*4 ns; Reset default 0x07; [0x0C, BIT(23:16)]
Bit 31-24 (R/W): Trigger_2 Pulse width (n+1)*4 ns. Reset default 0x07; [0x0C, BIT(27:24)]

- Address offset: 0x00010: A32 address space:

Bit 13-5 (R/W): Address Max; Reset default 0x1FF; [0x10, BIT(13:5)]
Bit 22:14 (R/W): Address Min; Reset default 0x000; [0x10, BIT(22:14)]
Bit 31-23 (R/W): Base Address. Reset default 0x100; [0x10, BIT(31:23)]

- Address offset: 0x00014: Block size:

Bit 7-0 (R/W): Block size. Reset default 0x01; This is used on TD only. It's read/write register but does not affect anything in the FPGA.
Bit 23-16 (R): Block size (block level). This is the block level used on the FPGA.
Bit 31-24 (R): Block size set by TS (or TImaster). This is an intermediate value. The ROC should readout these eight bits, and set them to the FADC250, FADC125, etc.

- Address offset: 0x00018: TI data format control: Reset default 011; [0x00, BIT(31:29)]

Bit 0: if '1', two block placeholder words are enabled; '0' disabled.
Bit 2-1: Event format control:
bit 1: '1' to enable the lower 32-bit trigger timing word;
bit 2: '1' to enable the higher 16-bit of event number and higher 16-bit of trigger timing;

- Address offset: 0x0001C: VME setting; Reset default 0x011:

Bit 0 (R/W): '1' enable Bus_Error_En, so the block read can be terminated by event block trailer; [0x10, BIT(0)]
Bit 1 (R/W): '1' en_token_in is true, '0' en_token_in is false; [0x10, BIT(1)]
Bit 2 (R/W): '1' enable 'Multi-board' readout, '0' disable 'Multi-board'; [0x10, BIT(2)]; asset to enable multi-board token passing protocol;
Bit 3 (R/W): '1' enable en_A32m, '0' disable en_A32m; [0x10, BIT(3)]; assert to enable common A32 multi-board addressing of module;
Bit 4 (R/W): '1' enable en_A32, '0' disable en_A32; [0x10, BIT(4)]
Bit 7 (R/W): '1' enable VME bus interrupt for module error?

Bit 8 (R/W): '1' I2C device address 0x1101xxx, '0' I2C device address 0x0000xxx; [0x04, BIT8]
Bit 9 (R/W): '1' token_in high, '0' token_in low; [0x04, BIT(9)]. If both bit 9 and bit 1 are set high, the Token_Out will be high (this is for SD test).
Bit 10 (R/W): '1' first_board true, '0' first_board false; [0x04, BIT(10)]
Bit 11 (R/W): '1' last_board true, '0' last board false; [0x04, BIT(11)]
Bit 15 (R/W): '1' disable data readout buffer full [0x04, BIT(15)]

- Address offset: 0x00020: Trigger source register:

Bit 15-0 (R/W): Trigger source enables: Reset default 0x0000; [0x00, BIT(23:16)]
Bit 0: P0 trigger input;
Bit 1: HFBR#1 trigger input;
Bit 2: TImaster loopback trigger input;
Bit 3: Front Panel trigger input;
Bit 4: VME trigger;
Bit 5: Front Panel Trigger Codes (as Supervisor) inputs;
Bit 6: TS_rev2 trigger input;
Bit 7: Random Trigger.
Bit 10: HFBR#5 trigger input
Bit 12: SubTS#1 trigger enable, this is valid on HFBR#1 input only;
Bit 13: SubTS#2 trigger enable, this is valid on HFBR#1 input only;
Bit 14: SubTS#3 trigger enable, this is valid on HFBR#1 input only;
Bit 15: SubTS#4 trigger enable, this is valid on HFBR#1 input only;
Bit 31-16 (R): Trigger source monitor. [0x00, BIT(31:24)]

- Address offset: 0x00024: Sync Source register:

Bit 15-0 (R/W): Sync Source enables: Reset default 0x02; [0x00, BIT(28:24)]
Bit 0: P0 sync input (in Subsystem TS mode);
Bit 1: HFBR#1 sync input;
Bit 2: HFBR#5 sync input;
Bit 3: Front panel trigger inhibit enable;
Bit 4: TImaster loopback SYNC enable
Bit 6: automatic SyncReset enable
Bit 7: Enable the option for RESET to be set high (sync code 0x99), and low (sync code 0xcc).
Bit(11-8) (R): last SYNC code from HFBR#1;
Bit(15-12) (R): last SYNC code from HFBR#5;
Bit(19:16) (R): last SYNC code from loopback;
Bit(20) (R): SYNC history fifo empty;
Bit(21) (R): SYNC history fifo has more than 512 entries;
Bit(22) (R): SYNC history fifo full (reached 1024 entries);
Bit 31-24 (R): Sync source monitoring. [0x28, BIT(23:16)]

- Address offset: 0x00028: Busy source registers:

Bit 15-0 (R/W): Busy source enables: [0x04, BIT(31:16)]

Bit 0: '1' enable the Switch Slot #A BUSY input, '0' disable;
Bit 1: '1' enable the Switch Slot #B BUSY input, '0' disable;
Bit 2: '1' enable the VME P2 BUSY input, '0' disable;
Bit 3: '1' enable the FTDC front panel BUSY input, '0' disable;
Bit 4: '1' enable the FADC front panel BUSY input, '0' disable;
Bit 5: '1' enable the Front Panel BUSY, which is the same as TsRev2 busy;
Bit 7: '1' enable TS feed_back BUSY, '0' disable the busy. (useful in TM mode)
Bit 15-8: HFBR #8-#1 BUSY enables: '1' enable the HFBR BUSY input, '0' disable;
Bit 31-16 (R): BUSY source monitoring. [0x28, BIT(15:0)]

- Address offset: 0x0002C: Clock source selection:

  Bit 1-0 (R/W): software bit switch to control the clock source. Reset default 00; [0x08, BIT(13:12)]
  Bit[1:0] = 00: oscillator clock;
  Bit[1:0] = 01: HFBR#5 clock input;
  Bit[1:0] = 10: HFBR#1 clock input;
  Bit[1:0] = 11: Front panel 34-pin connector clock input.

- Address offset: 0x00030: Trigger_1 pre-scale:

  Bit 15-0 (R/W): pre-scale factor: Rate = Rate_0 / (Bit(15:0)+1). [0x0C, BIT(31:28)]

- Address offset: 0x00034: Trigger block inhibit:

  Bit 7-0 (R/W): TS trigger inhibit threshold (in the unit of event blocks); Reset default 0x01; [0x08, BIT(31:24)]
  Bit 23-8 (R): Number of blocks in the DAQ ready to be readout. [0x14, BIT(31:24)]
  (on TI, Bit 23-16 (R): Number of events before the a block is formed. [0x14, BIT(23:16)])
  Bit 27-24 (R): Number of missing block acknowledge;
  Bit 28 (R): if '1', the RUN is stopped because the block number (readout) has reached. (set by 0xFC)
  Bit 29 (R): if '1', the event block is being filled by FillTrg;
  Bit 30 (R): SyncReset Request set. If '1', SyncReset is required. To be issued by TImaster/TS.
  Bit 31 (R): SyncEvent received, and the system is BUSY. Waiting for ROC to clear the frontend data.

- Address offset: 0x00038: Trigger rules:

  Bit 7-0 (R/W): No more than 1 Trigger in (Bit(6:0)*(16/500 ns)); Bit7 determines 16ns or 500ns step. Reset default 0x03; [R:0x58, BIT(23:16)] [W:0x810, BIT(7:0)]
  Bit 15-8 (R/W): no more than 2 trigger in (Bit(14:8)*(16/500ns)); Bit15 determines 16ns or 500ns step. Reset default 0x03; [W:0x810, BIT(15:8)]
  Bit 23-16 (R/W): no more than 3 triggers in (Bit(22:16)*(16/500 ns)); Bit23 determines 16ns or 500ns step. Reset default 0x03; [R:0x58, BIT(31:24)] [W:0x810, BIT(23:16)]
  Bit 31-24 (R/W): no more than 4 triggers in (Bit(30:24)*(16/500 ns)). Bit31 determines 16ns or 500ns step. Reset default 0x03; [W:0x810, BIT(31:24)]

- Address offset: 0x0003C: Trigger coincidence window:

  Bit 7-0 (R/W): Trigger input coincidence window; Reset default 0x01;
  Bit15-8 (R/W): Trigger inhibit window (extra to bit(7:0)). Reset default 0x00;

These two parameters are used to determine the event resolution

- Address offset: 0x00048: Front panel generic trigger input enable:

  Bit 15-0 (R/W): Front panel generic trigger input enable (34-pin TI). Reset default 0x00000000; [0x08, BIT(21:16)] The lower 6 bits are used for front panel TS_code input control.

- Address offset: 0x0004C: Blocks for VME interrupt:

  Bit 15-0 (R/W): 4-bit output to the front panel generic output connector; Reset default 0x0000; [0x2C, BIT(3:0)]
  Bit 23-16 (R): Number of data blocks ready for VME interrupt. [0x2C, BIT(31:24)]
  Bit 31-24 (R): on TI: Number of events of a partial block (or, before the block is formed)
  On TS: bit(15:8) of the number of data blocks ready for VME interrupt.

- Address offset: 0x00050: Sync delay setting (to compensate for the fiber length):

  Bit 7-0 (R): on TI: SYNC phase of HFBR#1 input; [0x1C, BIT(7:0)]
  Bit 15-8 (R/W): HFBR#1 SYNC input delay; Reset default 0x00; [0x1C, BIT(15:8)]
  Bit 23-16 (R/W): TM (internal loopback) SYNC delay; Reset default 0x00; [0x1C, BIT(23:16)]
  Bit 23-16 (R): on TI: SYNC phase of HFBR#5 input; [0x1C, BIT(23:16)]
  Bit(31:24 (R/W): HFBR#5 SYNC input delay. Reset default 0x00; [0x1C, BIT(31:24)]

- Address offset: 0x00074: Front Panel generic trigger input pre-scale: Reset default 0x00000000

  Bit 3-0 (R/W): FP Generic trigger input #1;
  Bit 7-4 (R/W): FP Generic trigger input #2;
  Bit 11-8 (R/W): FP Generic trigger input #3;
  Bit 15-12 (R/W): FP Generic trigger input #4;
  Bit 19-16 (R/W): FP Generic trigger input #5;
  Bit 23-20 (R/W): FP Generic trigger input #6;

- Address offset: 0x00078: VME Sync Load[0x900, BIT(7:0)]

  Bit 7-4 == Bit 3-0 (R/W): 4-bit sync code; Decoding of the Sync command (bit[7:0]):
  0x11: VME clock DCM reset, and full reset;
  0x22: CLK250 resync (AD9510, DCM resync and MGT reset);
  0x33: AD9510 re-sync (slower clock phase adjustment), part of 0x22 function;
  0x44: Reset the MGT status_B registers;
  0x55: Trigger link enable (serial link started), FIFO read counter reset;
  0x77: Trigger link disable, trigger FIFO write counter reset;
  0xAA: reset the TIslave trigger ready register;
  0xBB: Reset the event number, and trigger input scalars (the 0xDD will not do);
  0xDD: (SyncReset), FPGA logic and counter reset, this reset all goes to SD, CTP/GTP;
  0x99: Force SyncReset high if this feature is enabled (by offset 0x24, bit 7);
  0xCC: set the SyncReset low if it is forced high by code 0x99.
  0x66, 0x88, 0xee: to be assigned;
  0x00, 0xff: reserved, not to be assigned

- Address offset: 0x0007C: VME Sync Delay. The latency before being serialized.

  Bit 6-0 (R/W): latency, in 4ns steps. Reset default 000,0111 [0x904, BIT(6:0)]

- Address offset: 0x00080: Reset pulse width: Reset default 00,0111

  Bit 7-0 (R/W): Reset (to SW#A, SW#B and on-board) pulse width. Pulse width is (Bit(6:0)*(4/32 ns)), Bit(7) determines the steps (4ns or 32ns); [0x904, BIT(13:8), bit(13) set to pulse to 1us wide]

- Address offset: 0x00084: VME Trigger/Command Register

  Bit 11-0 (R/W): Trigger Command code transmitted in the trigger link; In the 12 bits, 0xABC, the 0xA determines the command type. For example:

  Bit(11-0) = 0x123: (A=1) one trigger1 (readout trigger) pulse will be generated, and the event type = 0x23;

  Bit(11-0) = 0x221: (A=2) one trigger2 pulse will be generated. The 0x21 is ignored;

  Bit(11-0) = 0x812: (A=8) Set the block level (size), and the block level is set to 0x12.

- Address offset: 0x00088 (R/W): VME Random Trigger Command Register: [0x808, BIT(15:0)]

  Bit 3-0: Random trigger_1 rates: 500KHz/($2^{Bit(3:0)}$);
  Bit 6-4: same as Bit(2-0) for redundancy check. No match, no trigger_1;
  Bit 7: enable/disable random trigger_1; (There is NO requirement that it match with bit 3)
  Bit 11-8: Random trigger_2 rates: 500KHz/($2^{Bit(11:8)}$);
  Bit 14-12: same as Bit(10-8) for redundancy check. No match, no trigger_2.
  Bit 15: enable/disable random trigger_2;

- Address offset: 0x0008C(R/W): VME Trigger Generation: [0x804, BIT(31:0)]

  Bit 15-0: Number of trigger_1s to be generated; If 0xFFFF, the number of event will not be limited.
  Bit 31-16: (trigger rate control) Time between triggers. T = (120+30*Bit(30:16)*$1024^{Bit(31)}$) ns. (Assuming that the ClkVme=33MHz or 30ns period).

- Address offset: 0x00090(R/W): VME Trigger_2 Generation: [0x80C, BIT(31:0)]

  Bit 15-0: Number of trigger_2s to be generated;
  Bit 31-16: (trigger rate control) Time between triggers. T = (120+30*Bit(30:16)*$1024^{Bit(31)}$) ns. (Assuming that the ClkVme=33MHz or 30ns period).

- Address offset: 0x00094 (R): Number of Blocks in the DAQ system: [0x14, BIT(15:0)]

  Bit 31-24: Number of events before a full data block;
  Bit 23-0: Number of full data blocks the TI has ever generated;

- Address offset: 0x00098 (R): SYNC history fifo, The fifo status is in register offset 0x24.

  Bit 31-16: time stamp of the SYNC command, in steps of ~8us;
  Bit(15): whether the time stamp has overflowed since previous SYNC code
  Bit (14): Loopback sync valid;
  Bit (13:10): Loopback sync code;
  Bit (9): HFBR#5 sync valid;
  Bit (8:5): HFBR#5 sync code;

Bit (4): HFBR#1 sync valid;
Bit (3:0): HFBR#1 sync code;

- Address offset: 0x0009C (R/W): The FPGA running mode;

  Bit 7-0: TS in running mode if set to 0x5A; if other value, not in running mode. Reset default 0x00;
  TI in running mode if set to 0x71. TI starts clock monitoring in 'running' mode.

- Address offset: 0x000A0 (R): Fiber latency measurement result: [0x18]

  Bit 31-23: latency data in 4ns steps
  Bit 22-16: Delay in the IODelay, in 5000/64=78.125ps steps
  Bit 15:0: Delay in the carry chain, two bits per slice, (or two mux per bit)

- Address offset: 0x000A4 (R): Fiber latency measurement result from HFBR#5

  Bit 31-23: latency data in 4ns steps
  Bit 22-16: Delay in the IODelay, in 5000/64=78.125ps steps
  Bit 15:0: Delay in the carry chain, two bits per slice, (or two mux per bit)

- Address offset: 0x000A8 (R): Trigger live timer: [0x20]

  Bit 31-0 (r): board live time counter. The real time is Bit(31:0)*256*30ns.

- Address offset: 0x000AC (R): Trigger busy (trigger dead) timer: [0x24]

  Bit 31-0 (r): TID busy (cannot accept trigger, or trigger dead) time counter. The real time is Bit(31:0)*256*30ns. This counter and the live time counter make up the total time counter, which is the total time since any one of the trigger sources is enabled.

- Address offset: 0x000B0 (R): MGT STATUS_A: [0x30]

  Bit 7-0: MGT[7:0] reset_done;
  Bit 11-8: MGT PLL lock detected (two MGTs per PLL lock);
  Bit 15-12: fixed at 0x9
  Bit 23-16: loopback trigger buffer length, this is the similar register as bit(9:0) of register offset 0xB8.
  Bit 31-24: if '1', the HFBR#8, #7,…#1 is receiving idle word (K byte plus non-K byte);

- Address offset: 0x000B4 (R): MGT STATUS_B registers: [0x34]

  Bit 7-0: Channel bonding sequence detected in MGT[7:0];
  Bit 15-8: received data is not an 8B/10B character, or has disparity error in MGT[7:0];
  Bit 23-16: RX disparity error has occurred in MGT[7:0];
  Bit 31-24: Rx data not in 8B/10B table has occurred in MGT[7:0].

- Address offset: 0x000B8 (R): MGT trigger data buffer length: [0x38]

  Bit 9-0: Global trigger data buffer length (to be minimized to 0 for the longest fiber);
  Bit 11-10: Data generation fifo full (in TRGDAQ module);
  Bit 13-12: Data Readout fifo prog_almost_full (in VME module);
  Bit 15:14: Data Readout fifo full; The order should be: DataReadoutFifoProgFull → DataGenFifoFull → DataReadoutFifoFull

Bit 25-16: Sub-system trigger data buffer length;
Bit 27: TI is in running mode if '1';
Bit 28: HFBR#1 MGT receiver error;
Bit 29: CLK250 DCM locked;
Bit 30: Clk125 DCM locked;
Bit 31: VME CLK (33MHz or 25MHz) DCM locked

- Address offset: 0x000BC (R): TS input trigger counter: [0x3C]

  Bit 31-0: Number of triggers received by TS (before BUSY inhibits).

- Address offset: 0x000C0 (R): valid for TM (or with TS function), not valid for TI: [0x40]

  Bit 7-0: Number of blocks to be readout on HFBR#1;
  Bit 15-8: Number of blocks is still missing on HFBR#1
  Bit 23-16: Number of blocks to be readout on HFBR#2
  Bit 31-24: Number of blocks is still missing on HFBR#2

- Address offset: 0x000C4 (R): valid for TM (or with TS function), not valid for TI: [0x44]

  Bit 7-0: Number of blocks to be readout on HFBR#3;
  Bit 15-8: Number of blocks is still missing on HFBR#3;
  Bit 23-16: Number of blocks to be readout on HFBR#4;
  Bit 31-24: Number of blocks is still missing on HFBR#4;
  For TS, Bit 31-0: External Trigger counter, Number of triggers from External trigger before lookup table.

- Address offset: 0x000C8 (R): valid for TM (or with TS function), not valid for TI: [0x48]

  Bit 7-0: Number of blocks to be readout on HFBR#5;
  Bit 15-8: Number of blocks is still missing on HFBR#5;
  Bit 23-16: Number of blocks to be readout on HFBR#6;
  Bit 31-24: Number of blocks is still missing on HFBR#6;
  For TS, Bit 31-0: FrontPanel Trigger counter, Number of triggers from FP trigger before lookup table.

- Address offset: 0x000CC (R): valid for TM (or with TS function), not valid for TI: [0x4C]

  Bit 7-0: Number of blocks to be readout on HFBR#7;
  Bit 15-8: Number of blocks is still missing on HFBR#7;
  Bit 23-16: Number of blocks to be readout on HFBR#8;
  Bit 31-24: Number of blocks is still missing on HFBR#8;

- Address offset: 0x000D0 (R): valid for TM (or with TS function)

  Bit 4-0: A24 address used for the module (to match with A23-A19); [0x54, BIT(4:0)]
  Bit 9-5: A24 address set by the onboard hardware switch; [0x54, BIT(9:5)]
  Bit 14-10: GA(4:0), VME64x geographic address; [0x54, BIT(14:10)]
  Bit 15: parity of GA(4:0); [0x54, BIT15]
  Bit 27-16: Number of blocks to be readout on TM itself; [0x50, BIT(23:16)]
  Bit 31-28: Number of blocks is still missing on TM itself; [0x50, BIT(31:24)]

- Address offset: 0x000D4 (R/W): Periodic Sync Event register

Bit 15-0: Number of data blocks to assert a sync event (periodic SyncEvent);
Bit 23-16: Sync event enable if set to 0x5A;

- Address offset: 0x000D8 (R): Event number register

  Bit 15-0: Number of data blocks to assert a sync event (periodic SyncEvent);
  Bit 31-16: higher 16-bit (bit 47-32) of event number counter;

- Address offset: 0x000DC (R): Event number register

  Bit 31-0: lower 32-bit (bit 31-0) of event number counter.

- Address offset: 0x000F0 (R): valid for TM (or with TS function)

  Bit 31-0: Number of valid code from Front Panel Async trigger inputs

- Address offset: 0x000FC (R/W): End_of_Run number of block setting

  Bit 31-0: number of block to End the run. If this is set to 0, there is no limit (disabled).

  Bit 0: Enable the front panel (external input) signal to latch the trigger input scalars;

  Bit 1: Enable the front panel (same signal as controlled by bit0) to reset the trigger input scalars; **These two** bits are kind of related to the OneShotVme command, offset 0x100, bit 24 and bit25.

- Address offset: 0x00100 (W): Reset and one-shot registers. The signal will be one ClkVme cycle. If the ClkVme is 25 MHz, the one-shot will be 40ns wide. Positive logic. [0x100]

  Bit 0: not used;
  Bit 1: if '1', RESET signal to reset the VME_to_I2C engine;
  Bit 2: if '1', RESET signal to reset the VME_to_JTAG engine;
  Bit 3: if '1', RESET signal to reset the VME_to_SFM engine;
  Bit 4: if '1', RESET signal to reset the VME registers (TID settings) to their default values;
  Bit 6: if '1', reset the SYNC history fifo (clear the fifo);
  Bit 7: if '1', this register will generate a BUSY reset, and Trg_Ack pulse (TS rev2 compatible).
  Bit 8: if '1', Reset the CLK250/Clk200 DCM.
  Bit 9: if '1', Reset the CLK125 DCM.
  Bit 10: if '1', Reset the MGT (MultiGigabit Transceiver,) inside the FPGA.
  Bit 11: if '1', Auto alignment of SYNC phase from HFBR#1; auto align P0 sync input for TD.
  Bit 12: if '1', TI: Auto alignment of SYNC phase from HFBR#5;
  TS: reset the BRAM loading address to 0 (very beginning).
  Bit 13: if '1', Auto alignment of fiber latency measurement signals;
  Bit 14: if '1', Reset the IODELAY;
  Bit 15: if '1', Measure the fiber latency
  Bit 16: if '1', this register will generate a 'TAKE_TOKEN'
  Bit 17: if '1', the available number of data blocks will decrease by 1,
  Bit 20: if '1', generate a SyncEvent (forced SyncEvent). This can be used as end_of_run etc.
  Bit 23: if '1', generate Sync_Reset_Request.
  Bit 24: if '1', all the trigger input scalars are latched (ready for read out), the BusyTimer and LiveTimer are also latched;
  Bit 25: if '1', all the trigger input scalars are reset. (Bit 24 and Bit 25 can be set simultaneously). The event number is also reset by this.

Bit 31: if '1', the end_of_run command. If the readout block is not full, dummy trigger will be generated to fill the block.

- Address offset: 0x00180 (R): FP input trigger scalar for #1:

  Bit 31-0: 32-bit scalar, number of input#1 counter

- Address offset: 0x00184 (R): FP input trigger scalar for #2:

  Bit 31-0: 32-bit scalar, number of FP input#2 counter

- Address offset: 0x00188 (R): FP input trigger scalar for #3:

  Bit 31-0: 32-bit scalar, number of FP input#3 counter

- Address offset: 0x0018C (R): FP input trigger scalar for #4:

  Bit 31-0: 32-bit scalar, number of FP input#4 counter

- Address offset: 0x00190 (R): FP input trigger scalar for #5:

  Bit 31-0: 32-bit scalar, number of FP input#5 counter

- Address offset: 0x00194 (R): FP input trigger scalar for #6:

  Bit 31-0: 32-bit scalar, number of FP input#6 counter

- Address offset: 0x001D0 (R): optic transceiver HFBR#1 TI ID (in master mode)

  Bit 7-0: Trigger Source Enable of the TI connected to fiber#1;
  Bit 15-8: Crate ID of the TI connected to fiber#1.
  Bit 23-16: Block level set on TI connected to fiber#1.

- Address offset: 0x001D4 (R): optic transceiver HFBR#2 TI ID (in master mode)

  Bit 7-0: Trigger Source Enable of the TI connected to fiber#2;
  Bit 15-8: Crate ID of the TI connected to fiber#2.
  Bit 23-16: Block level set on TI connected to fiber#2.

- Address offset: 0x001D8 (R): optic transceiver HFBR#3 TI ID (in master mode)

  Bit 7-0: Trigger Source Enable of the TI connected to fiber#3;
  Bit 15-8: Crate ID of the TI connected to fiber#3.
  Bit 23-16: Block level set on TI connected to fiber#3.

- Address offset: 0x001DC (R): optic transceiver HFBR#4 TI ID (in master mode)

  Bit 7-0: Trigger Source Enable of the TI connected to fiber#4;
  Bit 15-8: Crate ID of the TI connected to fiber#4.
  Bit 23-16: Block level set on TI connected to fiber#4.

- Address offset: 0x001E0 (R): optic transceiver HFBR#5 TI ID (in master mode)

  Bit 7-0: Trigger Source Enable of the TI connected to fiber#5;
  Bit 15-8: Crate ID of the TI connected to fiber#5.

Bit 23-16: Block level set on TI connected to fiber#5.

- Address offset: 0x001E4 (R): optic transceiver HFBR#6 TI ID (in master mode)

  Bit 7-0: Trigger Source Enable of the TI connected to fiber#6;
  Bit 15-8: Crate ID of the TI connected to fiber#6.
  Bit 23-16: Block level set on TI connected to fiber#6.

- Address offset: 0x001E8 (R): optic transceiver HFBR#7 TI ID (in master mode)

  Bit 7-0: Trigger Source Enable of the TI connected to fiber#7;
  Bit 15-8: Crate ID of the TI connected to fiber#7.
  Bit 23-16: Block level set on TI connected to fiber#7.

- Address offset: 0x001EC (R): optic transceiver HFBR#8 TI ID (in master mode)

  Bit 7-0: Trigger Source Enable of the TI connected to fiber#8;
  Bit 15-8: Crate ID of the TI connected to fiber#8.
  Bit 23-16: Block level set on TI connected to fiber#8.

- Address offset: 0x001F0 (R): The TI master (itself) ID (in master mode)

  Bit 7-0: Trigger Source Enable of the TI itself, should be the same as bit7-0 of register 0x20;
  Bit 15-8: Crate ID of the TI itself, should be the same as bit7-0 of register 0x00.

- Address offset: 0x008CX (0x8C0 – 0x8FC) (W): Trigger table loading: (prototype TS / TImaster) [0x8CX]

  Bit 31-0: 32-bit wide table loading.
  Address bits(5-2) are used to load 16 32-bit words;
  6-bit read addressing with 8-bit trigger type (byte wide)

- Address offset: 0x02000~0x021FC (R): Mirror registers for VXS switch slot #B on TI board

  Bit 31-0: 32-bit wide SD status (or data).

- Address offset: 0x02800~0x029FC (R): Mirror registers for VXS switch slot #A on TI board

  Bit 31-0: 32-bit wide CTP/GTP status (or data).

6.3 VME to Serial engines:

A24D32 are used for VME to serial engines. The engines include: VME to JTAG engine for the FPGA, VME to JTAG engine for the PROM, VME to I2C for the switch slot #A, VME to I2C engine for the switch slot #B, and VME to I2C engine for the P2 connector (could be used for anything). In the I2C engines design, only the lower one-byte or 2-byte of the 32-bit data word is used. The higher bytes are not used.

Address offset: 0x1XXXX: JTAG for PROM; Refer to the programming manual for VME to JTAG design for details.

Address offset: 0x2XXXX: JTAG for FPGA;

Address offset: 0x3XXXX: I2C for VXS switch slot #A; Refer to the programming manual for VME to I2C design for details.

Address offset: 0x4XXXX: I2C for VXS switch slot #B;
Address offset: 0x5XXXX: I2C for VME P2 connector (to be assigned);
Address offset: 0x6XXXX: Serial Flash memory interface.
Address offset: 0x0NXXX: SFM memory readout: (to be implemented)
0x07X0: IO_Delay #X reset;
0x07X4: IO_Delay #X delay increment (by 1);
0x07X8: IO_Delay #X de-serialized data readout, idle='0xFFFF';
0x07Xc: IO_Delay #X automatic delay increment by a number stored in SFM.

6.4 VME data acquisition:

For data acquisition, the A32 block reads are used. The base address is set by the upper 9 bits of A24 register 0x00010, that is A[31:23] = RegData[31:23] of A24=0x00010.

7 Backplane pin out tables:

7.1 VXS P0 Pinout Table

Payload slot#18, TI or TImaster			
Pin name	Signal Description	Signal Level	Direction
DP1 (A1+, B1-)	CLOCK_C	LVPECL(DP)	PP18 → SWA
DP2 (D1+, E1-)	CLOCK_D	LVPECL(DP)	PP18 → SWA
DP3 (B2+, C2-)	Not Used		
DP4 (E2+, F2-)	SYNC	LVPECL(DP)	PP18 → SWA
DP5 (A3+, B3-)	TRIG1	LVPECL(DP)	PP18 → SWA
DP6 (D3+, E3-)	TRIG2	LVPECL(DP)	PP18 → SWA
DP7 (B4+, C4-)	TP_Data_LINK	LVDS(DP)	PP18 ←→ SWA
DP8 (E4+, F4-)	BUSY	LVDS	PP18 ← SWA
SE1 (G1)	SCL	I2C (+3.3V)	PP18 → SWA
SE2 (G3)	SDA	I2C (+3.3V)	PP18 ←→ SWA
DP23 (B12+, C12-)	CLOCK_A	LVPECL(DP)	PP18 → SWB
DP24 (E12+, F12-)	CLOCK_B	LVPECL(DP)	PP18 → SWB
DP25 (A13+,B13-)	TOKEN_OUT	LVDS(DP)	PP18 → SWB
DP26 (D13+, E13-)	SYNC	LVPECL(DP)	PP18 → SWB
DP27 (B14+, C14-)	TRIG1	LVPECL(DP)	PP18 → SWB
DP28 (E14+, F14-)	TRIG2	LVPECL(DP)	PP18 → SWB
DP29 (A15+,B15-)	SD/GTP_Data_Link	LVDS, 250Mbps	PP18←→SWB
DP30 (D15+,E15-)	BUSY	LVDS	PP18 ← SWB
SE7 (G13)	SCL	I2C(+3.3V)	PP18 → SWB
SE8 (G15)	SDA	I2C(+3.3V)	PP18 ←→ SWB

7.2 Other payload slots for subsystem TS:

DP23 (B12+, C12-)	TRIG_LINK	LVPECL(DP)	PP ← SWB
DP24 (E12+, F12-)	SYNC	LVPECL(DP)	PP ← SWB
DP25 (A13+, B13-)	CLK250MHz	LVPECL(DP)	PP ← SWB
DP26			

DP27			
DP28			
DP29	SD_Data_link	LVDS	PP←→SWB
DP30	BUSY	LVDS	PP → SWB
SE7			
SE8			

7.3 VME P2 User-defined pin table

Similar to this, but Row-C is used. The two adjacent pins are used as a pair for differential signals.

Pin name	Signal Name	Signal Level
C01	SCL	I2C (LVCMOS)
C02	SDA	I2C (LVCMOS)
C05	CLK250_P	ECL
C06	CLK250_N	ECL
C09	CLK_A_P	ECL
C10	CLK_A_N	ECL
C13	CLK_B_P	ECL
C14	CLK_B_N	ECL
C17	TRIG1_P	ECL
C18	TRIG1_N	ECL
C21	TRIG2_P	ECL
C22	TRIG2_N	ECL
C25	SYNC_P	ECL
C26	SYNC_N	ECL
C29	BUSY+	ECL
C30	BUSY-	ECL

8 TID Operation examples:

The following is some operating procedures at VxWorks interactive mode. This is just a memo for the quick test of the TID board. They may change as the TID debug proceeds. First, one needs to login the VME controller. Here is the sequence:

Xming to PHECDA, linux server computer

From any xterm (or PUTTY), telnet to DAVW1 (neither username, nor password is needed). Only one telnet process is supported for the MVME6100 module). The address mapping for A24 is 0x90xxxxxx. For DAVW8, which is a MVME5100 module, the address mapping for A24 is 0xFA000000. The M6100 has twice as much as M5100 in A32 memory. The M5100 is 0x08000000-0x0FFFFFFF; while the M6100 is 0x08000000-0x17FFFFFF.

The following commands are assuming that the TI is in slot#21 VME64x compatible crate (Geographic address available). 0xA8 = 10101xxx, that is the Geographic Address GA=21 or 10101.

8.1 A24 register echoing (write and read):

➔ *(0x90A80008)=0x5566aa99; the same register should be read out

8.2 Readout the FPGA user_ID:

The FPGA user code is readout through VME_to_JTAG engine. The FPGA user_ID is firmware specific. If this code matches, it is TID and the right version of the firmware is loaded.

- ➔ *(0x90a80100)=0x04: VME_to_JTAG engine logic reset
- ➔ *(0x90aa003C)=0x0: Reset FPGA JTAG to 'reset_idle' state
- ➔ *(0x90aa092C)=0x3C8: enable user_ID readback
- ➔ *(0x90aa1F1C)=0x00: shift in 32-bit data, and the readback is user_ID. The user_ID should be 710xnmmm: n is the major version of the firmware, mmm is the revision of the firmware.

8.5 SW#A I2C operation:

The VME_to_I2C engine hides the serialization, and the two-bytes write (and/or read) can be finished by a single VME write (and/or read) command. For SW#A, the I2C chain is 011; for device 1101000, the I2C device at the FPGA is 000; assuming the byte address is 0xAD (10101101).

- ➔ *(0x90a80100)=0x01: VME_to_I2C engine reset
- ➔ *(0x90ab1EB4)=0xDADA: VME_to_I2C write
- ➔ m 0x90ab1EB4, 4: VME to I2C read. ignore the higher two bytes
- ➔ *(0x90a80004)=0x100: Set the I2C address to 0b1101xxx
- ➔ *(0x90ab1eb4)=0xdata: VME to I2C write

9 TID Operation procedures (software setup):

The following is the operating procedures at VxWorks interactive mode. This is just a memo for the quick test of the TI board. The procedure will be optimized as the test goes along. This assumes that the hardware switch is set properly (as TI, TD, TS/TD/TI etc.)

9.1 Fiber latency measurement:

- ➔ *(0x90a80100)=0x4000 //reset the digital IODELAY logic/clock
- ➔ *(0x90a80100)=0x2000 //phase alignment of the latency measurement signal
- ➔ *(0x90a80100)=0x8000 //Fiber latency measurement
- ➔ M 0x90a800a0,4 //Fiber latency readout
- ➔ *(0x90a80100)=0x800 //Sync phase alignment relative to the 250MHz clock
- ➔ *(0x90a80050)=0xAAxxBBxx // load the Sync delay (AA for HFBR#5, BB for HFBR#1). The BB should be based on the previous measurement.
- ➔ M 0x90a80050,4 //check the SYNC delay setting and phase alignment.

9.3 Trigger link startup:

- ➔ *(0x90a80078)=0x77
- ➔ *(0x90a80078)=0x77 //WriteStart, buffer_write_address reset and trigger data transmit disable
- ➔ *(0x90a8007c)=0x54 //Sync latency, delay before SYNC being serialized. This delay should cover the trigger word sterilizer/deserializer delay.
- ➔ *(0x90a80080)=0x7 //. The Reset pulse width is (7+1)*4ns;
- ➔ *(0x90a80078)=0x55 //Start the trigger link, and this SYNC command will enable the trigger link buffer readout.

9.7 Trigger/DAQ monitoring:

- ➔ M 0x90a80034, 4 //polling the register to see if there is data block to read
- ➔ M 0x90a800a8, 4 //TID trigger live timer (live time)
- ➔ M 0x90a800ac, 4 //TID trigger busy timer (dead time)

9.8 Data Readout:

- ➔ M 0x80300100,4 //A32 readout; or
- ➔ tidRead(slot, nwords) //readout nwords from TI; or
- ➔ tidBERead(slot) // readout a block, and using Bus_error to terminate the read; or
- ➔ ……

10. Citations:

Works Cited

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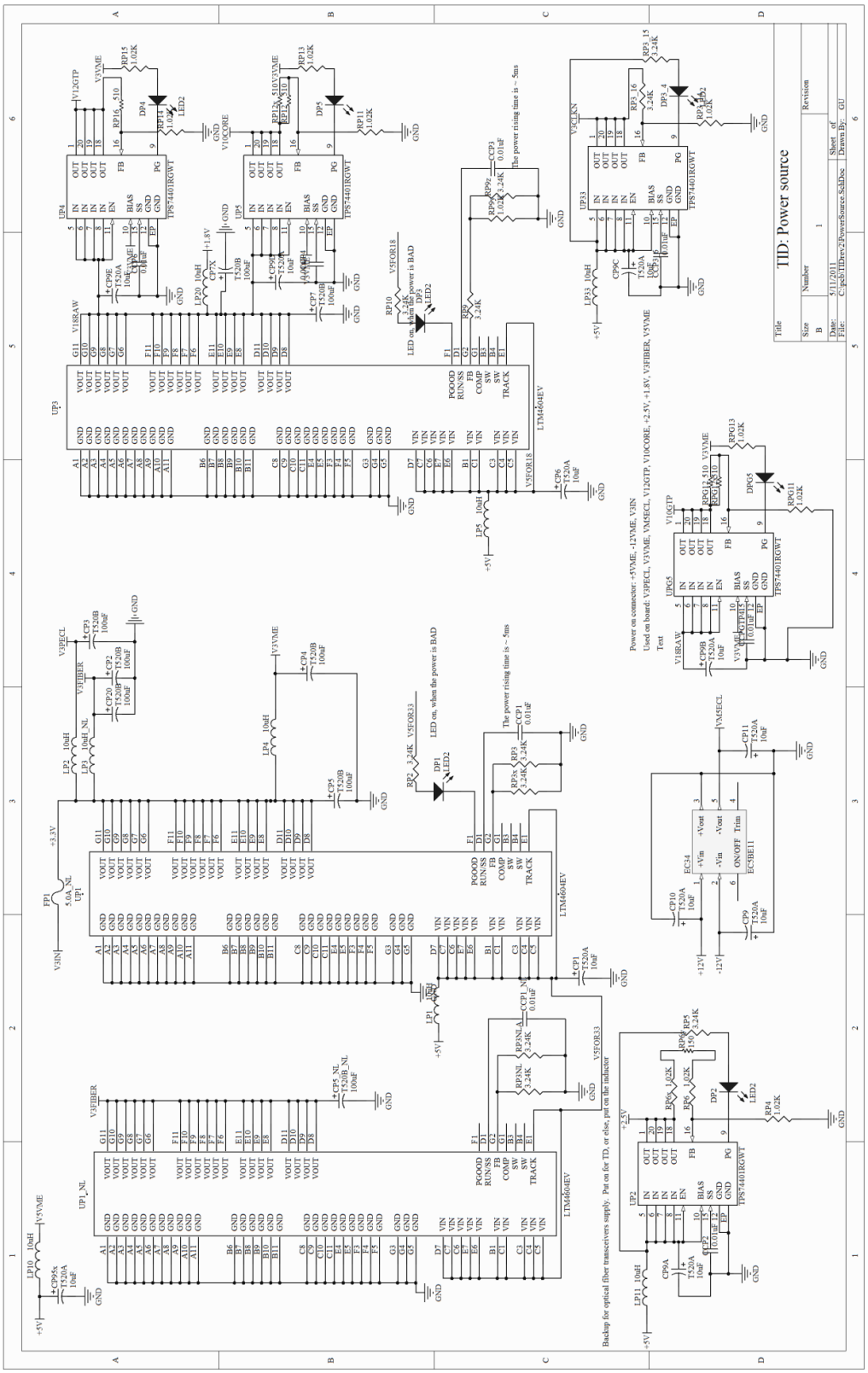
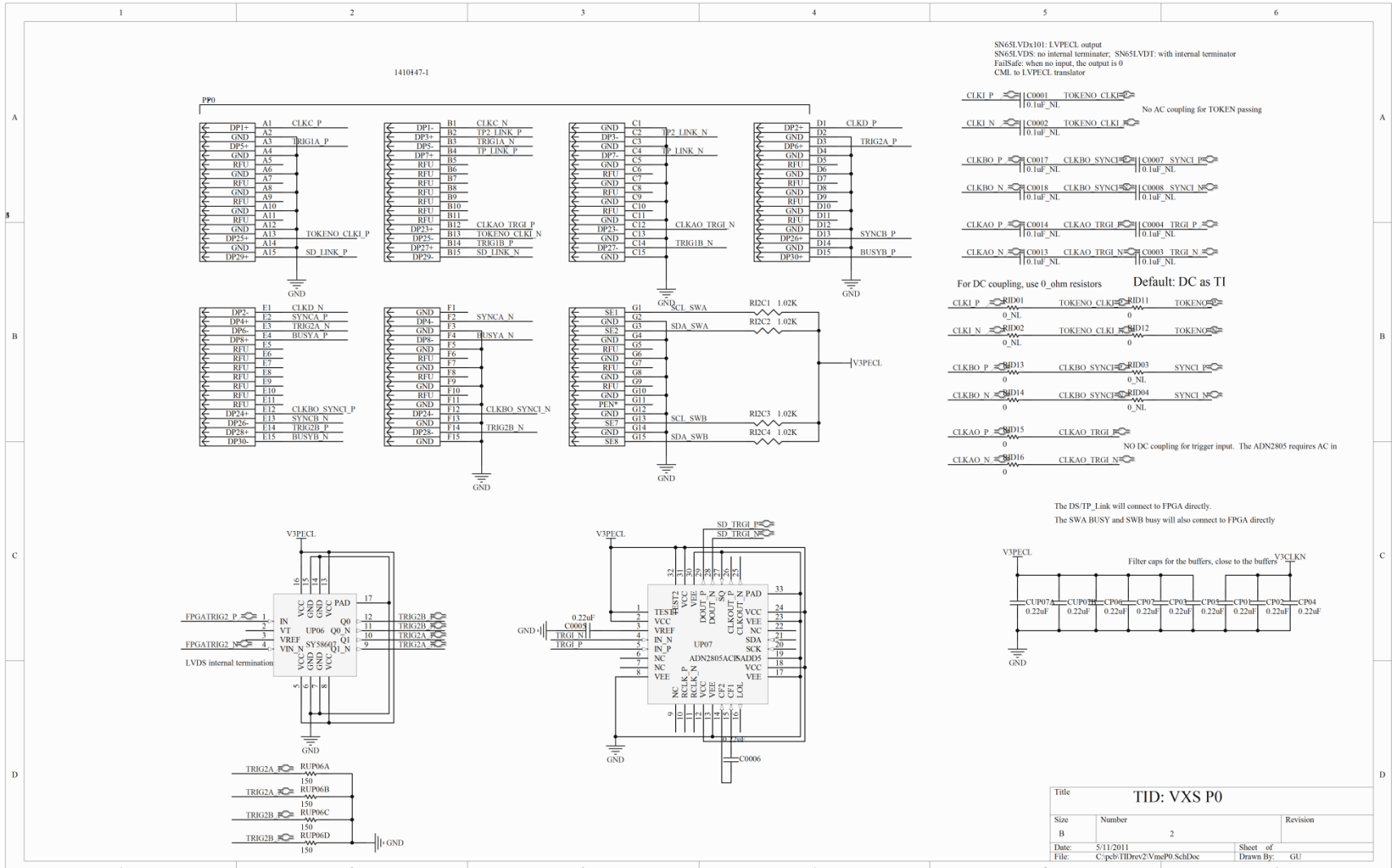
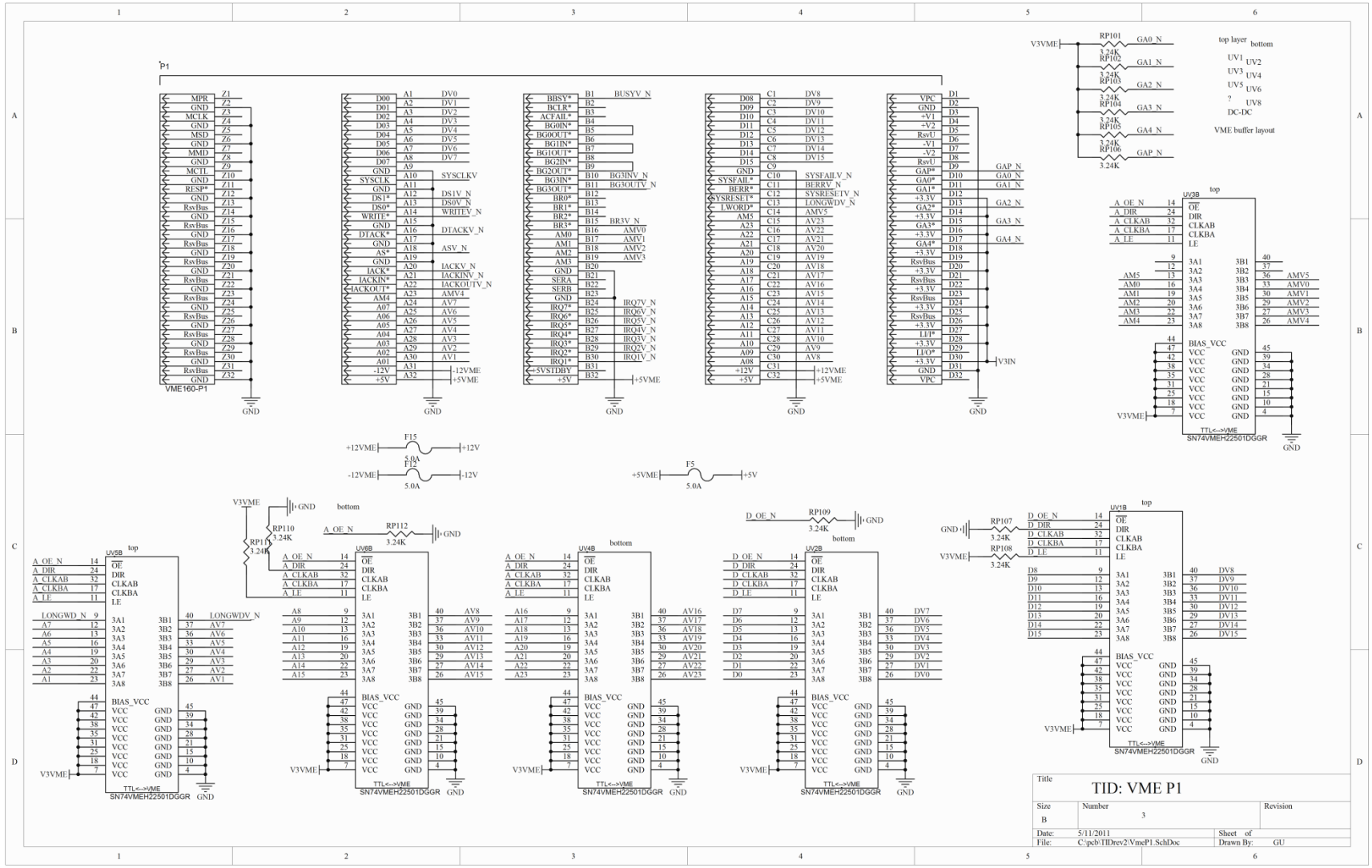
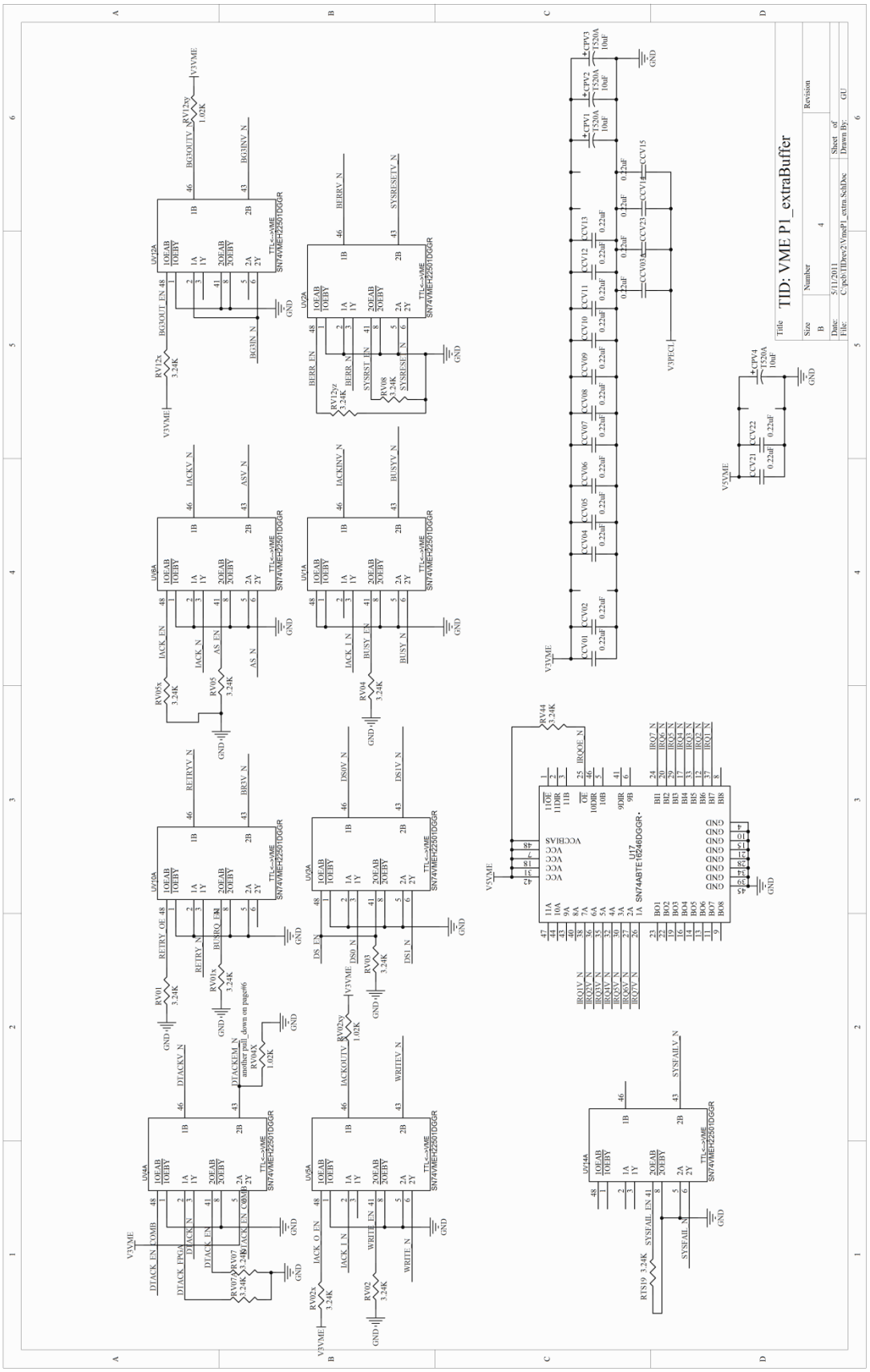
GU. (2010). Optical transceiver jitter measurement., (pp. 1-12).
Raydo, B. (2008). Trigger Distribution board., (pp. 1-10).
GU, (2010). VME to JTAG implementation
GU, (2010). VME to I2C implementation

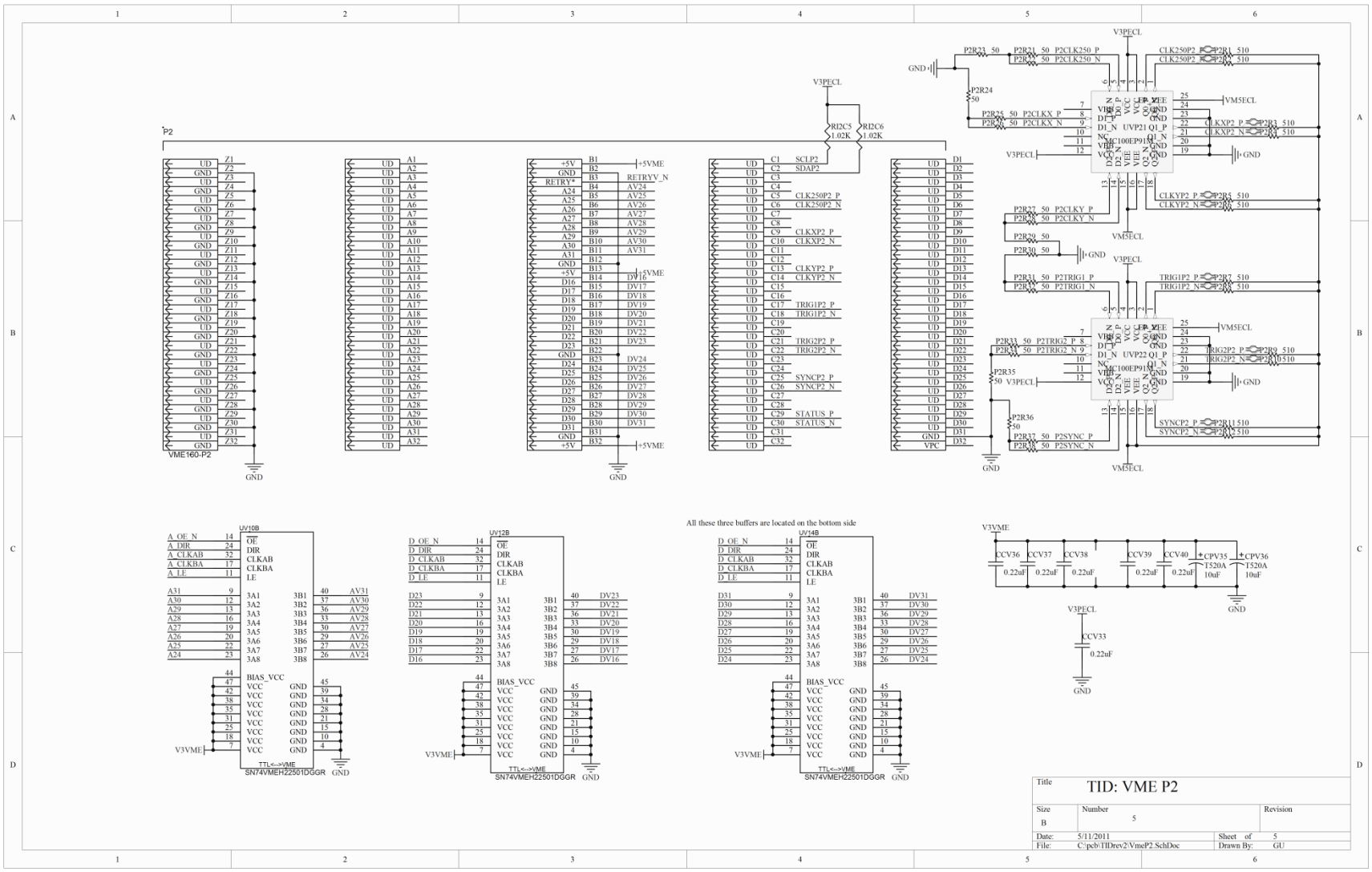
Appendix A: TID Schematics:

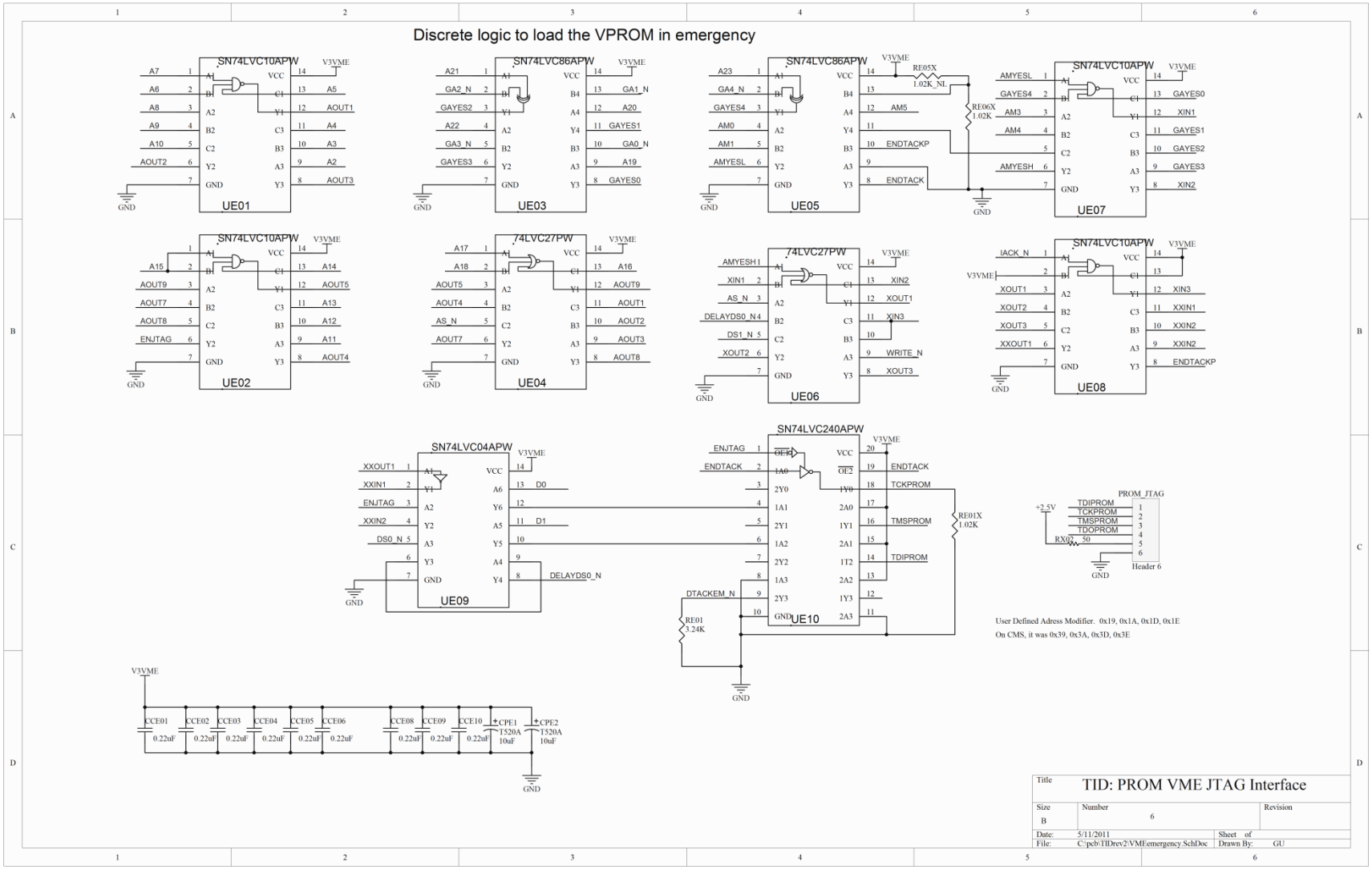


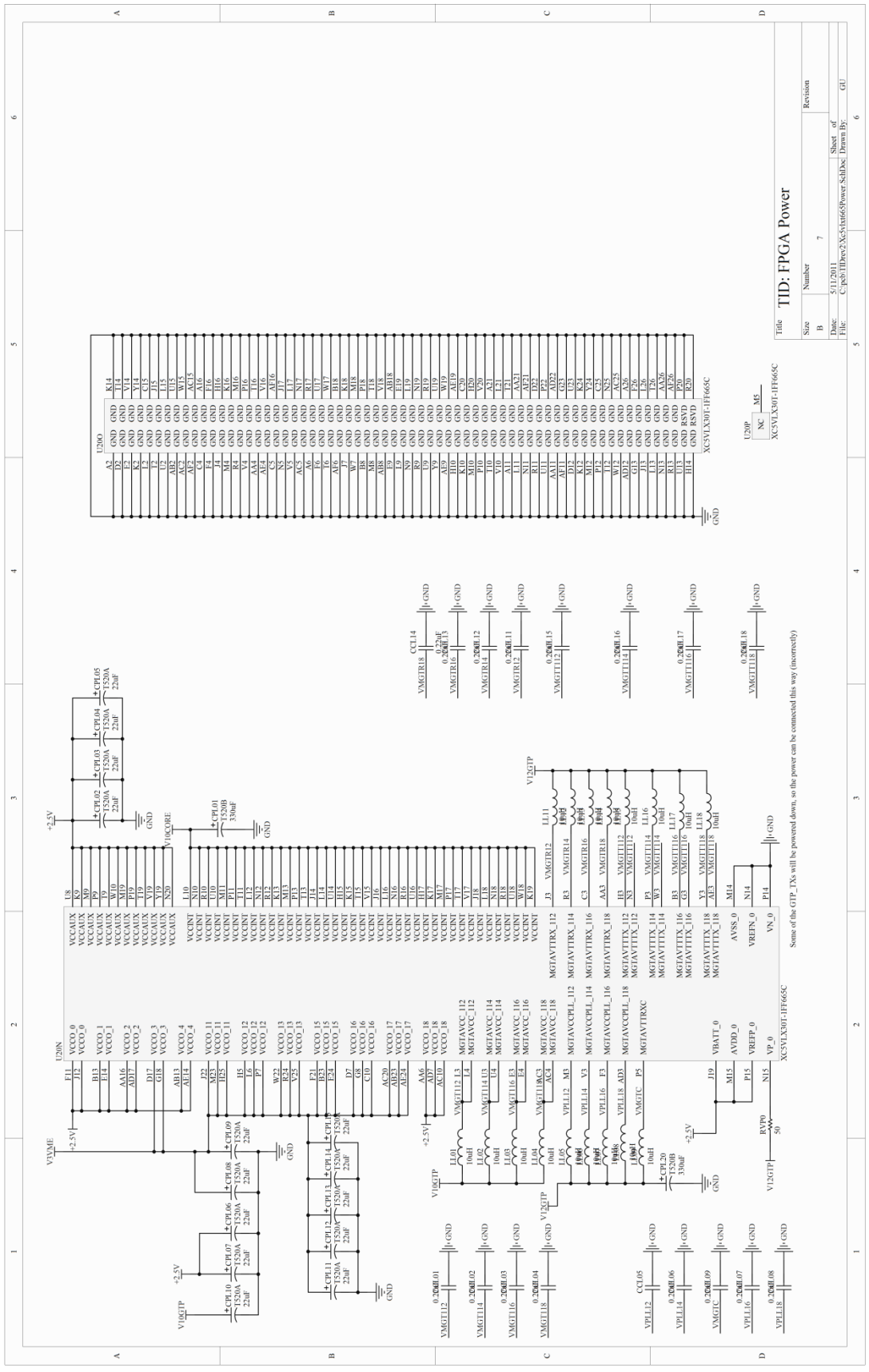

1410147-1
PP0
SN65LVDx101: LVPECL output
SN65LVDS: no internal terminater; SN65LVDT: with internal terminator
FailSafe: when no input, the output is 0
CML to LVPECL translator
No AC coupling for TOKEN passing
For DC coupling, use 0_ohm resistors
Default: DC as TI
NO DC coupling for trigger input. The ADN2805 requires AC in
The DS/TP_Link will connect to FPGA directly.
The SWA BUSY and SWB busy will also connect to FPGA directly
Filter caps for the buffers, close to the buffers
LVDS internal termination
V3PECL
GND
Title
TID: VXS P0
Size
B
Number
2
Revision
Date: 5/11/2011
Sheet of
File: C:\pcb\TIDrev2\VmeP0.SchDoc
Drawn By: GU

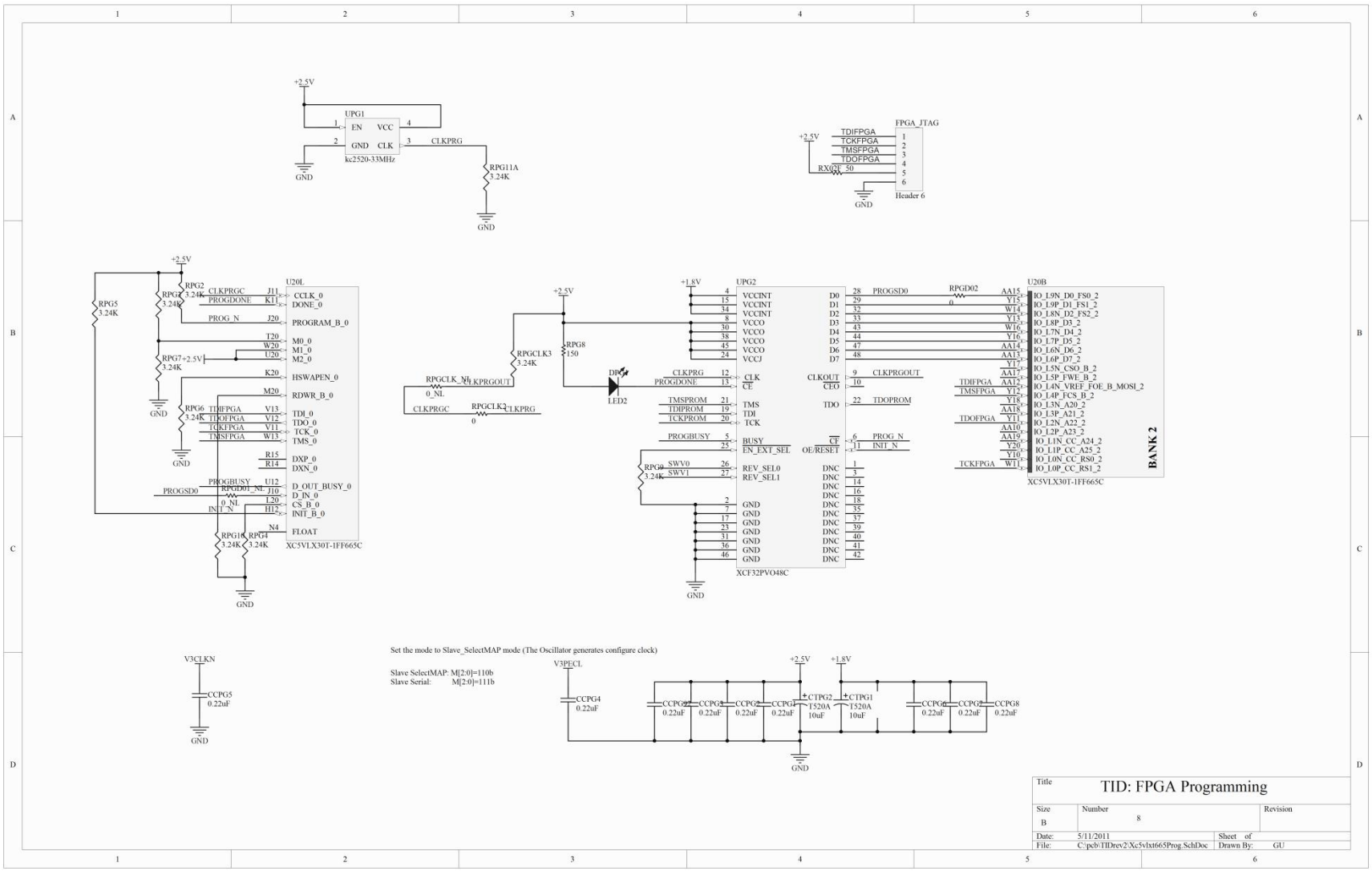

P1
VME160-P1
MPR
MCLK
MSD
MMD
MCTL
RESP*
SYSCLK
DS1*
DS0*
WRITE*
DTACK*
AS*
IACK*
IACKIN*
IACKOUT*
SYSCLKV
DS1V_N
DS0V_N
WRITEV_N
DTACKV_N
ASV_N
IACKV_N
IACKINV_N
IACKOUTV_N
BUSYV_N
BG3INV_N
BG3OUTV_N
IRQ7V_N
IRQ6V_N
IRQ5V_N
IRQ4V_N
IRQ3V_N
IRQ2V_N
IRQ1V_N
SYSFAILV_N
BERRV_N
SYSRESETV_N
LONGWDV_N
GAP_N
GA0_N
GA1_N
GA2_N
GA3_N
GA4_N
V3IN
+12VME
+5VME
-12VME
GND
F15
F13
F5
5.0A
+12V
-12V
+5V
RP101
RP102
RP103
RP104
RP105
RP106
3.24K
V3VME
top layer
bottom
UV1
UV2
UV3
UV4
UV5
UV6
UV8
DC-DC
VME buffer layout
UV3B
UV5B
UV6B
UV4B
UV2B
UV1B
top
bottom
SN74VMEH22501DGGR
TTL<->VME
BIAS_VCC
RP107
RP108
RP109
RP110
RP111
RP112
Title
TID: VME P1
Size
B
Number
3
Revision
Date:
5/11/2011
Sheet of
File:
C:\pcb\TIDrev2\VmeP1.SchDoc
Drawn By:
GU

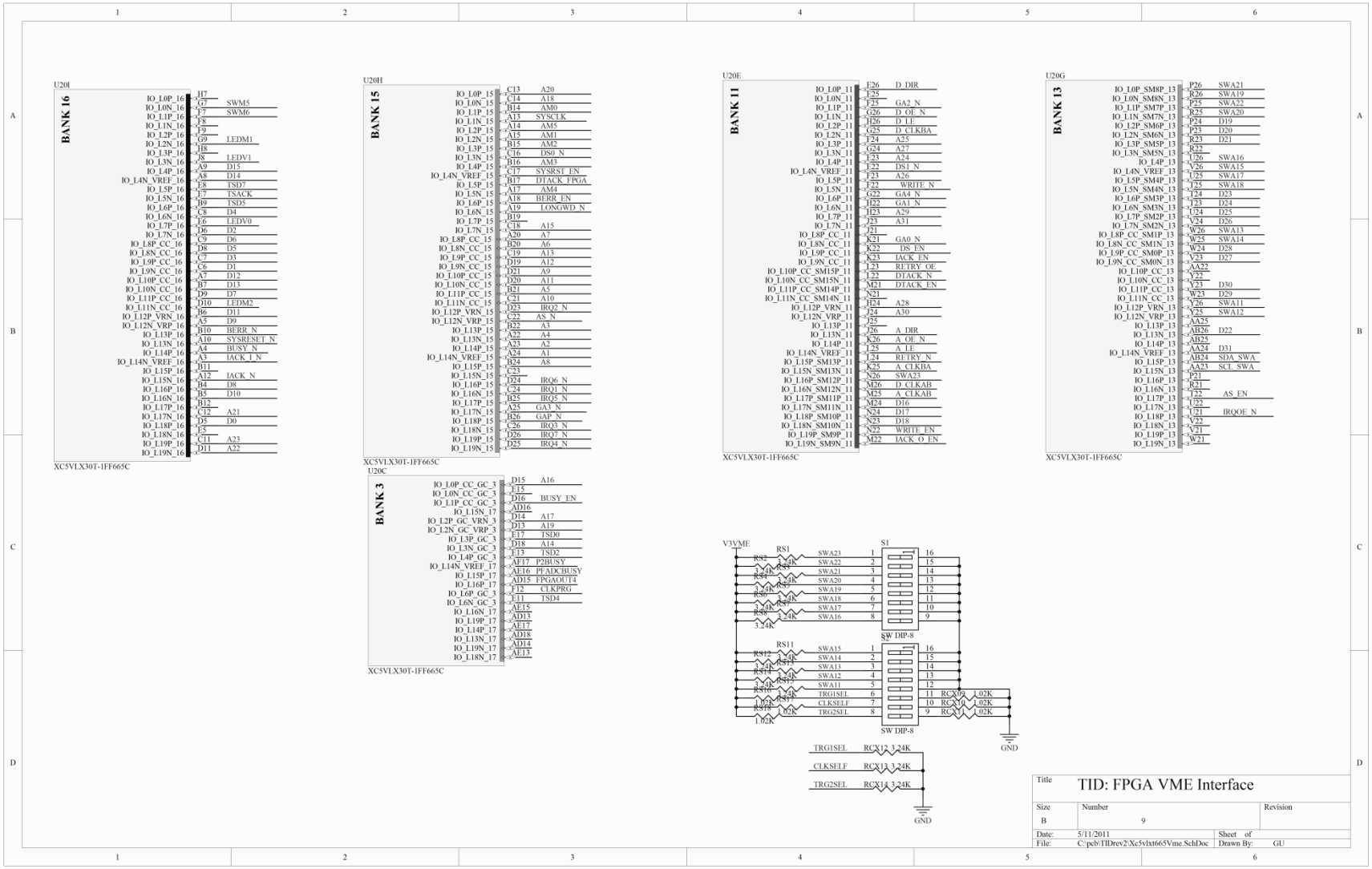

TID: VME P1_extraBuffer
Size
B
Number
4
Revision
Date: 5/11/2011
File: C:\pcb\TIDvec2\VmeP1_extra.SchDoc
Sheet of
Drawn By:
GU
SN74VME H22501DGGR
SN74ABTE16245DGGR
V3VME
V5VME
GND

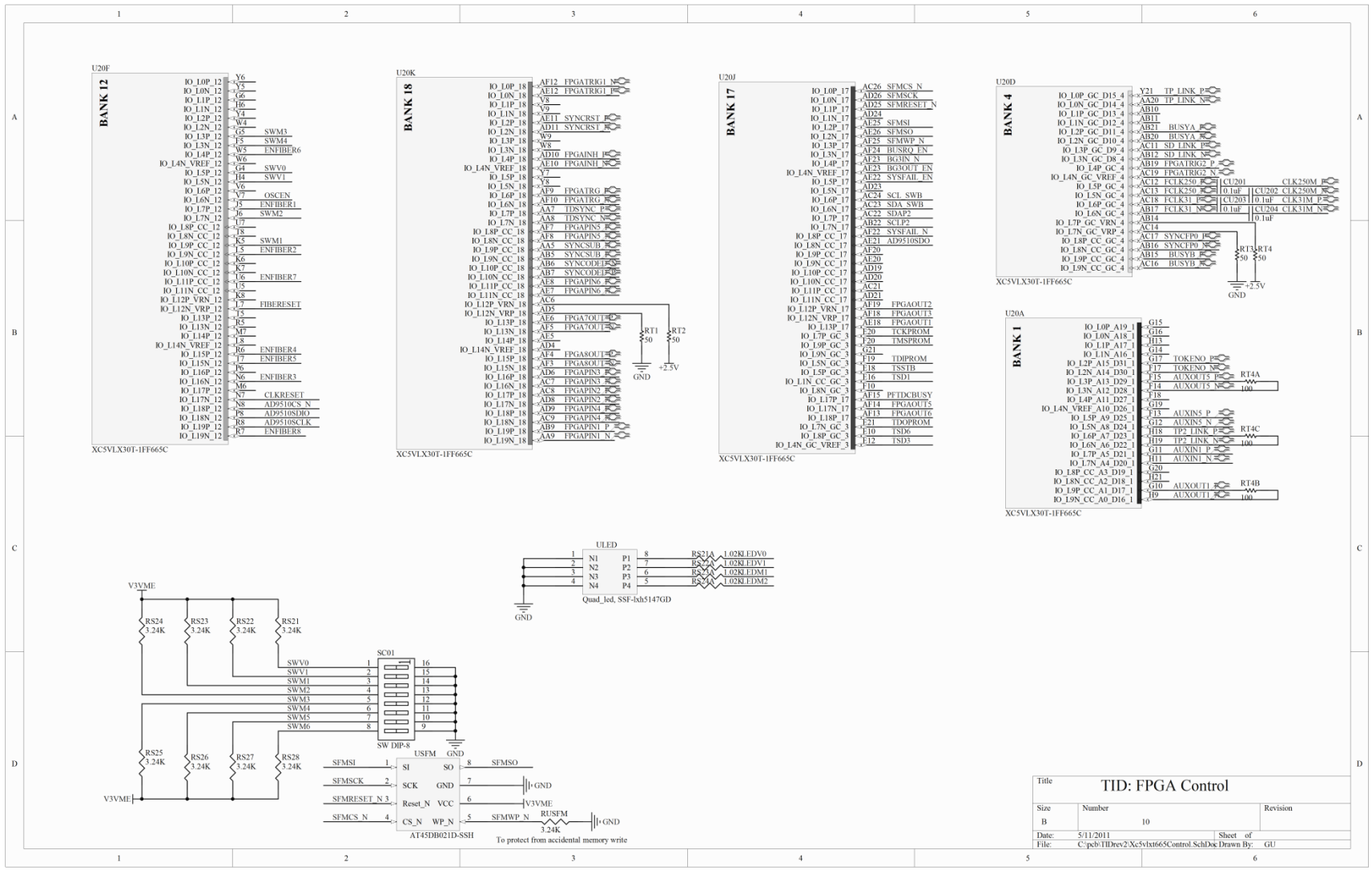

P2
VME160-P2
All these three buffers are located on the bottom side
UV10B
UV12B
UV14B
SN74VMEH22501DGGR
TTL<->VME
V3PECL
V3VME
VM5ECL
GND
TID: VME P2
Size
B
Number
5
Revision
Date: 5/11/2011
Sheet of 5
File: C:\pcb\TIDrev2\VmeP2.SchDoc
Drawn By: GU

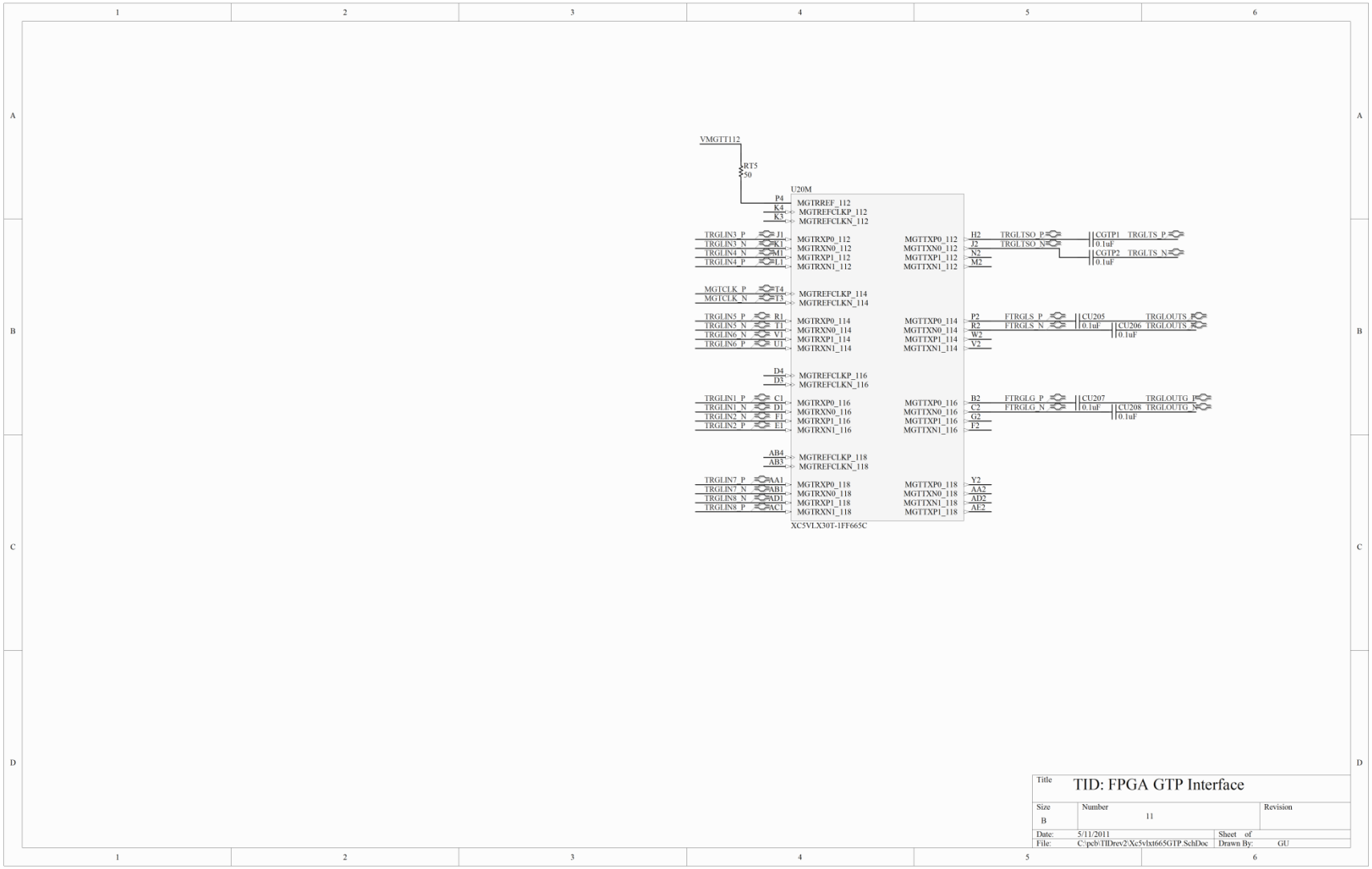

Discrete logic to load the VPROM in emergency
SN74LVC10APW
UE01
SN74LVC86APW
UE03
SN74LVC86APW
UE05
SN74LVC10APW
UE07
SN74LVC10APW
UE02
74LVC27PW
UE04
74LVC27PW
UE06
SN74LVC10APW
UE08
SN74LVC04APW
UE09
SN74LVC240APW
UE10
V3VME
GND
RE05X 1.02K_NL
RE06X 1.02K
RE01X 1.02K
RE01 3.24K
PROM_JTAG
TDIPROM
TCKPROM
TMSPROM
TDOPROM
Header 6
User Defined Adress Modifier. 0x19, 0x1A, 0x1D, 0x1E
On CMS, it was 0x39, 0x3A, 0x3D, 0x3E
CCE01 0.22uF
CCE02 0.22uF
CCE03 0.22uF
CCE04 0.22uF
CCE05 0.22uF
CCE06 0.22uF
CCE08 0.22uF
CCE09 0.22uF
CCE10 0.22uF
CPE1 1520A 10uF
CPE2 1520A 10uF
Title TID: PROM VME JTAG Interface
Size B
Number 6
Revision
Date: 5/11/2011
Sheet of
File: C:\pcb\TIDrev2\VMEemergency.SchDoc
Drawn By: GU

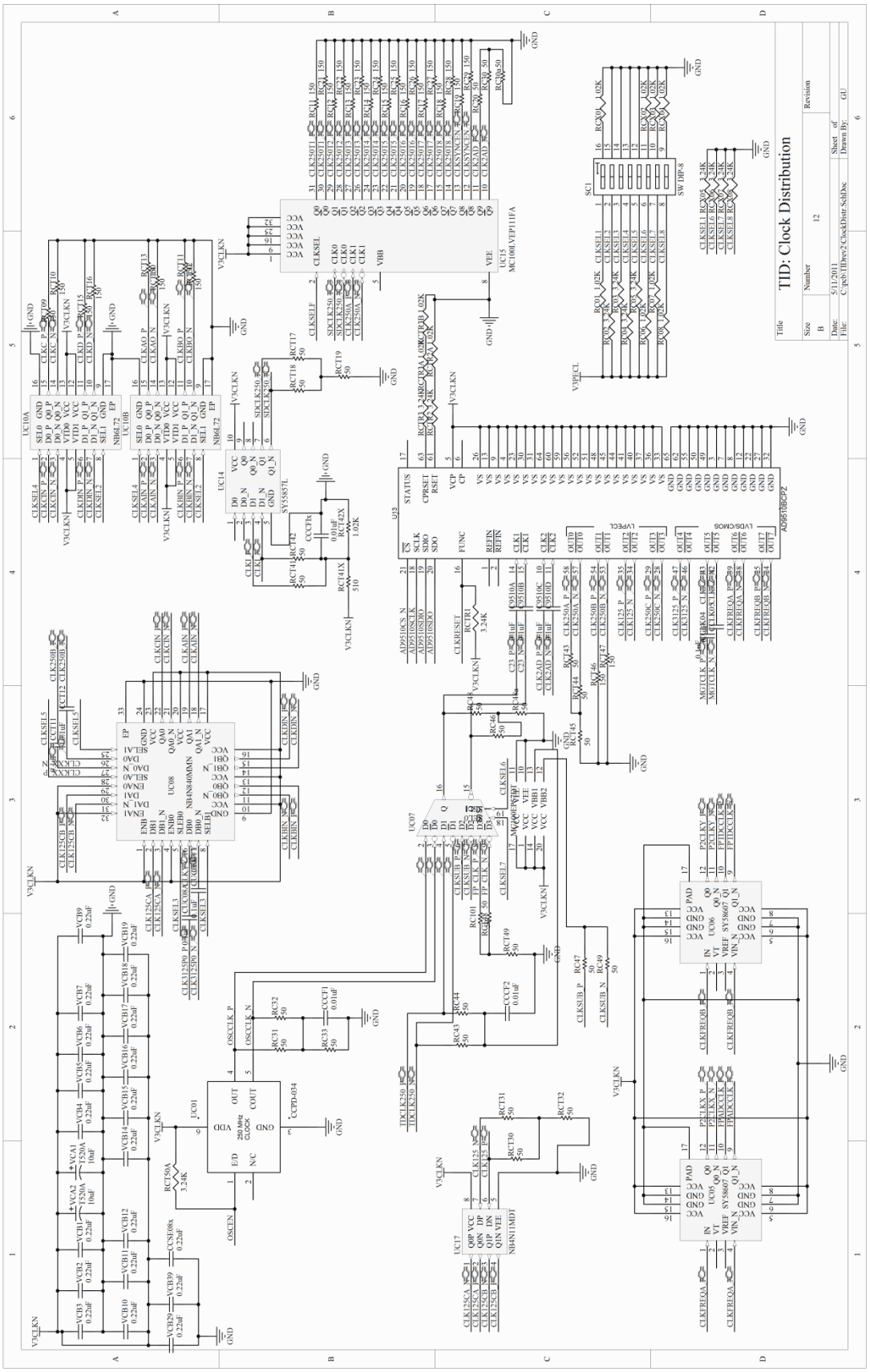

TID: FPGA Power
XC5VLX30T-1FF665C
Some of the GTP_TXs will be powered down, so the power can be connected this way (incorrectly)

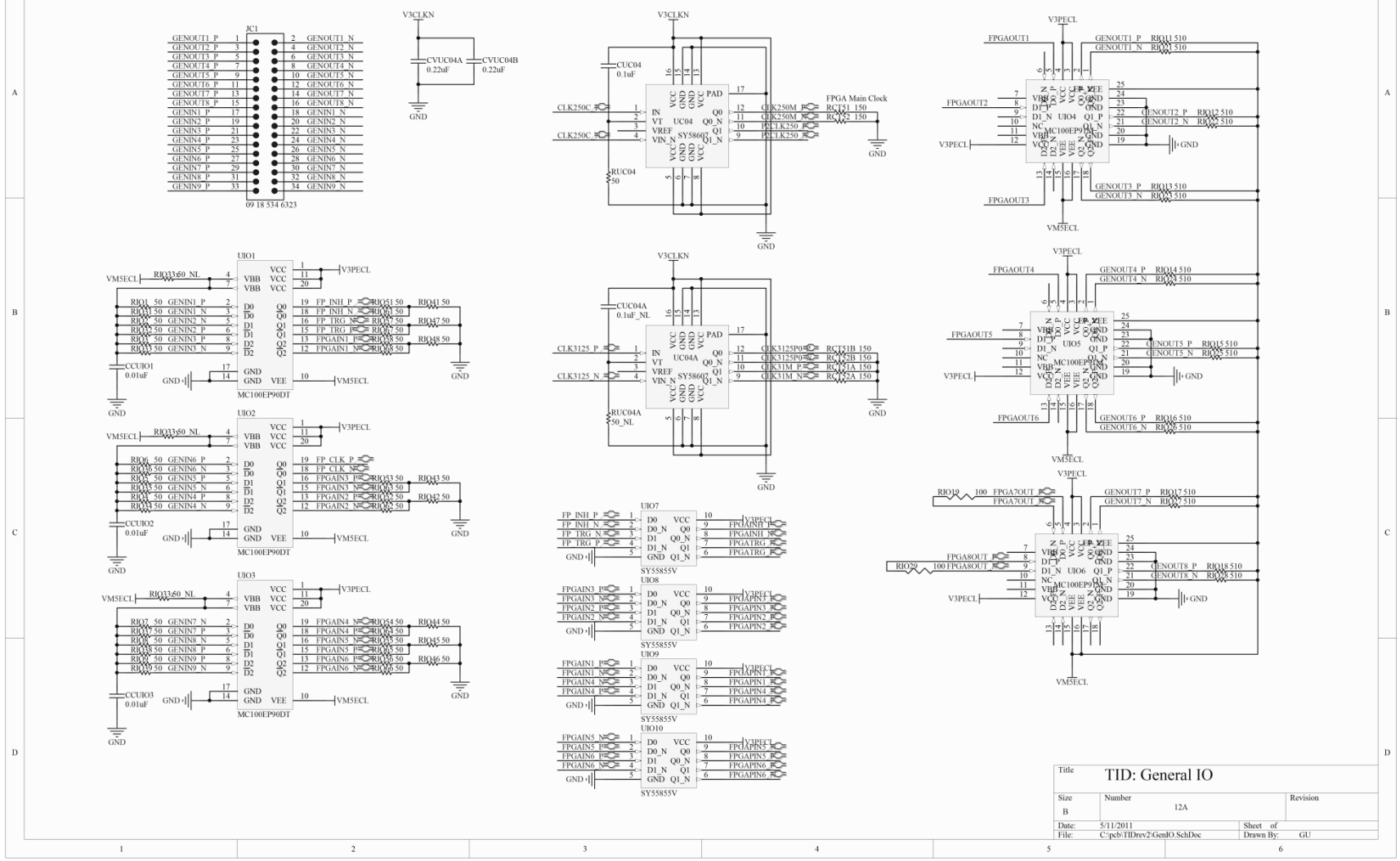

+2.5V
UPG1
EN
VCC
GND
CLK
kc2520-33MHz
CLKPRG
RPG11A
3.24K
GND
FPGA_JTAG
TDIFPGA
TCKFPGA
TMSFPGA
TDOFPGA
RX03E 50
Header 6
U20L
RPG2
RPG5
RPG7
RPG6
RPG1
RPG4
CLKPRGC
PROGDONE
PROG_N
M0_0
M1_0
M2_0
HSWAPEN_0
RDWR_B_0
TDI_0
TDO_0
TCK_0
TMS_0
DXP_0
DXN_0
D_OUT_BUSY_0
D_IN_0
CS_B_0
INIT_B_0
FLOAT
XC5VLX30T-1FF665C
U20B
BANK 2
XC5VLX30T-1FF665C
UPG2
VCCINT
VCCO
VCCJ
CLKPRG
PROGDONE
TMSPROM
TDIPROM
TCKPROM
PROGBUSY
EN_EXT_SEL
REV_SEL0
REV_SEL1
GND
DNC
CLK
CE
TMS
TDI
TCK
BUSY
OE/RESET
CLKOUT
CEO
TDO
CF
PROGSD0
CLKPRGOUT
TDOPROM
PROG_N
INIT_N
XCF32PVO48C
RPGCLK3
RPGCLK_NL
RPGCLK2
RPG8
150
LED2
RPG9
SWV0
SWV1
RPGD02
V3CLKN
CCPG5
0.22uF
Set the mode to Slave_SelectMAP mode (The Oscillator generates configure clock)
Slave SelectMAP: M[2:0]=110b
Slave Serial: M[2:0]=111b
V3PECL
CCPG4
CCPG1
CCPG2
CCPG3
CCPG6
CCPG7
CCPG8
CTPG2
CTPG1
T520A
10uF
Title
TID: FPGA Programming
Size
B
Number
8
Revision
Date:
5/11/2011
Sheet of
File:
C:\pcb\TIDrev2\Xc5vlx665Prog.SchDoc
Drawn By:
GU

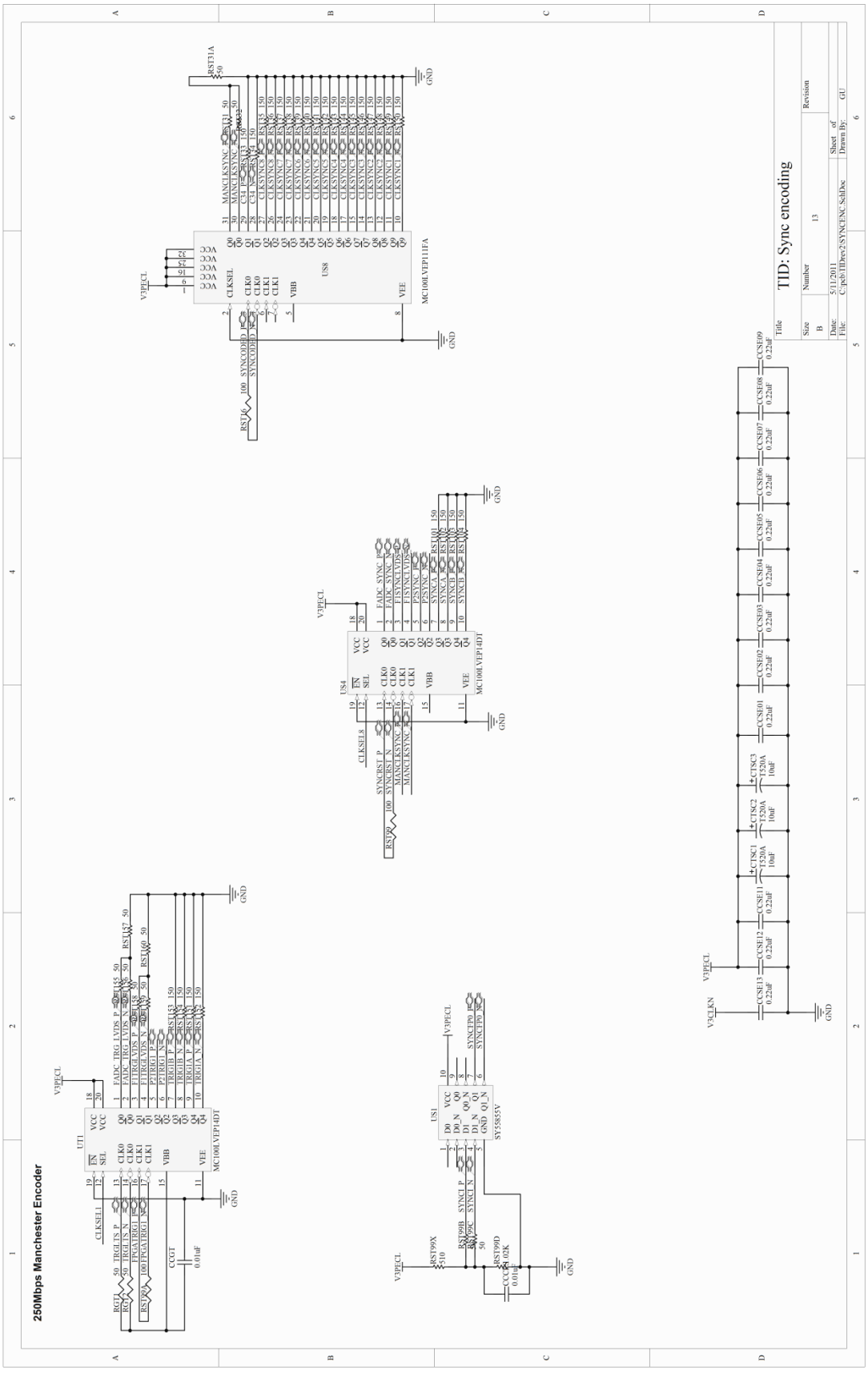

U20I
BANK 16
XC5VLX30T-1FF665C
U20H
BANK 15
XC5VLX30T-1FF665C
U20C
BANK 3
XC5VLX30T-1FF665C
U20E
BANK 11
XC5VLX30T-1FF665C
U20G
BANK 13
XC5VLX30T-1FF665C
V3VME
RS1
S1
SW DIP-8
RS11
SW DIP-8
GND
TRG1SEL
CLKSELF
TRG2SEL
GND
Title
TID: FPGA VME Interface
Size
B
Number
9
Revision
Date: 5/11/2011
Sheet of
File: C:\pcb\TIDrev2\Xc5vlxt665Vme.SchDoc
Drawn By: GU

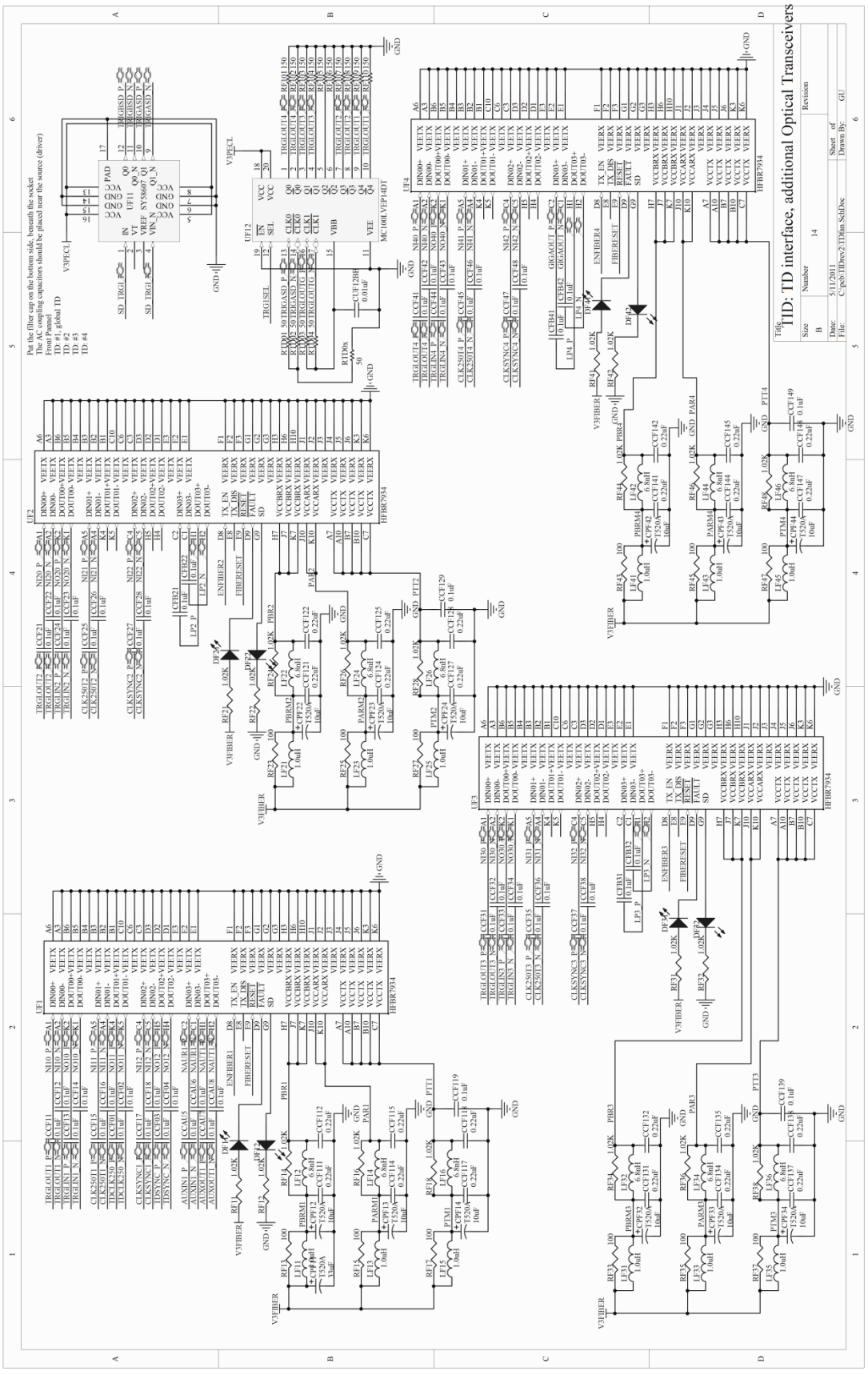

U20F
BANK 12
XC5VLX30T-1FF665C
U20K
BANK 18
XC5VLX30T-1FF665C
U20J
BANK 17
XC5VLX30T-1FF665C
U20D
BANK 4
XC5VLX30T-1FF665C
U20A
BANK 1
XC5VLX30T-1FF665C
ULED
Quad_led, SSF-lxh5147GD
SC01
SW DIP-8
V3VME
USFM
AT45DB021D-SSH
To protect from accidental memory write
Title
TID: FPGA Control
Size
B
Number
10
Revision
Date: 5/11/2011
Sheet of
File: C:\pcb\TIDrev2\Xc5vlxt665Control.SchDoc
Drawn By: GU

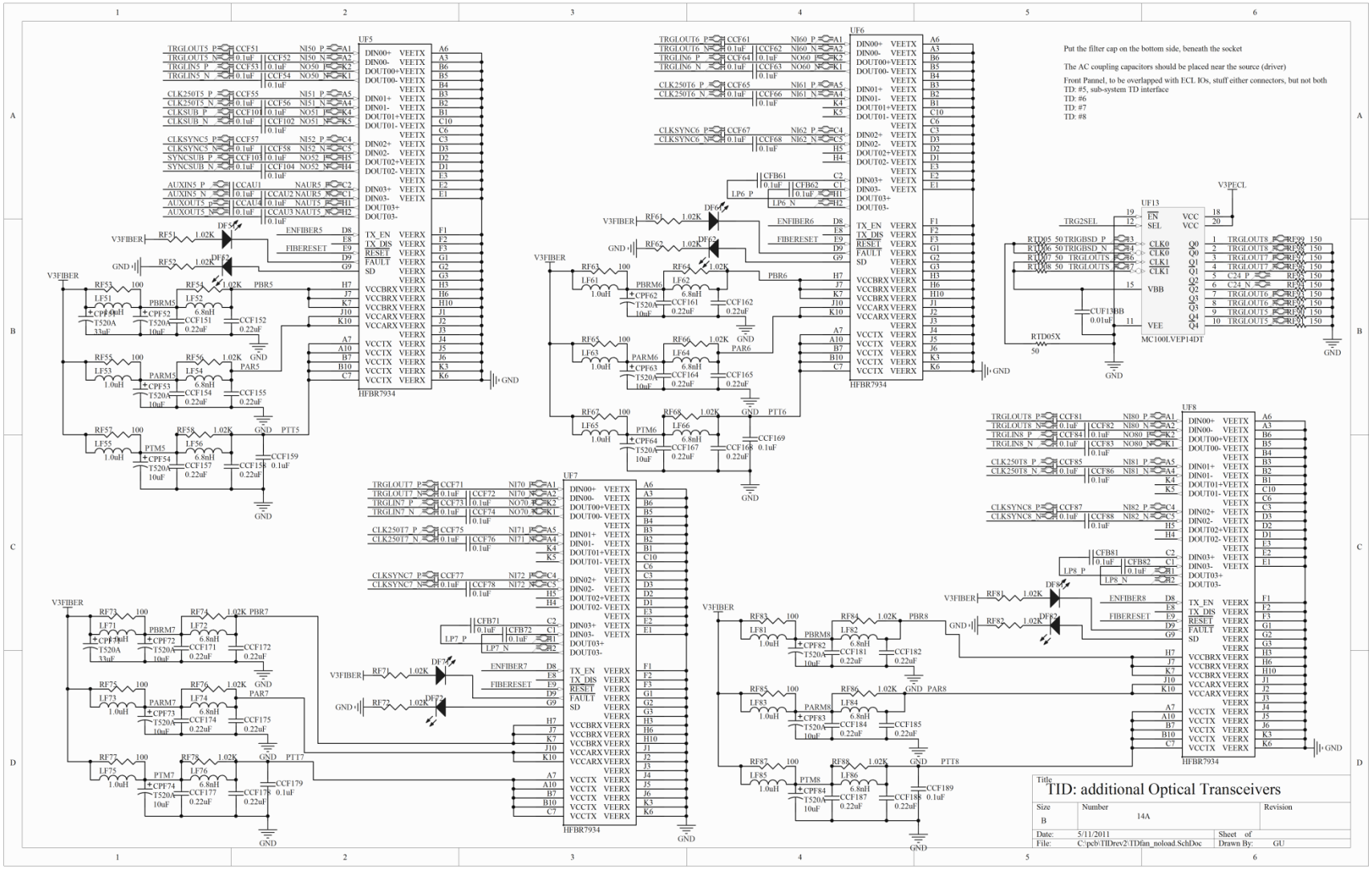

VMGTT112
RT5
50
U20M
P4 MGTRREF_112
K4 MGTREFCLKP_112
K3 MGTREFCLKN_112
TRGLIN3_P J1 MGTRXP0_112
TRGLIN3_N K1 MGTRXN0_112
TRGLIN4_N M1 MGTRXP1_112
TRGLIN4_P L1 MGTRXN1_112
MGTTXP0_112 H2 TRGLTSO_P
MGTTXN0_112 J2 TRGLTSO_N
MGTTXP1_112 N2
MGTTXN1_112 M2
CGTP1 TRGLTS_P
0.1uF
CGTP2 TRGLTS_N
0.1uF
MGTCLK_P T4 MGTREFCLKP_114
MGTCLK_N T3 MGTREFCLKN_114
TRGLIN5_P R1 MGTRXP0_114
TRGLIN5_N T1 MGTRXN0_114
TRGLIN6_N V1 MGTRXP1_114
TRGLIN6_P U1 MGTRXN1_114
MGTTXP0_114 P2 FTRGLS_P
MGTTXN0_114 R2 FTRGLS_N
MGTTXP1_114 W2
MGTTXN1_114 V2
CU205 TRGLOUTS_P
0.1uF
CU206 TRGLOUTS_N
0.1uF
D4 MGTREFCLKP_116
D3 MGTREFCLKN_116
TRGLIN1_P C1 MGTRXP0_116
TRGLIN1_N D1 MGTRXN0_116
TRGLIN2_N F1 MGTRXP1_116
TRGLIN2_P E1 MGTRXN1_116
MGTTXP0_116 B2 FTRGLG_P
MGTTXN0_116 C2 FTRGLG_N
MGTTXP1_116 G2
MGTTXN1_116 F2
CU207 TRGLOUTG_P
0.1uF
CU208 TRGLOUTG_N
0.1uF
AB4 MGTREFCLKP_118
AB3 MGTREFCLKN_118
TRGLIN7_P AA1 MGTRXP0_118
TRGLIN7_N AB1 MGTRXN0_118
TRGLIN8_N AD1 MGTRXP1_118
TRGLIN8_P AC1 MGTRXN1_118
MGTTXP0_118 Y2
MGTTXN0_118 AA2
MGTTXN1_118 AD2
MGTTXP1_118 AE2
XC5VLX30T-1FF665C
Title TID: FPGA GTP Interface
Size B
Number 11
Revision
Date: 5/11/2011
Sheet of
File: C:\pcb\TIDrev2\Xc5vlx665GTP.SchDoc
Drawn By: GU

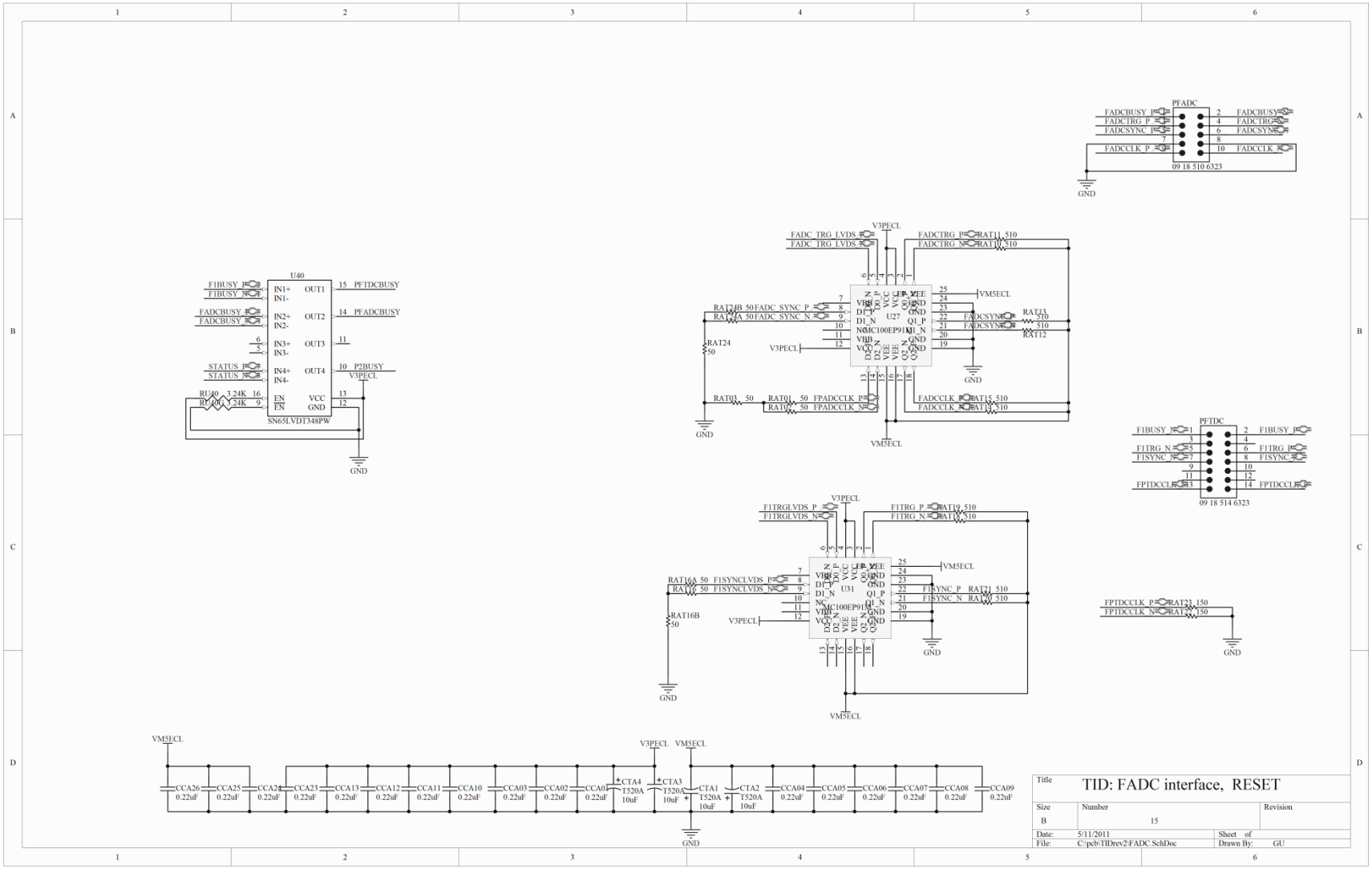

Title
TTD: Clock Distribution
Size
B
Number
12
Revision
Date:
5/11/2011
Sheet of
File:
C:\pcb\TIDrev2\ClockDistr.SchDoc
Drawn By:
GU

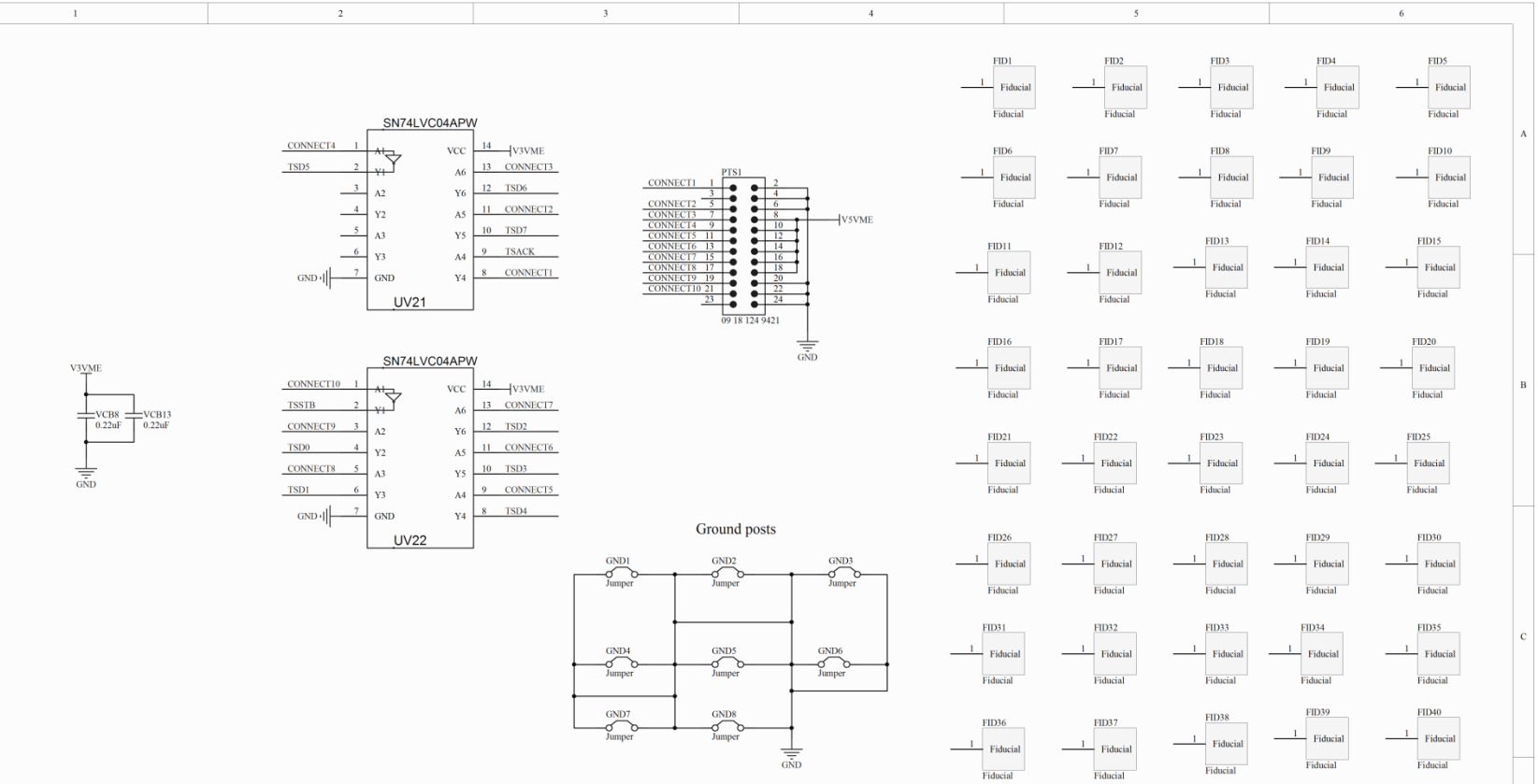

JC1
GENOUT1_P 1
GENOUT2_P 3
GENOUT3_P 5
GENOUT4_P 7
GENOUT5_P 9
GENOUT6_P 11
GENOUT7_P 13
GENOUT8_P 15
GENIN1_P 17
GENIN2_P 19
GENIN3_P 21
GENIN4_P 23
GENIN5_P 25
GENIN6_P 27
GENIN7_P 29
GENIN8_P 31
GENIN9_P 33
2 GENOUT1_N
4 GENOUT2_N
6 GENOUT3_N
8 GENOUT4_N
10 GENOUT5_N
12 GENOUT6_N
14 GENOUT7_N
16 GENOUT8_N
18 GENIN1_N
20 GENIN2_N
22 GENIN3_N
24 GENIN4_N
26 GENIN5_N
28 GENIN6_N
30 GENIN7_N
32 GENIN8_N
34 GENIN9_N
09 18 534 6323
V3CLKN
CVUC04A 0.22uF
CVUC04B 0.22uF
GND
V3CLKN
CUC04 0.1uF
CLK250C_P
CLK250C_N
RUC04 50
IN VT VREF VIN_N VCC GND GND VCC PAD Q0 Q0_N Q1 Q1_N SY58602U
CLK250M_P
CLK250M_N
PCLK250_P
PCLK250_N
RC1251 150
RC1252 150
FPGA Main Clock
GND
V3CLKN
CUC04A 0.1uF_NL
CLK3125_P
CLK3125_N
RUC04A 50_NL
IN VT VREF VIN_N VCC GND GND VCC PAD Q0 Q0_N Q1 Q1_N SY58602U
CLK3125P0_P
CLK3125P0_N
CLK31M_P
CLK31M_N
RC1251B 150
RC1252B 150
RC1251A 150
RC1252A 150
GND
V3PECL
FPGAOUT1
FPGAOUT2
FPGAOUT3
GENOUT1_P RIO11 510
GENOUT1_N RIO10 510
GENOUT2_P RIO12 510
GENOUT2_N RIO13 510
GENOUT3_P RIO13 510
GENOUT3_N RIO14 510
MC100EP90DT
VM5ECL
FPGAOUT4
FPGAOUT5
FPGAOUT6
GENOUT4_P RIO14 510
GENOUT4_N RIO15 510
GENOUT5_P RIO15 510
GENOUT5_N RIO16 510
GENOUT6_P RIO16 510
GENOUT6_N RIO17 510
RIO19 100 FPGA7OUT_P
FPGA7OUT_N
FPGA8OUT_P
FPGA8OUT_N
RIO20 100 FPGA8OUT_N
GENOUT7_P RIO17 510
GENOUT7_N RIO18 510
GENOUT8_P RIO18 510
GENOUT8_N RIO19 510
UIO1
UIO2
UIO3
VM5ECL
RIO33 50_NL
V3PECL
RIO1_50 GENIN1_P
RIO0_50 GENIN1_N
RIO2_50 GENIN2_N
RIO3_50 GENIN2_P
RIO4_50 GENIN3_P
RIO5_50 GENIN3_N
RIO6_50 GENIN6_P
RIO7_50 GENIN6_N
RIO8_50 GENIN5_P
RIO9_50 GENIN5_N
RIO10_50 GENIN4_P
RIO11_50 GENIN4_N
RIO7_50 GENIN7_N
RIO6_50 GENIN7_P
RIO9_50 GENIN8_N
RIO8_50 GENIN8_P
RIO11_50 GENIN9_P
RIO10_50 GENIN9_N
FP_INH_P
FP_INH_N
FP_TRG_N
FP_TRG_P
FP_CLK_P
FP_CLK_N
FPGAIN1_P
FPGAIN1_N
FPGAIN2_P
FPGAIN2_N
FPGAIN3_P
FPGAIN3_N
FPGAIN4_P
FPGAIN4_N
FPGAIN5_P
FPGAIN5_N
FPGAIN6_P
FPGAIN6_N
RIO51 50
RIO50 50
RIO49 50
RIO48 50
RIO53 50
RIO52 50
RIO55 50
RIO54 50
RIO41 50
RIO47 50
RIO43 50
RIO42 50
RIO44 50
RIO45 50
RIO46 50
CCUIO1 0.01uF
CCUIO2 0.01uF
CCUIO3 0.01uF
D0 D0 D1 D1 D2 D2 Q0 Q0 Q1 Q1 Q2 Q2
GND GND VEE
MC100EP90DT
UIO7
UIO8
UIO9
UIO10
FPGAPINH_P
FPGAPINH_N
FPGATRG_N
FPGATRG_P
FPGAPIN3_P
FPGAPIN3_N
FPGAPIN2_P
FPGAPIN2_N
FPGAPIN1_P
FPGAPIN1_N
FPGAPIN4_P
FPGAPIN4_N
FPGAPIN5_P
FPGAPIN5_N
FPGAPIN6_P
FPGAPIN6_N
D0 D0_N D1 D1_N GND VCC Q0 Q0_N Q1 Q1_N
SY55855V
Title
TID: General IO
Size B
Number 12A
Revision
Date: 5/11/2011
Sheet of
File: C:\pcb\TIDrev2\GenIO.SchDoc
Drawn By: GU


250Mbps Manchester Encoder
TTID: Sync encoding
MC100LVEP111FA
MC100LVEP14DT
SY55855V
V3PECL
V2CLKN
GND
CLKSEL1
CLKSEL8
SYNCRST_P
SYNCRST_N
MANCLKSYNC_P
MANCLKSYNC_N
SYNCOEID
SYNCI_P
SYNCI_N
SYNCP0_P
SYNCP0_N
TRGLTS_P
TRGLTS_N
FPGATRIG1_P
FPGATRIG1_N
Size
B
Number
13
Revision
Date: 5/11/2011
Sheet of
File: C:\pcb\TIDsvn2\SYNCENC.SchDoc
Drawn By: GU


TID: TD interface, additional Optical Transceivers


Put the filter cap on the bottom side, beneath the socket
The AC coupling capacitors should be placed near the source (driver)
Front Pannel, to be overlapped with ECL IOs, stuff either connectors, but not both
TD: #5, sub-system TD interface
TD: #6
TD: #7
TD: #8
UF5
UF6
UF7
UF8
UF13
HFBR7934
MC100LVEP14DT
V3FIBER
V3PECL
GND
PAR5
PAR6
PAR7
PAR8
PTM5
PTM6
PTM7
PTM8
PTT5
PTT6
PTT7
PTT8
TID: additional Optical Transceivers
Size B
Number 14A
Revision
Date: 5/11/2011
Sheet of
File: C:\pcb\TIDrev2\TIDfan_noload.SchDoc
Drawn By: GU


PFADC
FADCBUSY_P
FADCTRG_P
FADCSYNC_P
FADCCLK_P
FADCBUSY
FADCTRG
FADCSYNC
FADCCLK
09 18 510 6323
GND
U40
F1BUSY_P
F1BUSY_N
FADCBUSY_P
FADCBUSY_N
STATUS_P
STATUS_N
IN1+
IN1-
IN2+
IN2-
IN3+
IN3-
IN4+
IN4-
OUT1
OUT2
OUT3
OUT4
EN
EN
VCC
GND
15 PFTDCBUSY
14 PFADCBUSY
11
10 P2BUSY
13
12
RU40 3.24K
RU39 3.24K
SN65LVDT348PW
V3PECL
FADC_TRG_LVDS_P
FADC_TRG_LVDS_N
FADCTRG_P RAT11 510
FADCTRG_N RAT10 510
U27
VM5ECL
RAT24B 50 FADC_SYNC_P
RAT24A 50 FADC_SYNC_N
RAT24
50
FADCSYNC_P
FADCSYNC_N
RAT13
RAT12
510
RAT03 50
RAT01 50 FPADCCLK_P
RAT00 50 FPADCCLK_N
FADCCLK_P RAT15 510
FADCCLK_N RAT14 510
PFTDC
F1BUSY_N
F1TRG_N
F1SYNC_N
FPTDCCLK_N
F1BUSY_P
F1TRG_P
F1SYNC_P
FPTDCCLK_P
09 18 514 6323
F1TRGLVDS_P
F1TRGLVDS_N
F1TRG_P RAT19 510
F1TRG_N RAT18 510
U31
RAT16A 50 F1SYNCLVDS_P
RAT16B 50 F1SYNCLVDS_N
RAT16B
50
F1SYNC_P RAT21 510
F1SYNC_N RAT20 510
FPTDCCLK_P RAT23 150
FPTDCCLK_N RAT22 150
VM5ECL
V3PECL VM5ECL
CCA26 0.22uF
CCA25 0.22uF
CCA24 0.22uF
CCA23 0.22uF
CCA13 0.22uF
CCA12 0.22uF
CCA11 0.22uF
CCA10 0.22uF
CCA03 0.22uF
CCA02 0.22uF
CCA01 0.22uF
CTA4 T520A 10uF
CTA3 T520A 10uF
CTA1 T520A 10uF
CTA2 T520A 10uF
CCA04 0.22uF
CCA05 0.22uF
CCA06 0.22uF
CCA07 0.22uF
CCA08 0.22uF
CCA09 0.22uF
Title
TID: FADC interface, RESET
Size
B
Number
15
Revision
Date: 5/11/2011
Sheet of
File: C:\pcb\TIDrev2\FADC.SchDoc
Drawn By: GU



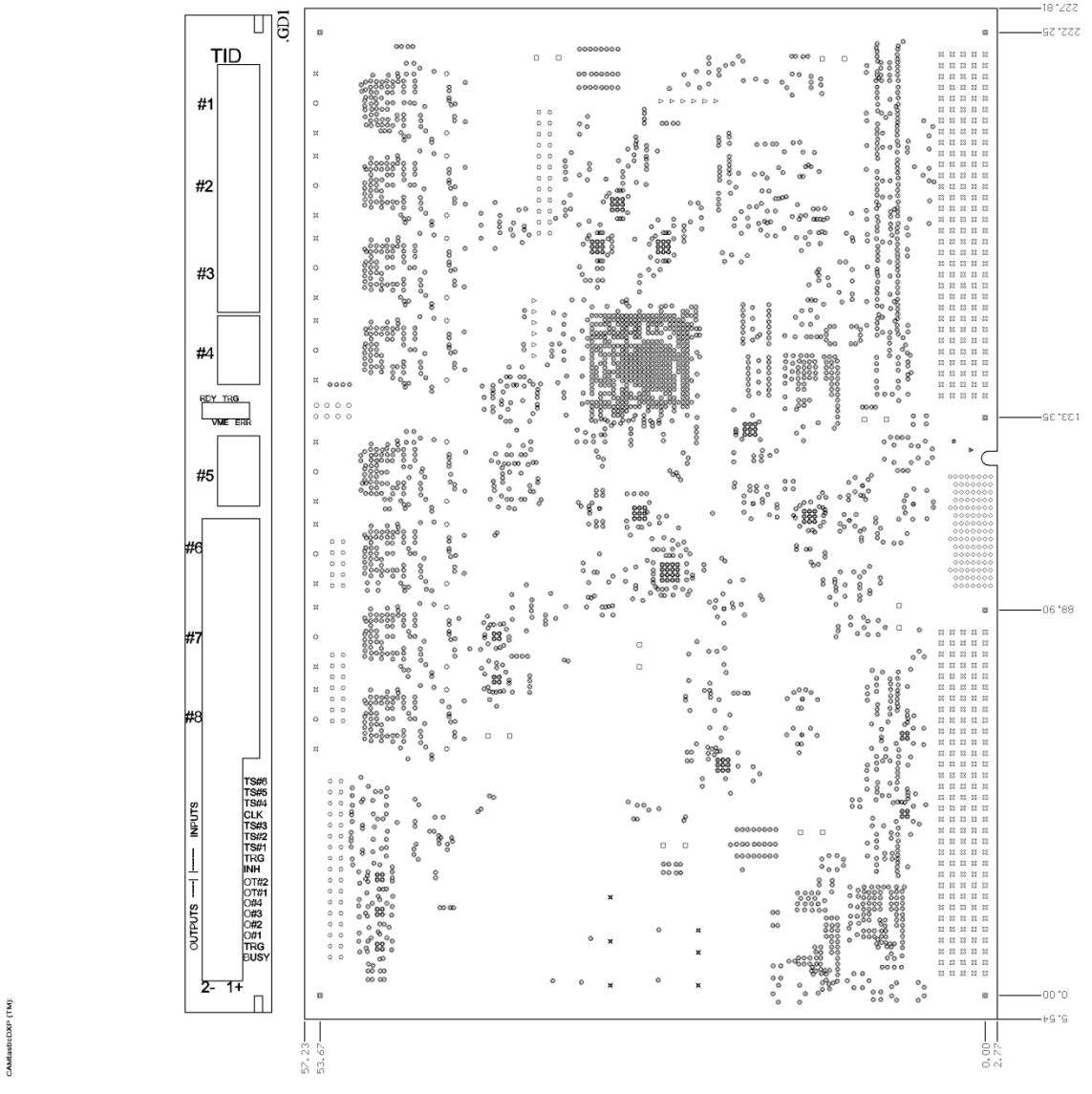
The active parts are on the TID PCB, though the +5V needs go to the mezz board for termination
The passive connectors and resistors, jumpers and the TS_rev2 cable connectors will be on the mezz. board

The above may have lower noise, but there are unnecessary power consumption if the mezz board is not used.
So, this scheme is chosen, that TS_rev2 interface are all on Mezz card.

This is placed in the middle top part of the PCB

Title	TID: TS_Rev2 Interface	
Size: B	Number: 16	Revision:
Date: 5/11/2011	Sheet of	
File: C:\pcb\TIDrev2\TSrev2Mezz.SchDoc	Drawn By: GU	

Appendix B: TID fabrication drawing:



Symbol	Hit Count	Tool Size	Plated	Hole Type
●	2903	0.3mm (11.811mil)	PTH	Round
⊕	115	0.33mm (12.992mil)	PTH	Round
◇	109	0.56mm (22.047mil)	PTH	Round
□	16	0.7mm (27.559mil)	PTH	Round
▽	12	0.9mm (35.433mil)	PTH	Round
⊠	320	0.9652mm (38mil)	PTH	Round
⊡	82	1mm (39.37mil)	PTH	Round
○	8	1.016mm (40mil)	PTH	Round
⌑	6	1.27mm (50mil)	PTH	Round
⌑	16	1.7018mm (67mil)	PTH	Round
◌	24	2.6924mm (106mil)	PTH	Round
◙	6	2.794mm (110mil)	PTH	Round
▽	1	2.794mm (110mil)	NPTH	Round
⌑	1	3.2mm (125.984mil)	NPTH	Round
	3619	Total		

.GTL

CAMtastic!2XP (TM)

.GBL

CAMtastic©KP (TM)

Appendix C: Bill of materials:

Component list

Source Data From:

Project:

Variant:

Report Date: 5/12/2011

Print Date: 12-May-11

Description	Footprint	Quantity		Designator
Capacitor	0402	11		C0001, C0002, C0003, C0004, C0007, C0008, C0013, C0014, C0017, C0018, CUC04A
Capacitor (Semiconductor SIM Model)	1608[0603]	28		C0005, C0006, CCL01, CCL02, CCL03, CCL04, CCL05, CCL06, CCL07, CCL08, CCL09, CCL11, CCL12, CCL13, CCL14, CCL15, CCL16, CCL17, CCL18, CP01, CP02, CP03, CP04, CP05, CP06, CP07, CUP07A, CUP07B
Capacitor, Capacitor (Semiconductor SIM Model)	0402	121		C9510A, C9510B, C9510C, C9510D, CCAU1, CCAU2, CCAU3, CCAU4, CCAU5, CCAU6, CCAU7, CCAU8, CCF01, CCF02, CCF03, CCF04, CCF11, CCF12, CCF13, CCF14, CCF15, CCF16, CCF17, CCF18, CCF21, CCF22, CCF23, CCF24, CCF25, CCF26, CCF27, CCF28, CCF31, CCF32, CCF33, CCF34, CCF35, CCF36, CCF37, CCF38, CCF41, CCF42, CCF43, CCF44, CCF45, CCF46, CCF47, CCF48, CCF51, CCF52, CCF53, CCF54, CCF55, CCF56, CCF57, CCF58, CCF61, CCF62, CCF63, CCF64, CCF65, CCF66, CCF67, CCF68, CCF71, CCF72, CCF73, CCF74, CCF75, CCF76, CCF77, CCF78, CCF81, CCF82, CCF83, CCF84, CCF85, CCF86, CCF87, CCF88, CCF101, CCF102, CCF103, CCF104, CCF119, CCF129, CCF139, CCF149, CCF159, CCF169, CCF179, CCF189, CCLK04, CCLK05, CCT11, CCT12, CFB21, CFB22, CFB31, CFB32, CFB41, CFB42, CFB61, CFB62, CFB71, CFB72, CFB81, CFB82, CGTP1, CGTP2, CU201, CU202, CU203, CU204, CU205, CU206, CU207, CU208, CUC04, CUC08A, CUC08B

Capacitor, Ceramic Chip Capacitor - Standard	0603	143		CCA01, CCA02, CCA03, CCA04, CCA05, CCA06, CCA07, CCA08, CCA09, CCA10, CCA11, CCA12, CCA13, CCA23, CCA24, CCA25, CCA26, CCE01, CCE02, CCE03, CCE04, CCE05, CCE06, CCE08, CCE09, CCE10, CCF111, CCF112, CCF114, CCF115, CCF117, CCF118, CCF121, CCF122, CCF124, CCF125, CCF127, CCF128, CCF131, CCF132, CCF134, CCF135, CCF137, CCF138, CCF141, CCF142, CCF144, CCF145, CCF147, CCF148, CCF151, CCF152, CCF154, CCF155, CCF157, CCF158, CCF161, CCF162, CCF164, CCF165, CCF167, CCF168, CCF171, CCF172, CCF174, CCF175, CCF177, CCF178, CCF181, CCF182, CCF184, CCF185, CCF187, CCF188, CCPG1, CCPG2, CCPG3, CCPG4, CCPG5, CCPG6, CCPG7, CCPG8, CCPG92, CCSE01, CCSE02, CCSE03, CCSE04, CCSE05, CCSE06, CCSE07, CCSE08, CCSE08x, CCSE09, CCSE11, CCSE12, CCSE13, CCV01, CCV02, CCV03A, CCV04, CCV05, CCV06, CCV07, CCV08, CCV09, CCV10, CCV11, CCV12, CCV13, CCV14, CCV15, CCV21, CCV22, CCV23, CCV33, CCV36, CCV37, CCV38, CCV39, CCV40, CVUC04A, CVUC04B, VCB1, VCB2, VCB3, VCB4, VCB5, VCB6, VCB7, VCB8, VCB9, VCB10, VCB11, VCB12, VCB13, VCB14, VCB15, VCB16, VCB17, VCB18, VCB19, VCB29, VCB39
Capacitor, Capacitor (Semiconductor SIM Model)	0402	18		CCCF1, CCCF2, CCCFlx, CCCFS, CCGT, CCP1, CCP1_NL, CCP2, CCP3, CCP3_6, CCP4, CCP6, CCPGTP4, CCUIO1, CCUIO2, CCUIO3, CUF12BB, CUF13BB
Solid Tantalum Chip Capacitor, Standard T491 Series - Industrial Grade	A	71		CP1, CP6, CP9, CP9A, CP9B, CP9C, CP9D, CP9E, CP10, CP11, CP95x, CPE1, CPE2, CPF11, CPF12, CPF13, CPF14, CPF22, CPF23, CPF24, CPF32, CPF33, CPF34, CPF42, CPF43, CPF44, CPF51, CPF52, CPF53, CPF54, CPF62, CPF63, CPF64, CPF71, CPF72, CPF73, CPF74, CPF82, CPF83, CPF84, CPL02, CPL03, CPL04, CPL05, CPL06, CPL07, CPL08, CPL09, CPL10, CPL11, CPL12, CPL13, CPL14, CPL15, CPV1, CPV2, CPV3, CPV4, CPV35, CPV36, CTA1, CTA2, CTA3, CTA4, CTPG1, CTPG2, CTSC1, CTSC2, CTSC3, VCA1, VCA2
Solid Tantalum Chip Capacitor, Standard T491 Series - Industrial Grade, Solid Tantalum Chip Capacitor, Standard T520 Series - Industrial Grade	B	9		CP2, CP3, CP4, CP5, CP7, CP7X, CP20, CPL01, CPL20
Solid Tantalum Chip Capacitor, Standard T491 Series - Industrial Grade	B	1		CP5_NL
Typical RED, GREEN, YELLOW, AMBER GaAs LED	3.2X1.6X1.1	24		DF11, DF12, DF21, DF22, DF31, DF32, DF41, DF42, DF51, DF52, DF61, DF62, DF71, DF72, DF81, DF82, DP1, DP2, DP3, DP3_4, DP4, DP5, DPG1, DPG5
	EC5BE17	1		EC34
FUSE 5A SLO BLO NANO 2 SMD	NANO_FUSE	3		F5, F12, F15
	fiducial	40		FID1, FID2, FID3, FID4, FID5, FID6, FID7, FID8, FID9, FID10, FID11, FID12, FID13, FID14, FID15, FID16, FID17, FID18, FID19, FID20, FID21, FID22, FID23, FID24, FID25, FID26, FID27, FID28, FID29, FID30, FID31, FID32, FID33, FID34, FID35, FID36, FID37, FID38, FID39, FID40

FUSE 5A SLO BLO NANO 2 SMD	NANO_FUSE	1		FP1
Header, 6-Pin	HDR1X6	2		FPGA_JTAG, PROM_JTAG
Jumper Wire	RAD-0.2	8		GND1, GND2, GND3, GND4, GND5, GND6, GND7, GND8
Flat Cable Connector (IDC), Low-Profile Male Header, Angled Solder Pin, 34 Contacts, Performance Level 2	918534x323	1		JC1
INDUCTOR 1.0UH 300MA 20% 0805	0805	24		LF11, LF13, LF15, LF21, LF23, LF25, LF31, LF33, LF35, LF41, LF43, LF45, LF51, LF53, LF55, LF61, LF63, LF65, LF71, LF73, LF75, LF81, LF83, LF85
INDUCTOR 6.8NH 10% 0603 SMD	0603	24		LF12, LF14, LF16, LF22, LF24, LF26, LF32, LF34, LF36, LF42, LF44, LF46, LF52, LF54, LF56, LF62, LF64, LF66, LF72, LF74, LF76, LF82, LF84, LF86
Inductor	L0603	17		LL01, LL02, LL03, LL04, LL05, LL06, LL07, LL08, LL09, LL11, LL12, LL13, LL14, LL15, LL16, LL17, LL18
Inductor	1210	9		LP1, LP2, LP3, LP4, LP5, LP10, LP11, LP20, LP33
VME160-P1	VME160	1		P1
VME160-P2	VME160	1		P2
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W, Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	2-0402	45		P2R1, P2R2, P2R3, P2R4, P2R5, P2R6, P2R7, P2R8, P2R9, P2R10, P2R11, P2R12, RAT10, RAT11, RAT12, RAT13, RAT14, RAT15, RAT18, RAT19, RAT20, RAT21, RCT41X, RIO11, RIO12, RIO13, RIO14, RIO15, RIO16, RIO17, RIO18, RIO21, RIO22, RIO23, RIO24, RIO25, RIO26, RIO27, RIO28, RP12, RP12x, RP16, RPG12, RPG12x, RST99X
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W, Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	2-0402	112		P2R21, P2R22, P2R23, P2R24, P2R25, P2R26, P2R27, P2R28, P2R29, P2R30, P2R31, P2R32, P2R33, P2R34, P2R35, P2R36, P2R37, P2R38, RAT01, RAT02, RAT03, RAT16, RAT16A, RAT16B, RAT24, RAT24A, RAT24B, RC20, RC30, RC30a, RC31, RC32, RC33, RC43, RC44, RC46, RC47, RC48, RC48a, RC49, RC101, RCT17, RCT18, RCT19, RCT30, RCT31, RCT32, RCT43, RCT44, RCT45, RCT48, RCT49, RIO1, RIO2, RIO3, RIO4, RIO5, RIO6, RIO7, RIO8, RIO9, RIO31, RIO32, RIO33, RIO34, RIO35, RIO36, RIO37, RIO38, RIO39, RIO41, RIO42, RIO43, RIO44, RIO45, RIO46, RIO47, RIO48, RIO51, RIO52, RIO53, RIO54, RIO55, RIO56, RIO57, RIO58, RIO61, RIO62, RIO63, RIO64, RIO65, RIO66, RIO67, RIO68, RST31, RST31A, RST32, RST155, RST156, RST157, RST158, RST159, RST160, RT1, RT2, RT3, RT4, RT5, RUC04, RVP0, RX02, RX02F
Flat Cable Connector (IDC), Low-Profile Male Header, Angled Solder Pin, 10 Contacts, Performance Level 2	918510x323	1		PFADC
Flat Cable Connector (IDC), Low-Profile Male Header, Angled Solder Pin, 14 Contacts, Performance Level 2	918514x323	1		PFTDC
P0-PL-VXS	P0-105_P0-	1		PP0

	PL-VXS			
Flat Cable Connector (IDC), PCB Transition Connector, 2 Rows, Kinked Solder Pin, 24 Contacts	9181249421	1		PTS1
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W, Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	2-0402	80		RAT22, RAT23, RC11, RC12, RC13, RC14, RC15, RC16, RC17, RC18, RC19, RC21, RC22, RC23, RC24, RC25, RC26, RC27, RC28, RC29, RCT46, RCT47, RCT51, RCT51A, RCT51B, RCT52, RCT52A, RCT52B, RF90, RF91, RF92, RF93, RF94, RF95, RF96, RF97, RF98, RF99, RF101, RF102, RF103, RF104, RF105, RF106, RF107, RF108, RF109, RF110, RP6y, RPG8, RST33, RST34, RST35, RST36, RST37, RST38, RST39, RST40, RST41, RST42, RST43, RST44, RST45, RST46, RST47, RST48, RST49, RST50, RST101, RST102, RST103, RST104, RST151, RST152, RST153, RST154, RUP06A, RUP06B, RUP06C, RUP06D
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W, RES 100 OHM 1/16W 1% 0402 SMD, Resistor	0603	85		RC01, RC06, RC07, RC08, RCT42X, RCTR2A, RCTR3A, RCTR3B, RCX01, RCX02, RCX03, RCX04, RCX09, RCX10, RCX11, RE01X, RE06X, RF11, RF12, RF14, RF16, RF18, RF21, RF22, RF24, RF26, RF28, RF31, RF32, RF34, RF36, RF38, RF41, RF42, RF44, RF46, RF48, RF51, RF52, RF54, RF56, RF58, RF61, RF62, RF64, RF66, RF68, RF71, RF72, RF74, RF76, RF78, RF81, RF82, RF84, RF86, RF88, RI2C1, RI2C2, RI2C3, RI2C4, RI2C5, RI2C6, RP3_14, RP4, RP6, RP6x, RP9y, RP11, RP13, RP14, RP15, RPG11, RPG13, RS16, RS17, RS18, RS21A, RS22A, RS23A, RS24A, RST99D, RV02xy, RV04X, RV12xy
Resistor	0603	88		RC02, RC03, RC04, RC05, RCT50A, RCTR1, RCTR2, RCTR3, RCX05, RCX06, RCX07, RCX08, RCX12, RCX13, RCX14, RE01, RP2, RP3, RP3_15, RP3_16, RP3NL, RP3NLA, RP3x, RP5, RP9, RP9z, RP10, RP101, RP102, RP103, RP104, RP105, RP106, RP107, RP108, RP109, RP110, RP111, RP112, RPG2, RPG3, RPG4, RPG5, RPG6, RPG7, RPG9, RPG10, RPG11A, RPGCLK3, RS1, RS2, RS3, RS4, RS5, RS6, RS7, RS8, RS11, RS12, RS13, RS14, RS15, RS21, RS22, RS23, RS24, RS25, RS26, RS27, RS28, RTS19, RU40, RU40G, RUSFM, RV01, RV01x, RV02, RV02x, RV03, RV04, RV05, RV05x, RV07, RV07A, RV08, RV12x, RV12yz, RV44
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W	0402	8		RCT09, RCT10, RCT11, RCT12, RCT13, RCT14, RCT15, RCT16
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W, RES 100 OHM 1/16W 1% 0402 SMD, Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	0402	16		RCT41, RCT42, RGT1, RGT2, RST99B, RST99C, RTD0x, RTD01, RTD02, RTD03, RTD04, RTD05, RTD05X, RTD06, RTD07, RTD08

Resistor	0603	1		RE05X
RES 100 OHM 1/16W 1% 0402 SMD, Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	0402	32		RF13, RF15, RF17, RF23, RF25, RF27, RF33, RF35, RF37, RF43, RF45, RF47, RF53, RF55, RF57, RF63, RF65, RF67, RF73, RF75, RF77, RF83, RF85, RF87, RIO19, RIO29, RST16, RST99, RST99A, RT4A, RT4B, RT4C
Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	0402	6		RID01, RID02, RID03, RID04, RPGCLK_NL, RPGD01_NL
Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	0402	8		RID11, RID12, RID13, RID14, RID15, RID16, RPGCLK2, RPGD02
Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	2-0402	4		RIO33x, RIO33y, RIO33z, RUC04A
DIP Switch, 8 Position, SPST	SW16_L	4		S1, S2, SC01, SC1
AD9510	CP-64-1_N	1		U13
IC 11-BIT I-WS BUS TXRX 48-TSSOP	TSSOP50P810-48AL	1		U17
Xilinx Virtex-5 LXT Platform FPGA, 665-Ball FFBGA, Speed Grade 1, 360 User I/Os, Commercial Grade	FF665	1		U20
On Semiconductor, Any level positive to ECL translator	QFN50P400X400-24W4M	7		U27, U31, UIO4, UIO5, UIO6, UVP21, UVP22
4 Channel ECL/PECL/LVDS -> LVTTL	TSSOP-16	1		U40
CCPD-034	SO6-5X7	1		UC01
Any level in, LVPECL out 1:2 fanout	QFN50P300X300-16V7N	6		UC04, UC04A, UC05, UC06, UF11, UP06
4:1 Differential Multiplexer	948E-02_L	1		UC07
ON-Semi Dual 2 X 2 CrossSwitch	RHB32_N	1		UC08
2x2 crosspoint switch with LVPECL output	QFN50P300X300-16V4N	2		UC10A, UC10B
Micrel dual Anylevel to LVPECL translator	TSSOP50P490-10AN	1		UC14
Low-Voltage 1:10 Differential LVECL/LVPECL/LVEPECL/HSTL Clock Driver	873A-02_L	2		UC15, US8
Differential to CML buffer	846A-02	1		UC17

	TSSOP14	4		UE01, UE02, UE07, UE08
	TSSOP14	2		UE03, UE05
	TSSOP14	2		UE04, UE06
	TSSOP14	3		UE09, UV21, UV22
	TSSOP20	1		UE10
HFBR7934	84512-102LF	8		UF1, UF2, UF3, UF4, UF5, UF6, UF7, UF8
Low-Voltage 1:5 Differential LVECL/LVPECL/LVEPECL/HSTL Clock Driver	948E-02_N	4		UF12, UF13, US4, UT1
Triple ECL to PECL Translator	948E-02_N	3		UIO1, UIO2, UIO3
Dual LVPECL to LVDS translator	TSSOP50 P490-10AN	5		UIO7, UIO8, UIO9, UIO10, US1
LUMEX, Quad pack LEDs	LED14	1		ULED
LTM4604EV	LGA-66_LTM4604EV(Primary)	3		UP1, UP1_NL, UP3
IC LDO REG 3.0A W/SS 20-VQFN	QFN-20	5		UP2, UP4, UP5, UP33, UPG5
Analog 1.25Gbps Clock and Data Recovery IC	QFN50P500X500-32W2N	1		UP07
Miniature Oscillator	CFPX-5	1		UPG1
XCF00P Series, Platform Flash In-System Programmable Configuration 1.8V PROM, 48-Pin TSSOP, 32-Megabit, Commercial Grade	VO48	1		UPG2
Atmel flash memory	8S1_N	1		USFM
IC UNIV BUS TXRX TRI-ST 48-TSSOP	TSSOP50 P810-48AL	9		UV1, UV2, UV3, UV4, UV5, UV6, UV10, UV12, UV14

Appendix D: Glossory:

TID: Trigger Interface and Distribution module; a PCB design can be configured as TI, TD, TS or TM;

TI: Trigger Interface module; It seats in payload slot#18 in front end crates, interfaces the trigger and the DAQ system; It is one stuffing variation of the TID.

TD: Trigger Distribution module; It seats in payload slot#1-16 in the global trigger distribution and fans out the TRIGGER/CLOCK/SYNC to eight TIs; it is one stuffing variation of the TID.

TS: Trigger Supervisor; It seats in payload#18 in the global trigger distribution crate; It is the interface between DAQ and trigger system; A simplified (pre-prototype) TS can be stuffed from a TID;

TM: TID Master. It is used in the subsystem test or commissioning setup; It generates TRG/CLK/SYNC as a TS, sends TRG/CLK/SYNC to P0 and P2 like a TI, and fans out TRG/CLK/SYNC through fiber to other TI like a TD.

SD: Signal Distribution module; It fans out TRG/CLK/SYNC from payload slot#18 to payload slots#1-16; It has clock jitter cleanup capability.

GTP: Global Trigger Processor module.

CTP: Crate Trigger Processor module.

DAQ: Data Acquisition.

ROC: Readout Controller; A VME CPU module used to readout the front end data through VME bus.

VXS: VME Switched Serial; A VME extension with dual-star serial switch slots.

MGT: Multiple Gbps Transceiver; A builtin transceiver module in Xilinx FPGA. In XC5VLX30T FPGA, it supports up to 3.125 Gbps.

Appendix E: TID data format:

The TID data is formatted in blocks of events. Each Trigger_1 is one event. A block of data contains a predefined number (the number could be 1) of triggers. Each block has block header, block trailer, possible place holder, and event data. The data format is summarized here:

Block headers
Event#1 data
Event#2 data
……
Event#N data
Block trailer
Filler words for 2ESST transfer

```
Block Header#1:
  bit(31:27): 10000, block header indicator;
  Bit(26:22): BoardID, the VME64x geographic address (slot number);
  Bit(21:18): 0000, ID for TI board;
  Bit(17:8): block number, lower ten bits;
  Bit(7:0): block size (as set by A24 register 0x14);

Block Header#2:
  Bit(31:17): 1111,1111,0001,000X; or 0xFF1X;
  Bit(16): TimeStamp, 1 if timestamp is available, 0 if not;
  Bit(15:8): 0010,0000, or 0x20;
  Bit(7:0): Block size;

Block Trailer#1:
  Bit(31:27): 10001, block trailer indicator;
  Bit(26:22): BoardID, VME64x geographic address (slot number);
  Bit(21:0): Word count; does not include block header or trailer.
Filler words:
  DataNotValid, read data when the data buffer is empty (no more data):
    Bit(31:27): 11110;
    Bit(26:22): BoardID
    Bit(21:0): 00,0000,1011,1010,1101,0000, or 0x00BAD0;
  Filler word #1 to make the word count an even number for D64 transfer:
    Bit(31:27): 1111,1;
    Bit(26:22): BoardID;
    Bit(21:0): block number;
  Filler word #2 to make the word count 'even' for 2ESST:
    Bit(31:27): 1111,1;
    Bit(26:22): BoardID;
    Bit(21:0): 00,1111,0001,0001,0001,0000; 0x0F1110 (0_fill_0)

Event data word1: (event header)
  Bit(31:24): Trigger Type;
        0x00: filler events,
        0x01: Physics trigger;
        0x02: VME trigger;
        0x03: Random trigger,
        For TImaster bit(31:26) represents the TS#6-1 inputs;
  Bit(23:16): 0000,0001, or 0x01;
  Bit(15:0): Event wordcount; Event header is excluded from the count

Event data word2:
  Bit(31:0): trigger number; counting from 1 to be consistent with wrap
```

```
        around;

Event data word3: (enabled by data format register 0x18, bit#1)
  Bit(31:0): trigger timing; 4ns step

Event data word4: (enabled by data format register 0x18, bit#2)
  Bit(31:16): trigger number bit(47:32), to form 48 bit counter with word2;
  Bit(15:0): trigger timing bit(47:32), to form 48 bit counter with word3;
```

Appendix F: Document revision history:

Updated on Apr. 20th, 2010

Updated on May 13th, 2010

Updated on May 19th, 2010: add the trigger acknowledge in the status word;

Updated on July 6th, 2010: Define the TI/TD mode in section 5.2.2;

Updated on Sept. 20th, 2010: Re-define the A24 address space;

Updated on Oct. 15th, 2010: Added Busy_Input_Enable (A24, 0x0004);

Updated on Oct. 18th, 2010: updated the Emergency loading after tests;

Updated on Jan. 13th, 2011: Add examples for VME trigger word loading;

Updated on Feb. 2nd, 2011: clarify the A24 0x00-0x1C registers;

Updated on Mar. 21st, 2011: further updates on registers to match with the firmware;

Updated on Mar. 25th, 2011: Added the software setup procedure section, with some updates on the registers;

Updated on Apr. 5th, 2011: Register offset 0x14 and 0x2C update.

Updated on Apr. 18th, 2011: Enables for each GTP input bits, CLK250 source selection

Updated on Apr. 20th, 2011: added the Sync decoding, and two more A24 read registers;

Updated on May 12th, 2011: Added the PCB schematics, fab layers, and BOM as appendix A, appendix B and appendix C.

Updated on June 6th, 2011: Added A24 offsets 0x38 and 0x3C for extra readout (v10)

Updated on June 22nd, 2011: Redefined A24, 0x08 and 0x30 registers;

Updated on Aug. 18th, 2011: Overall revision to add the TM description, Glossary and data format;

Updated on May 31st, 2012: expanded the trigger rule bits from 5 to 7 bits;

Updated on Oct. 10th, 2012: Put in the new register map; Specifically for TI/TImaster;

Updated on Feb. 14th, 2013: Add the A24 offset for switch slot mirror registers;

Updated on Mar. 12th, 2013: Add the switch usage of SC01

Updated on Apr. 3rd, 2013: updated offset register 0x24, 0x78 and 0x98

Updated on Apr. 23rd, 2013: updated offset registers: 0xD4, 0x100; added section 3.13 SyncEvent generation.

Updated on July 26th, 2013: clarify the trigger timing words (register 0x18);

Updated on Aug. 15th, 2013: updated A24 register 0x78, 0x100, 0xD8, 0xDC;

Updated on Sept. 13, 2013: updated A24 registers: 0x34, 0x04, 0x94 and 0xB0;

Updated on Sept. 27, 2013: updated the Appendix E, data format;

Updated on Oct. 17, 2013: updated register 0x14, 0x78 and 0x84;

Updated on Dec. 3, 2013: Added register offsets 0x1D0 – 0x1F0 for slave TI IDs;

Updated on Feb. 28, 2014: fixed the register 0xA4 to reflect the firmware, which is the fiber#5 measurement.