fADC125 register map

Firmware version 0x00020001

Main FPGA(0x0000-0x0ffc)

Board ID – Status (0x0000)

0xADC12500

Swap Control – Control/Status (0x0004)

Any write other than "0" swaps.

Firmware version – Status (0x0008)

Main CSR - Control/Status (0x000C)

1-0 (R/W) – select clock

00 – P2 clock
01 – P0 clock
10 – On
11 – local 125Mhz – (default in firmware)

Power Control - Control/Status (0x0010)

Writing 0x3000ABCD turns "ON",
Anything else turns "OFF"

DAC Control – Control (0x0014) – note: write only

0 – (W) –
1 – (W) – Serial Interface Chip Load (main and mezz chains)
2 – (W) – Serial Interface Clock Input (main and mezz chains)
3 – (W) –
4 – (W) – Serial Interface Data Input (main chain)
5 – (W) –
6 – (W) –
7– (W) –
8 – (W) – Serial Interface Data Input (mezz chain)

Control/Status (0x0018 -0x001C) – used for testing

Serial – Status (0x0020-0x002C)

0x0020 – main_serial(47 downto 32)
0x0024 – main_serial(31 downto 0)
0x0028 – mezz_serial(47 downto 32)
0x002C – mezz_serial(31 downto 0)

Temperature – Status (0x0030-0x0034)

0x0030 – main temperature
0x0034 – mezz temperature

Geographical slot address – Status (0x0038)

0 – (R) – bit 0 of GAD
1 – (R) – bit 1 of GAD
2 – (R) – bit 2 of GAD
3 – (R) – bit 3 of GAD
4 – (R) – bit 4 of GAD

A32 base address – Status (0x003C)

Block CSR – Control/Status (0x0040)

0 – (R) –
1 – (R) –
2 – (R) – Block of Events ready for readout
3 – (R) – BERR Status (1 = BERR asserted)
4 – (R) – Token Status (1 = module has token)
5 – (W) – Take Token
6 – (W) – Pulse Soft Sync Reset
7 – (W) – ~~Pulse Soft Trigger~~ (ACTUALLY bit 0 of 0xd010, on proc)
8 – (W) – Pulse Soft Reset
9 – (W) – Pulse Hard Reset

CTRL1 – Control/Status (0x0044)

1-0 (R/W) – Sync reset source select N/A, MOVED TO PROC (0xd00C)
    00– (R/W) – N/A, moved to proc
    01 – (R/W) – N/A, moved to proc
    10 – (R/W) – N/A, moved to proc
    11 – (R/W) – N/A, moved to proc
2 – (R/W) – Enable BERR response
3 – (R/W) – Enable Multiboard protocol
4 – (R/W) – FIRST board in Multiblock system
5 – (R/W) – LAST board in Multiblock system

ADR32 – Control/Status (0x0048)

0 – (R/W) – Enable 32-bit address decoding
[1… 6] – (not used – read as 0)
[15…7] – (R/W) – Base Address for 32-bit addressing mode (8 Mbyte total)

ADR_MB – Multiblock Address for data access (0x004C)

0 – (R/W) – Enable Multiblock address decoding
1 – 6 – (not used – read as 0)
[15…7] – (R/W) – Lower Limit address (ADR_MIN) for Multiblock access

16 – 22 – (not used – read as 0)
[31…23] – (R/W) – Upper Limit address (ADR_MAX) for Multiblock access
The board that has the TOKEN will respond with data when the VME address satisfies the following condition:

$$ADR\_MIN \leq Address < ADR\_MAX.$$

Module Busy Level – Control/Status (0x0050)

[19…0] – Busy level (eight byte words)
(External RAM word count > Busy level -> module busy = 1)
[31] – Force module busy

Block Count – Control/Status (0x0054)

[19…0] – (R) - number of event BLOCKS on board

CONFIGURATION_CSR (0x0058) – (Firmware Update)

[31] – (R/W) – vme program enable
[30…28] – (R/W) – Reserved
[27] – (R/W) – Reserved
[26…24] – (R/W) – OPCODE (bit 31 = 1 also required)
[23…9] – (R) – Reserved
8 – (R) – Busy (operation in progress)
[7…0] – (R) – Last Valid Data Read

CONFIGURATION_ADR/DATA_(R/W) (0x005C) – (Firmware Update)

[31] – Execute
[30…18] – Page address
[17…8] – Byte address
[7…0] – EPROM data to write

Processor FPGA(0xd000-0xdffc)

Processor Firmware Version – Status (0xd000)

Processor CSR – Control/Status (0xd004)

0 – (R) – busy status – not used
1 – (R/W) – processor csr clear – not used
2 – (R/W) – reset (testing) N/A

Trigger source – Control/Status (0xd008)

1 – 0 (R/W) – trig setup

00 - trig on p0_trg(0) rising
01 - trig on SW TRIGGER (was internal timer)
10 - trig on internal multiplicity sum
11 - trig on p2_trg(0) rising

CTRL2 – Control/Status (0xd00C)

0– (R/W) – Enable Trigger to Module (source = Trigger source[1-0])

1– (R/W) – ~~Enable Sync Reset to Module~~ N/A, MOVED TO FE (0x1004)

3-2 (R/W) – Sync reset source select - default "00"

00– (R/W) – P0 Connector (VXS)
01 – (R/W) –
10 – (R/W) – VME (software generated)
11 – (R/W) – no source

Control/Status (0xd010) – used for testing

0-R/W –

BLOCK SIZE – Control/Status (0xd014)

[15…0] - (R/W) – number of events in a BLOCK.

Stored Event Count ≥ BLOCK SIZE → BLOCK CSR[2] = 1.

[31…16] – (not used)

Trigger Count – Control/Status (0xd018)

[30…0] – (R) – total trigger count

31– (R/W) – reset count

Event Count – Control/Status (0xd01C)

[23…0] – (R) – number of events on board

CLOCK_125 COUNT REGISTER (0xd020)

0 – (W) – Write '1' resets the counter. Write '1' initiates 20us counting interval.

[31 - 0] – (R) – CLK_250 counter value. (Should be 5000 after count interval.)

SYNC_IN_P0 COUNT REGISTER (0xd024)

0 – (W) – Write '1' resets the counter.

[31 - 0] – (R) – SYNC_IN_P0 counter value.

TRIG2_IN_P0 COUNT REGISTER (0xd028)

0 – (W) – Write '1' resets the counter.

[31 - 0] – (R) – TRIG1_IN_P0 counter value

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Pulser_Control (0xd02C)

0 - (W) - write '1' to enable pulser mode
[1 - 31] - (reserved)

Pulser_Trig_delay (0xd030)

[11 – 0] – R/(W) – delay trigger, in # of samples at 125 Mhz
[31 - 12] - (reserved)

FE PFGA(0x1000-0xcffc)

FE Firmware Version – Status (0x1000)

FE Test Register (0x1004)

0– (R) – reset (testing) read
1– (R/W) – Collect On default on
2– (R/W) – Enable Sync Reset to Module default on, all rst sync

FE Asynchronous ADC read – Status (0xN020-0xN034) – not used

FE FIFO ADC read – Status (0xN040-0xN054) – not used

PTW (0x1058)

[9 - 0] – (R/W) – Window Width (NOW 10 bits!!!)

PL (0x105C)

[15 - 0] – (R/W) – # of samples back from trigger point

PTW DAT BUF LAST ADDR (0x1060) – N/A

[11 - 0] – (R/W) – Last Address of secondary buffer (see calculation 1.0 below)

PTW MAX BUF (0x1064) – N/A

[7 - 0] – (R/W) – Max # of unprocessed PTW blocks to store in secondary buffer (see calculation 2.0 below)

NSB (0x1068) - N/A

[12 - 0] – (R/W) – # of samples before (including) trigger point to include in data processing

NSA (0x106C) - N/A

[13 - 0] – (R/W) – # of samples after trigger point to include in data processing

TET 1 (0xN070)

[11 - 0] – (R/W) – Threshold Offset added to Initial pedestal calculation

TET 2 (0xN074)

[11 - 0] – (R/W) – Threshold Offset added to Initial pedestal calculation

TET 3 (0xN078)

[11 - 0] – (R/W) – Threshold Offset added to Initial pedestal calculation

TET 4 (0xN07C)

[11 - 0] – (R/W) – Threshold Offset added to Initial pedestal calculation

TET 5 (0xN080)

[11 - 0] – (R/W) – Threshold Offset added to Initial pedestal calculation

TET 6 (0xN084)

[11 - 0] – (R/W) – Threshold Offset added to Initial pedestal calculation

CONFIG1 (0x1088)

[2 - 0] – (R/W) – Process mode select

- "000" = Window Raw Data (NOT USED)
- "001" = Pulse Raw Data (NOT USED)
- "010" = Pulse Data (Integral and time, CDC format)
- "011" = Pulse Data (Integral and time, FDC format)
- "100" = Pulse Data (Peak Amplitude and time, FDC format)
- "101" = Pulse Data and Pulse Samples (CDC Format)
- "110" = Pulse Data and Pulse Samples (FDC Format)

[3] – (R/W) – Run (Collect On) default '1'

[9-4] – (R/W) – Max number of peaks to identify –must be > 0

Trigger Number (0xN08C)

[15- 0] – (R) – Trigger number

CONFIG2 (0xN090)

CH mask When '1' ADC values = 0

[0] – (R/W) – ADC 1

[1] – (R/W) – ADC 2

[2] – (R/W) – ADC 3

[3] – (R/W) – ADC 4

[4] – (R/W) – ADC 5

[5] – (R/W) – ADC 6

Test Waveform (0x1094)

[15] – (R/W) – '1' to write PPG Data ('0' for last two samples)

[14-13] – (R/W) – Don't care

[12] – (R/W) – Overflow

[11-0] – (R/W) – PPG Data

TEST (0x1098) N/A

[31 - 0] - (reserved)

PPG_Trig_delay (0x109C) – Uses HW trigger to start playback and delays HW trigger sampling **when testmode (config1(7)) enabled**

[11 – 0] – R/(W) – delay from output pulse to internally generated trigger, in # of samples at 125 Mhz

[31 - 12] - (reserved)

-----NEW REGISTERS------

Pedestal calc and scale factors (0x10A0)

[7-0] – (R/W) – NP (2^n # of samples for initial pedestal calc)

[15-8] – (R/W) – NP 2 (2^np2 # of samples for local pedestal calc)

[18-16] – (R/W) – IBIT (integration scale factor)

[21-19] – (R/W) – ABIT (amplitude scale factor)

[24-22] – (R/W) – PBIT (Pedestal scale factor)

Timing Thresholds 1(0xN0A4)

[7-0] – (R/W) – THRES_HI_0

[15-8] – (R/W) – THRES_LO_0

[23-16] – (R/W) – THRES_HI_1

[31-24] – (R/W) – THRES_LO_1

Timing Thresholds 2(0xN0A8)

[7-0] – (R/W) – THRES_HI_2

[15-8] – (R/W) – THRES_LO_2
[23-16] – (R/W) – THRES_HI_3
[31-24] – (R/W) – THRES_LO_3

Timing Thresholds 3(0xN0AC)

[7-0] – (R/W) – THRES_HI_4
[15-8] – (R/W) – THRES_LO_4
[23-16] – (R/W) – THRES_HI_5
[31-24] – (R/W) – THRES_LO_5

Integration End (0x10B0)

[11-0] – (R/W) – IE (integration end)
[19-12] – (R/W) – PG (Pedestal gap- from timing pedestal x-ing(5) to xthr sample)