VETROC set final assembly and test

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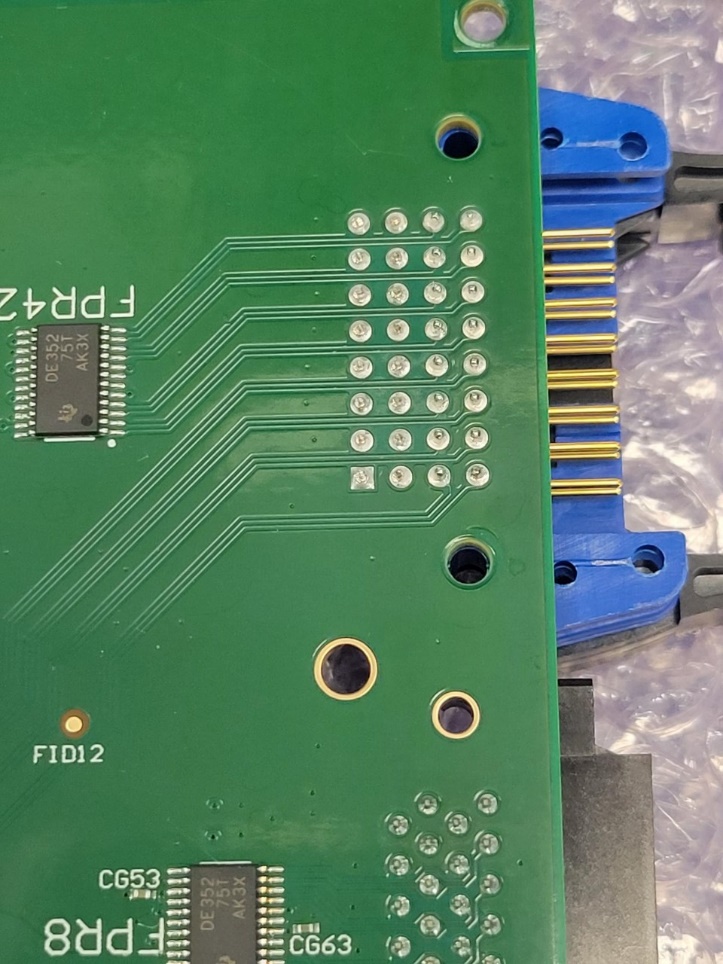
Physics Division

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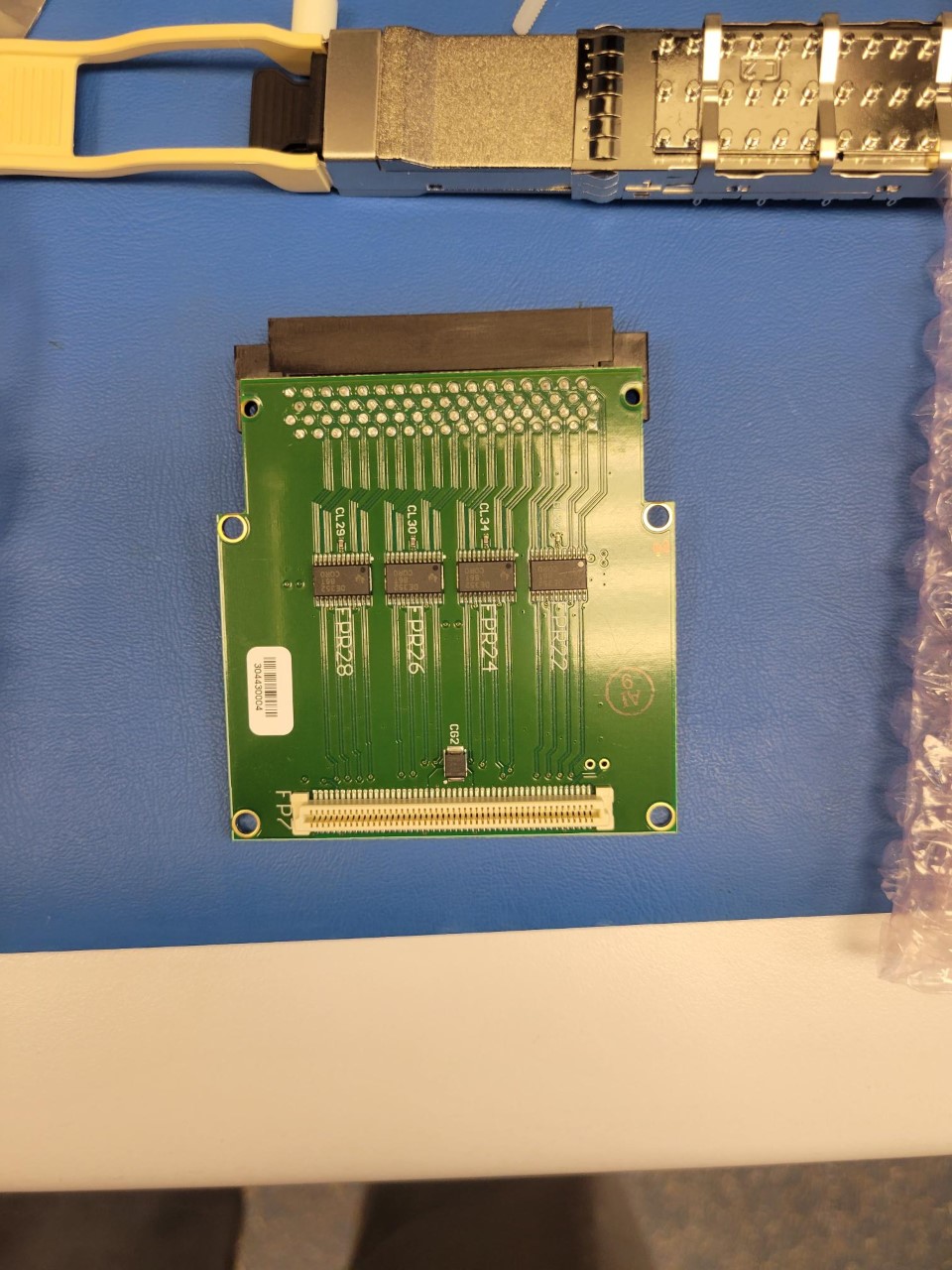
1. **Final Assembly at the lab.**
   1. trim the long pins of the 16-pin stacked connector on the bottom layer of the VETROCbase board



To trim the inner two rows, 16 pins

These 16-pins are too long on the bottom side, which will affect the neighboring board. The long pins are caused by the stacked connectors, which are populated to replace the obsolete 3M N3408-D302 three wall condo connector.

* 1. Trim the Mezzanine card connector pins



To trim all these 68 pins

These pins are too high for the mezzanine board to fit on the VETROCbase with the front panel. For mechanical strength, the front panel opening is minimized, which requires the tight limitation on the thickness of the mezzanine card.

* 1. Add the VXS alignment pin to VETROC base board



VXS alignment pin and the holding screw

While adding the VXS alignment pin, please check the VXS connector installation. The VXS connector should be flat on the VETROC board.

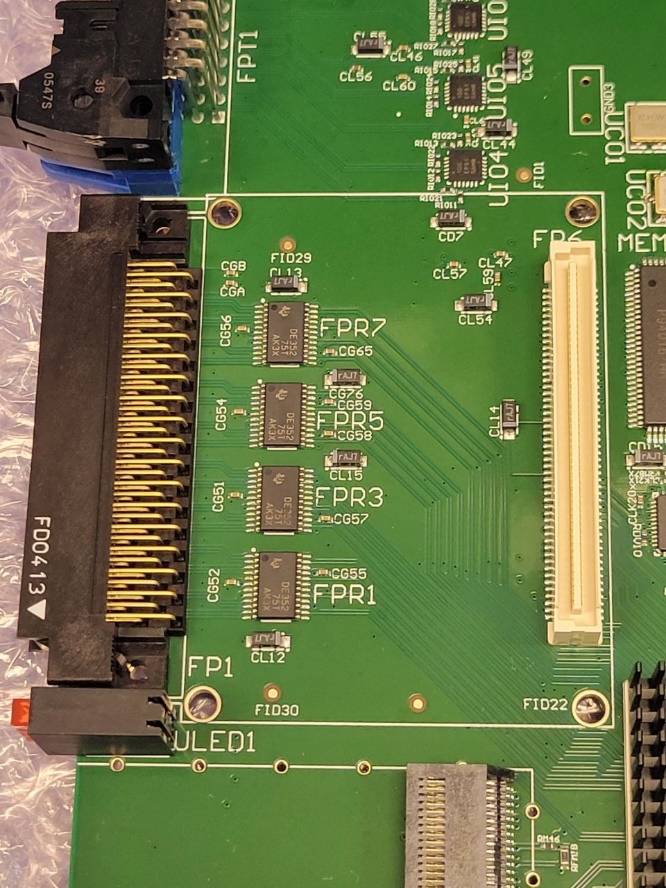
* 1. Populate the QSFP shells on the VETROC base board



Two QSFP shells need to be installed

When installing the QSFP shells, it is easier to plug a QSFP module half way (do not plug in completely as the QSFP will be on the top of the 38-pin QSFP connector), and press down to position. After the shell is properly installed, the QSFP module can be fully plugged in to check out the QSFP installation. When installing the second QSFP shell, special attention is needed on the front area of the EMI ‘spring leaf’, where the two shell’s EMI overlap. One method is to remove the ‘spring leaf’ from one of the QSFP shells. The other method is to wedge in a thin piece of material (a piece of paper is not strong enough, and a credit card is not thin enough) in between the two shells when installing.

* 1. Add the two mezzanine cards and the front panel



It may be necessary to trim off the corner to fit in the mezzanine card more easily

This step is the hardest. Because of the efforts trying to maintain the EMI on the front panel, the front panel installation is not user friendly. There is almost no slack in the front panel opening.

To install the mezzanine cards and the front panel, one must hold the mezzanine card in the front panel opening, and slide the front panel over the VETROC base board. After the front panel is fully in (the exact location), the mezzanine boards can be pushed down to mate with the on-board connectors. This requires the opposite procedure for removing the front panel, where one must unplug the mezzanine connector first before the front panel can be removed.

The front panel fit is so tight that the corners (as indicated in the above picture) may need be removed (cut off). The following picture shows the tight fit of the front panel.



Two pieces of EMI ‘spring leaf’

VETROC mezzanine board

Front Panel EMI gasket

VETROC base build in connector

* 1. Add the four nylon screw and spacer sets

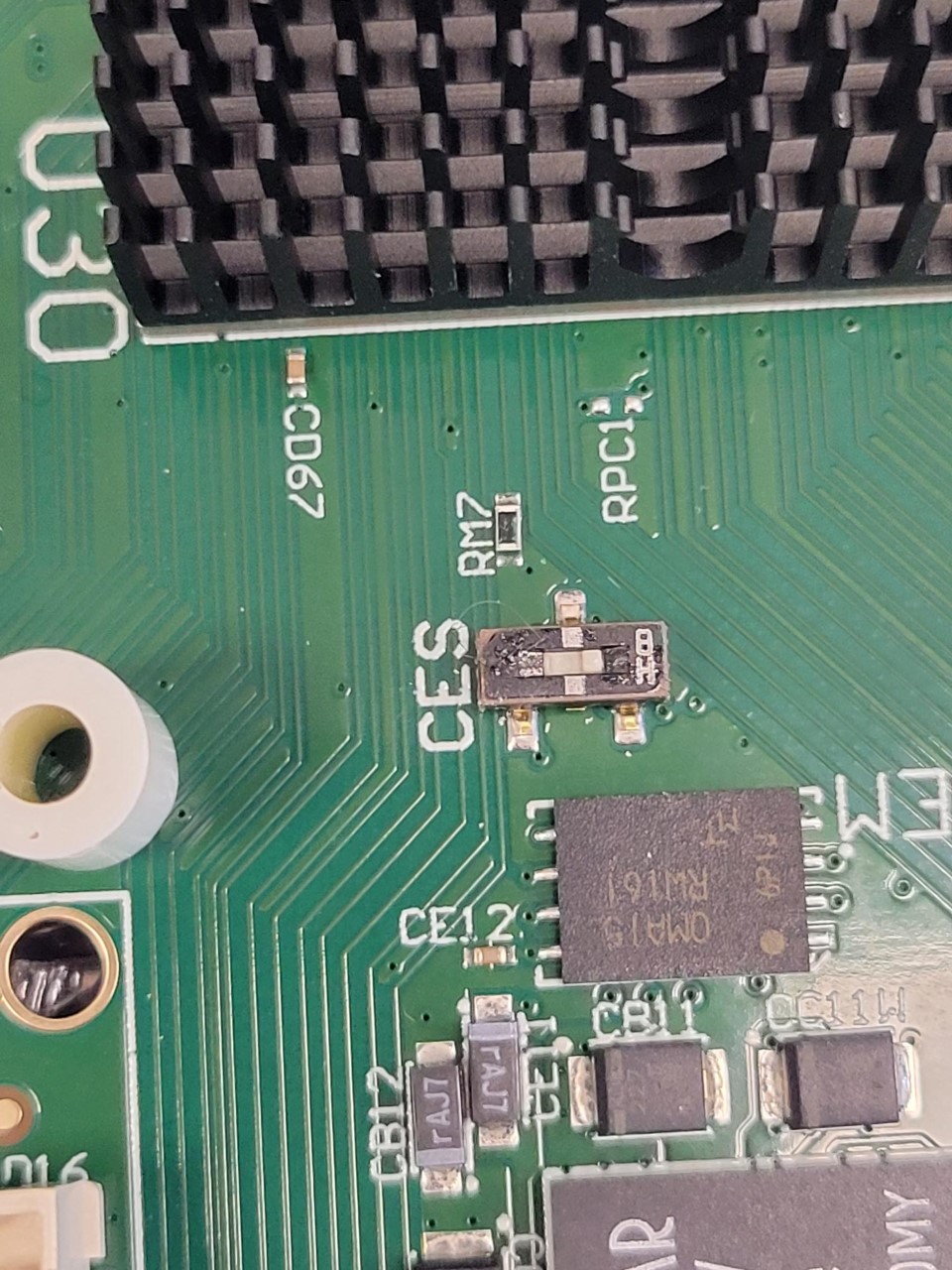
The mezzanine cards fit tightly on the VETROC base board. The front panel cannot move (get loose). The back (mezzanine card connector) is also very tight. For added safety, two sets of nylon screw and spacer are installed per mezzanine card.



The nylon nut, to be installed on the top of the mezzanine card

Nylon spacer

* 1. Set the CES flash memory selection switch



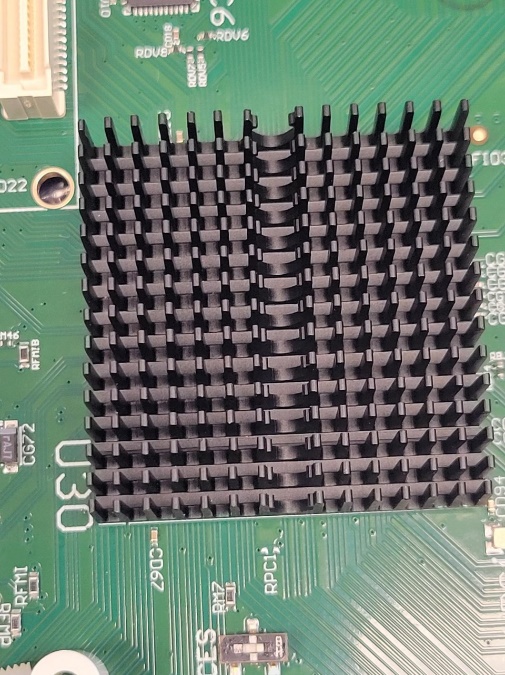
Three position switch:

Left: select Flash Memory A

Right: select flash memory B

Middle: no flash memory

* 1. Add the heat sink over the FPGA



This is the easiest step, but make sure that the heatsink will not be too close to the mezzanine card.

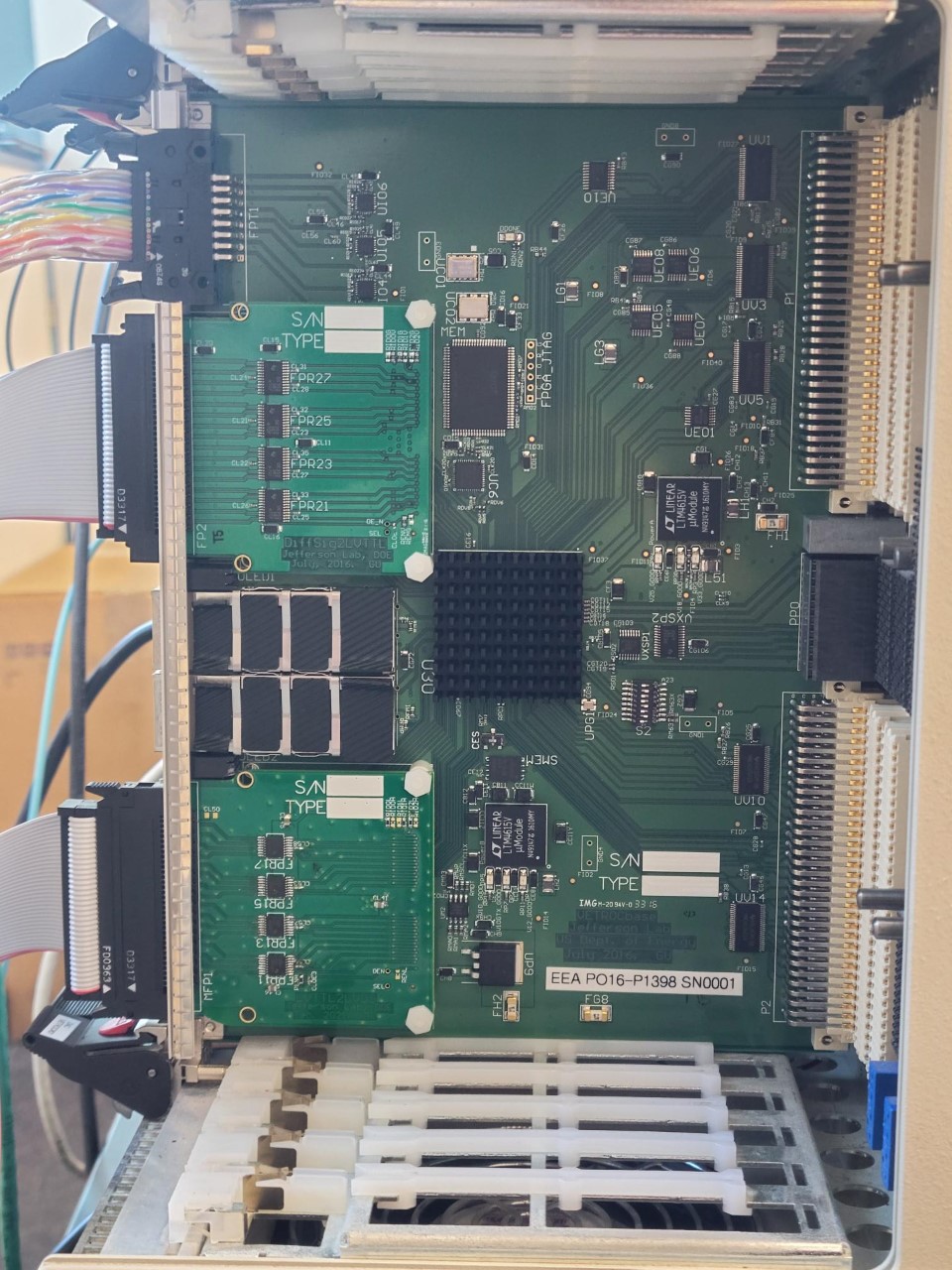
* 1. Add the QSFP shell on the VETROCIO

The same procedure as the VETROCbase board can be followed to add the QSFP shell on the VETROCIO board.

* 1. Add the VETRCIO front panel

This procedure is straightforward.

1. **Production test**
   1. 32-channel LVDS source board



A 32-channel LVDS driver card was produced for the VETROC set test. This card is the same size as the VETROC mezzanine differential signal receiver card, and it fits in the same mezzanine connector on the VETROCbase board. It is configured as “010” as the hardware ID (the VETROC mezzanine card, LVDS receiver card, is configured as “101” as the hardware ID).

When the card is plugged in the VETROC base board, the VETROCbase board can detect the hardware ID, and drives the mezzanine connector (LVTTL33).

A matching cable was produced (with 3M P50E-068 connectors on both ends) to connect the LVDS drivers to the LVDS receivers.

* 1. Production test firmware

The special firmware was developed for the VETROCbase FPGA. The firmware can automatically detect the mezzanine hardware ID. If the mezzanine is the LVDS driver, it routes the 32-bit VME register 0x78 data to the mezzanine board. If the mezzanine board is the LVDS driver, it routes the 32-bit data to VME register for readout.

The firmware is at c:\fpga\VETROCtest\VETROCtest.svf. The register map is as following:

|  |  |
| --- | --- |
| 0x28, bit(23:16) | GENIN(8:1) inputs |
| 0x60, bit(31:0) | ConnectorA inputs (top on-board) |
| 0x64, bit(31:0) | ConnectorB inputs (top mezzanine) |
| 0x68, bit(31:0) | ConnectorC inputs (bottom on-board) |
| 0x6C, bit(31:0) | ConnectorD inputs (bottom mezzanine) |
| 0x70, bit(31:0) | ConnectorE inputs (top VETROCIO) |
| 0x74, bit(31:0) | ConnectorF inputs (bottom VETROCIO) |
| 0x78, bit(31:0) | LVDS driver outputs (mezzanine hardware ID ‘010’) |
| 0c9C, bit(7:0) | GENOUT(8:1) outputs |

* 1. Production test setup

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The 68-pin cable from LVDS driver to LVDS receivers for VETROC/mezz input test.

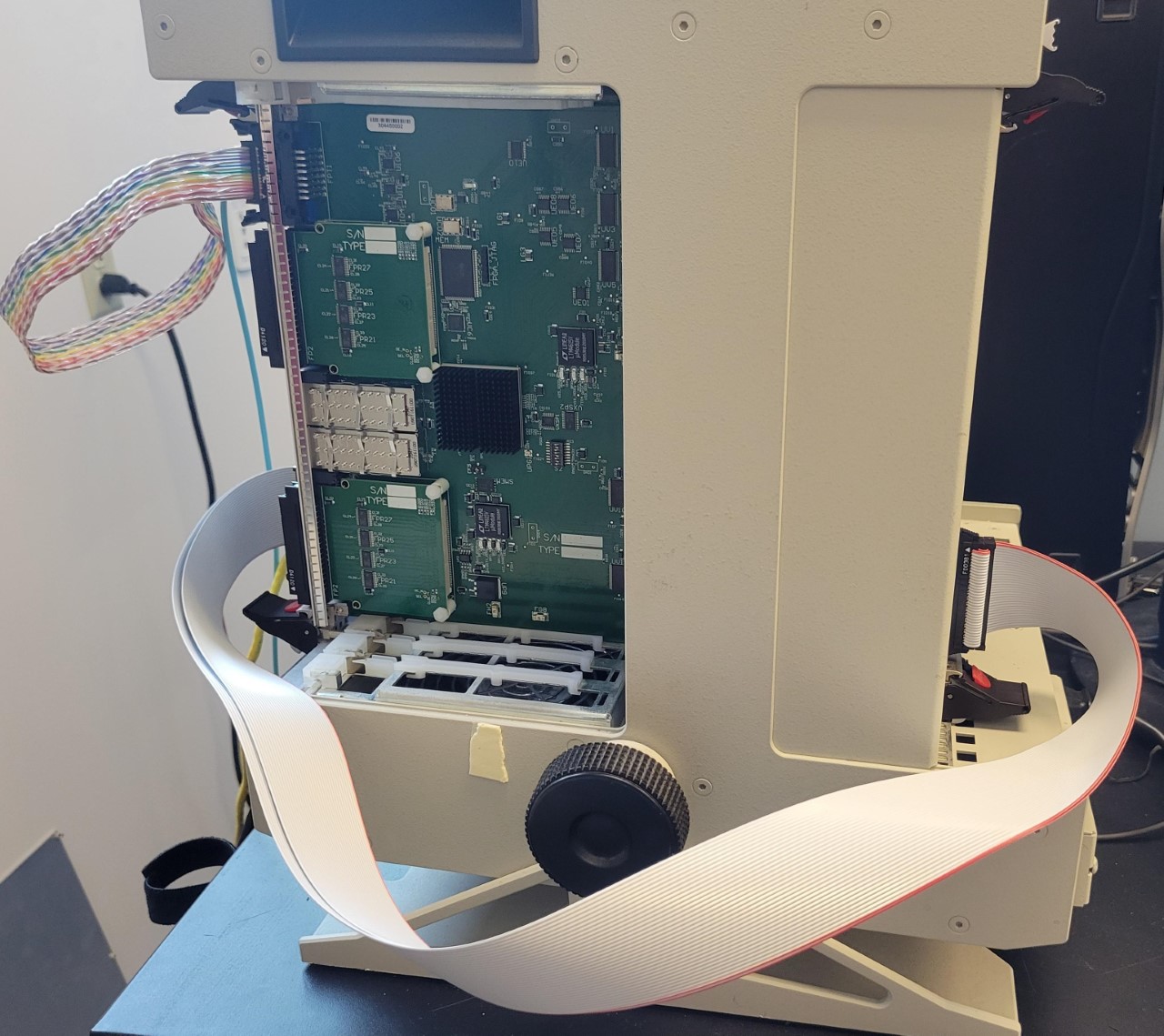
The 16-pin cable for GENOUT(8:1) to GENIN(8:1) loopback

The LVDS driver mezzanine card, and the VETROC used as LVDS signal source

The production test needs another VETROC base board loaded with the LVDS driver mezzanine card.

The 16-pin cable loopback the GENOUT(8:1) to GENIN(8:1) at the top of the front panel. The 68-pin 3M P50E cable needs to plug in/unplug from the six input connectors of the VETROC set.

The following picture is the side view of the VETROC set under test, though the VETROCIO board is hidden behind the crate back plate except the injector/ejectors.



* 1. Production test software

The test software runs on DAVW5, and located at /daqfs/home/jgu/ Trigger\_software/trigger.c.

* Linux> telnet davw5
* Davw5> ld < usrTempeDma\_AM.o
* Davw5> ld < trigger.o
* Davw5> VetrocTest(slotA, slotB) where slotA is the LVDS driver VME slot numbers; and the slotB is the VETROC under test VME slot number.

The software will load the test firmware (VETROCtest.svf), then test all the inputs. As the last step, the software will load the 192-channel high resolution TDC firmware (vfTDCV4r1.svf).

If the VETROC is used for other purposes, the user needs to flip the CES switch to the left, and load the specific firmware.

* 1. Real DAQ test, (simulate VXS crate with TI triggering)

This is a functional test using the code, not (specifically) designed for production test. After the working firmware is loaded, power cycle the crate, and then run the following:

* Linux> telnet davw5
* Davw5> ld < usrTempeDma\_AM.o
* Davw5> ld < trigger.o
* Davw5> TiFtdcTest(TI\_slot, FTDC\_slot, Nloops, BlkLevel)

where TI\_slot should be 3, FTDC\_slot should be 5 in the T-frame crate with the fake\_SD card in SW#B (right most slot of the T-frame crate).

Depending on the Ftdc front panel connection, the size of the output data file (tidsTiFtdc.dat) varies. This picture shows a typical setup.



VETROC in slot#6, with vetroc\_test firmware, and generate LVDS outputs

FTDC in slot#5, VXS payload card, Under tests

Fake\_SD card in SWB

TI in slot#3, supplies inputs to FTDC under test