

Nuclear Physics Division

*Data Acquisition Group*

# FanioDC, P2 Rear IO card

J. William Gu ([jgu@jlab.org](mailto:jgu@jlab.org))

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# Table of Contents

# Section Title Page

|  |  |  |
| --- | --- | --- |
| 1 | Introduction | 3 |
| 2 | Purpose of FanioDC Module | 3 |
| 3 | Function Description | 3 |
| 4 | Specifications | 4 |
| 5 | FanioDC operation | 5 |
| 6 | Front connector and VME P2 user pin out | 5 |
| 7 | Citation | 6 |
| Appendix A | Schematics | 7 |
| Appendix B | Fabrication Drawing | 8 |
| Appendix C | Bill of Materials | 9 |

# 1 Introduction

The P2 rear IO card (FanioDC) is being designed for Hall-B (Collaboration, 2009) upgrade. This module is responsible for connecting the trigger/clock/reset/busy signals between the TI (GU, TID design, 2009) and the FANIO (GU, FANIO, 2010) boards. Some extra functions are added to the board in case that the TI and/or the FANIO boards are not available when testing the CAEN TDC (1290). Figure 1 shows the diagram of the FanioDC in the setup.

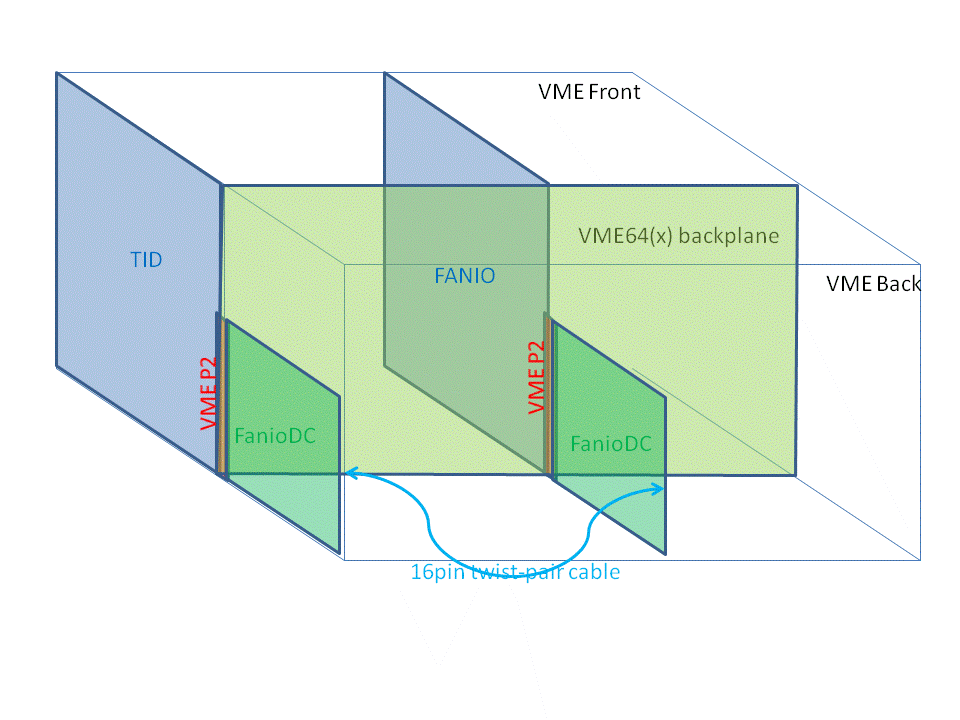
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Figure FanioDC board is located in the rear of VME64(x) crate

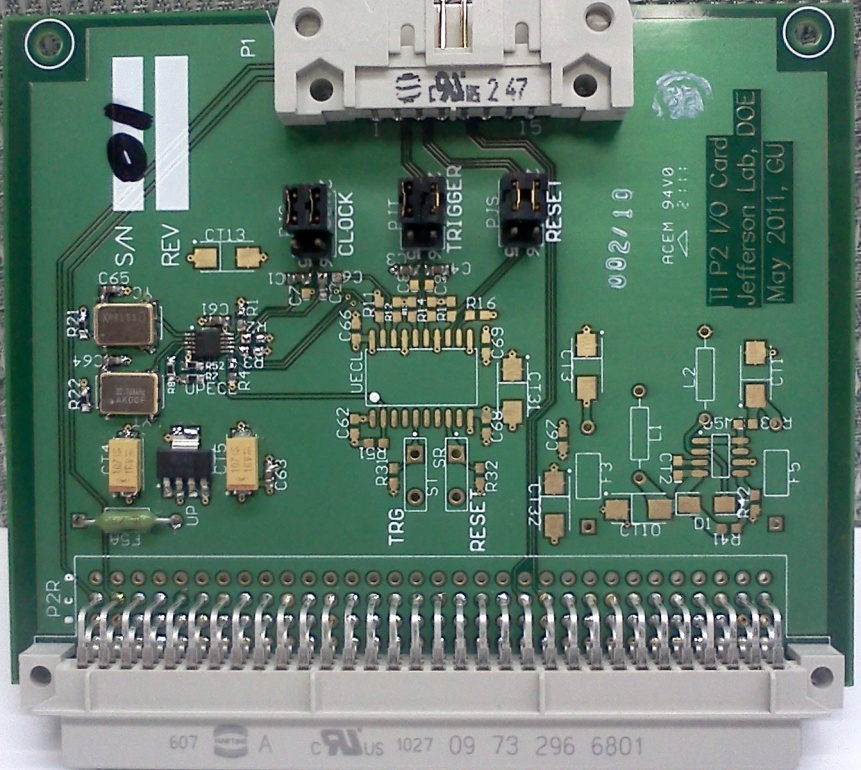


Figure FANIODC board

# 2 Purpose of the module

The main purpose is to supply an easy and robust connection between the TI and FANIO modules via their VME P2 connectors for CLOCK/TRIGGER/RESET/STATUS communication. The added function of the board makes it possible that the CAEN TDC (V1290) can be tested without the TI and/or FANIO modules.

When the FanioDC is plugged in the back of TI board, it connects the CLOCK/TRIGGER/RESET from the P2 VME connector (from TI) to the 16-pin front panel connector. The 16-pin connector can drive the CAEN TDC (V1290) directly, or connect to another FanioDC in the back of the FANIO board. The board also connects the STATUS (busy for example) from the 16-pin connector to the TI via P2 VME connector.

When the FanioDC is plugged in the back of FANIO board, it passes the CLOCK/TRIGGER/RESET from the 16-pin connector to the FANIO via P2 VME connector. It also pass the FANIO’s STATUS (busy for example) to the 16-pin connector. If there is no input at the 16-pin connector (that is there is no TI in the setup), the FanioDC can generate a 41.67 MHz clock to the FANIO board. It can generate TRIGGER and RESET via a push button. It can also generate a repetitive 32 KHz trigger, which may be too high to be useful for hall-B experiment though.

# 3 Functional Descriptions

Figure 3 shows the block diagram of the FanioDC module.

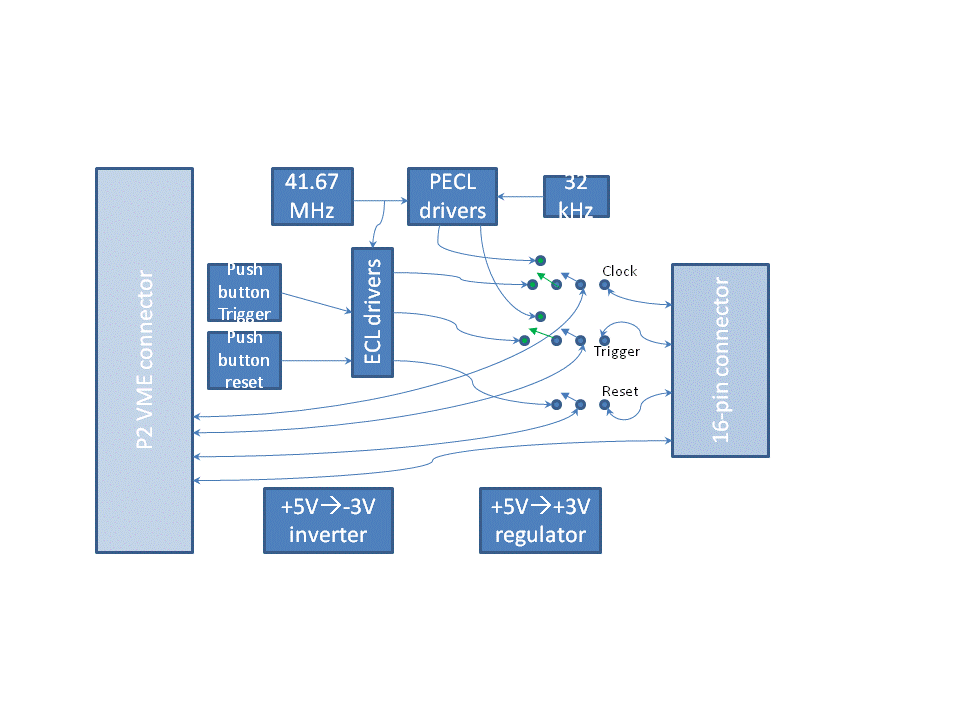


Figure : FanioDC functional diagram

The FanioDC gets its power from the P2 connector, which has +5V only. It uses a National Semiconductor’s LP3874 to lower down the voltage to +3.3V, which supply power for the CMOS output oscillators, and the PECL output drivers. It uses the Texas Instrument’s MC33063 to get -3.3V, which supplies power for the low voltage ECL drivers. The PECL clock is AC coupled to drive the FANIO, while the ECL output can be either AC or DC coupled to drive the FANIO

If the MC33063 does not work for our case here, the other option is to ‘steal’ the -3.3V supply from FANIO board via the row#A of P2 connector. This will sacrifice the independence of the FanioDC. If the clock (only the clock) is needed, the -3.3V power will not be necessary, as the PECL driver should work.

Multiple jumpers are used to select the clock/trigger/reset sources, and the routing is optimized for the direct pass through between P2 connector and the 16-pin front panel connector. The CLOCK, TRIGGER and RESET signals can be selected independently.

# 4. Specification Sheet

**4.1 Mechanical**

* Single width VME P2 rear I/O board. Size: 3Ux80mm (or 100mmX80mm).

**4.2 P2 inputs/outputs:**

* 41.67 MHz clock ECL 100 Ohm differential;
* Trigger, ECL 100 Ohm differential;
* Reset, ECL 100 Ohm differential;
* Status (busy), ECL 100 Ohm differential.
* SCL/SDA, LVTTL for I2C communication.

**4.3 Front panel inputs and outputs:**

* 41.67 MHz clock ECL 100 Ohm differential;
* Trigger, ECL 100 Ohm differential;
* Reset, ECL 100 Ohm differential;
* Status (Busy), ECL 100 Ohm differential

**4.4 Power requirements:**

* +5v @ 0.5 Amps;
* Optional -3.3V from FANIO or TI: 200mA

4.5 Environment:

* Forced air cooling;
* Commercial grade components ( 0-75 Celsius)

# 5 FanioDC operation procedure:

The FanioDC needs be properly set, and plugged into the proper crate and slot. Damage may happen to the FanioDC, the crate, or other PCBs in the crate if the right procedure is not followed.

5.1 Power supply:

The board can use (steal) -3.3V directly from the TI or FANIO. It can also generate its own -3.3V supply by a voltage inverter. If the on-board -3.3V is to be used, do not staff the fuse “F3”. If the fuse is staffed, do not staff the voltage inverter (U5M3). Anyway, the voltage inverter is preferred.

5.2 Hardware setting (jumper etc.):

5.2.1: Clock source selection (PJC setting)

|  |  |
| --- | --- |
| External (from 16-pin connector) | Short pin#1 to pin#3, short pin#2 to pin#4 |
| PECL clock | Short pin#5 to pin#3, short pin#6 to pin#4, and populate capacitors C1 and C2 |
| ECL clock | Short pin#5 to pin#3, short pin#6 to pin#4, and populate capacitors C6 and C7 |

5.2.2: Trigger source selection (PJT setting)

|  |  |
| --- | --- |
| External (from 16-pin connector) | Short pin#1 to pin#3, short pin#2 to pin#4 |
| PECL, 32kHz trigger | Short pin#5 to pin#3, short pin#6 to pin#4, and populate capacitors C3 and C4 |
| ECL, push button trigger | Short pin#5 to pin#3, short pin#6 to pin#4, and populate C8 and C9 as zero ohm resistors (DC coupling) |

5.2.3: Reset source selection (PJS setting)

|  |  |
| --- | --- |
| External (from 16-pin connector) | Short pin#1 to pin#3, short pin#2 to pin#4 |
| ECL, push button Reset | Short pin#5 to pin#3, short pin#6 to pin#4 |

6 Backplane pin out tables:

6.1 VME P2 User-defined pin table

|  |  |  |
| --- | --- | --- |
| Pin name | Signal Name | Signal Level |
| A23, A24, A25 | -3.3V | -3.3V power |
| C01 | SCL | I2C (LVTTL) |
| C02 | SDA | I2C (LVTTL) |
| C13 | CLK+ | ECL |
| C14 | CLK- | ECL |
| C17 | TRIG1+ | ECL |
| C18 | TRIG1- | ECL |
| C21 | TRIG2+ | ECL |
| C22 | TRIG2- | ECL |
| C25 | SYNC+ | ECL |
| C26 | SYNC- | ECL |
| C29 | BUSY+ | ECL |
| C30 | BUSY- | ECL |

6.2 Front panel 16-pin connector pin table

The definition is compatible with the CAEN TDC V1290.

|  |  |  |
| --- | --- | --- |
| Pin name | Signal Name | Signal Level |
| 1, 2, 11, 12 | Not used | N/A |
| 3, 4 | Trigger+, Trigger- | ECL, 100 ohm |
| 5, 6 | Reset+, Reset- | ECL, 100 ohm |
| 7, 8 | Clock+, Clock- | ECL, 100 Ohm |
| 9, 10 | Trigger2+, Trigger2- | ECL, 100 ohm |
| 13, 14 | Status+, Status- | ECL, 100 ohm |
| 15 | SCL (I2C clock) | LVTTL (CAEN no use pin) |
| 16 | SDA (I2C data) | LVTTL (CAEN no use pin) |

7. Citations:

# Works Cited

Collaboration, C. (2009). CLAS12 experiment. *Journal* , 1-25.

GU. (2010). *FANIO.* Retrieved from http://www.jlab.org/~gujh

GU. (2009). *TID design.*

##### Appendix A: design schematics

faniodc3.TIF

fanidc4.TIF

##### Appendix B: PCB layout

faniodc1.TIF

##### Appendix C: Bill of Material

FanioDC2.TIF