TS production test procedure

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Data Acquisition

1. Multimeter check:

* Check the resistance between the powers (+12 V, -12 V, +5 V, -5 V, +3.3 V, two +1 V, +1.2 V, +2.5 V, +1.8 V) and ground. The resistances should be greater than 100 Ohm.

1. Hardware setup

* Put on the alignment pin. Make sure that the alignment pin is tight and even on PCB;
* Put on the P0 connector. Nicely pressed, and evenly sit on PCB.
* Put on the heat sink for the FPGA;
* Put on the front panel;
* Set switch: S2: 10011111: SW8=1 to select on-board clock. This setting will be overwritten by FPGA; SW7=0 to set the TS in default mode, where the trigger2 output will be pulsed trigger1; SW6=0 to select firmware rev0.

1. Power up

* Plug the TS board into VXS trigger distribution crate payload slot #18. It is ok to be in other payload slot if no SD is present in the crate. All the power good LED near the power regulators should be OFF.
* Check the Voltage on the board (+12 V, -12 V, +5 V, -5 V, +3.3 V, two +1.0 V, +1.2 V, +2.5 V, +1.8 V), the voltage should be within 3% of the nominal value;
* The very top front panel LED should be OFF, the Program Done LED (near the PROM) should be ON

1. FPGA firmware loading

* Check and make sure that the ts.svf points to the correct TS FPGA firmware.
* From ‘phecda’ X-terminal, telnet to the VME6100 controller. No username or password is required to login. After login:
* >ld < usrTempeDma\_AM.o; //user defined AM code 0x19 can be used
* >ld < trigger.o; // Gu’s test software package
* >EMload(TS’ VME slot number); // load the firmware to the TS. The board type is TS, and the serial number can be read from the sticker on the PCB. These information will be saved in the PROM on the PCB. The firmware loading takes about five minutes. After the above command, the Program Done LED should be off, the LEDA#1 on the front panel should be ON, the other three LEDA on front panel should be OFF.
* >FPGAusercode(slot); //FPGA user-code shows the firmware version, and firmware type
* >PROMusercode(slot); //PROM user-code shows the board type and serial number

TStest4(TS’s slot) this is the combination of EMload, FPGAusercode and PROMusercode. Either “pass” or “fail” will be displayed at the end of the test.

1. FPGA/VME test, TI\_A output test (continue from step 4 X-terminal):

* Connect the fiber from TI\_A output to TI board (in the same crate, for VXS full sized crate with SD in place, put TI in slot#2, payload#17)
* >TSsetup(Tsslot); //setup the TS
* >TIsetup(Tislot); //setup the TI to accept TS clock, trigger and SYNC;
* >TrgStart(Tsslot); // VME trigger, The third LED should be flashing to indicate triggers;
* >tidsBERead(Tsslot); //Data readout, data file tidsBE.dat should be reasonable
* >tidsBERead(Tislot); //Data readout, data file tidsBE.dat should be reasonable and consistent with the previous data file from TS.

> TStest5(TS’s slot, TI’s slot) this is the combination of TSsetup, TIsetup, TrgStart and tidsBERead. Either “pass” or “fail” will be displayed at the end of the test.

1. FPGA/VME test, VXS P0 output test (continue from step 4 X-terminal):

* Connect the fiber from TD output to TI board
* >TSsetup(Tsslot); //setup the TS
* >TDsetup(Tdslot); //setup the TD board
* >TIsetup(Tislot); //setup the TI to accept
* >TrgStart(Tsslot); // VME trigger, The third LED should be flashing to indicate trigger
* >tidsBERead(Tsslot); //Data readout, data file tidsBE.dat should be reasonable
* >tidsBERead(Tislot); //Data readout, data file tidsBE.dat should be reasonable and consistent with the previous data file from TS.

> TStest6(TS’s slot, TD’s slot, TI’s slot) this is the combination of TSsetup, TDsetup, TIsetup, TrgStart and tidsBERead. Either “pass” or “fail” will be displayed at the end of the test.

1. TS partition test. Enable the partitions one by one. This also test the TS VXS/P0 trigger2 line:

* Connect the fiber from TD board to TI board;
* >SubTSSetup(TS’s slot); // enable the TS partition;
* >TDsetup(TD’s slot); // setup TD board;
* >TIsetup(TI’s slot); // setup TI board;
* >TrgStart(slot); // This is to enable the serial link (trigger word etc).
* >\*(0x90a80078)=0xdd; // reset the system;
* >\*(0x90a80020)=0x1000; // enable TS partition #1;
* >\*(0x90a80140)=0x491; //enable VME trigger as TS partition#1 input source
* >\*(0x90700020)=0x1004; // enable TD (in slot#14) trigger source, (trigger2), and set TD to partition #1
* >\*(0x90100020)=0x1000; //Set TI (in slot#2 or payload#17) to partition#1
* >\*(0x90a8008c)=0xffff0020; //TS partition#1 trigger 0x20=32 events.
* Check the counters on TI, TD, TS for consistency: the number of data blocks on TI/TD/TS should all match.
* Readout one block of data from TI. The number of words should be 0x90.
* Loopback over the partition#2, #3 and #4 (go back to “>\*(0x90a80078)=0xdd”)

> TStest7(TS’s slot, TD’s slot, TI’s slot) this is the combination of SubTSsetup, TDsetup, TIsetup, and looping over the four partitions with consistence check and event data check. Either “pass” or “fail” will be displayed at the end of the test.

1. TS🡪SD I2C test, and VXS/P0 busy input test:

* Connect the fiber from TD output to TI board
* >TSsetup(Tsslot); //setup the TS
* >TDsetup(Tdslot); //setup the TD board
* >TIsetup(Tislot); //setup the TI to accept
* >TrgStart(Tsslot); // VME trigger, The third LED should be flashing to indicate trigger
* >\*(0x90a80028)=0x2; // TS busy set to SD
* SD enable Busy from TD; (I2C operation on TS)
* TD busy set to 0x100, and set the block threshold to 1;
* System Sync\_reset;
* TS sends 0x100 VME trigger
* >tidsBERead(Tsslot); tidsBERead(TiSlot) //Data readout, data file tidsBE.dat should be reasonable
* >tidsBERead(Tsslot); tidsBERead(TiSlot) //Data readout, should be no data, as the threshold is set to 1.

> TStest8(TS’s slot, TD’s slot, TI’s slot) this is the combination of TSsetup, TDsetup, TIsetup, TrgStart and tidsBERead. Either “pass” or “fail” will be displayed at the end of the test.

1. TS front panel trigger input test, the Asynchronous trigger input: The generic differential output is used as the input for the trigger. A single pair differential cable is used for the test. All the fifteen inputs are enabled, and the generic outputs are enabled for about 2 minutes. This is tested by visually check the trigger LED (LEDA#3).

* Connect the TS front panel output to TS front panel input (same condo connector) using a pair of twisted cable;
* Set up TS trigger, TSsetup(islot); FPTableLoad(islot); TRGTableload(islot);
* Enable the trigger source \*(0x90300048)=0xffffffff;
* Start pulsing the front panel output “\*(0x9030004c)=0xffff; \*(0x9030004c)=0; sleep(1)”
* Move the trigger input from 1 to 2, to 3, …, to 15 and check the trigger LED. (test the asynchronous trigger inputs)
* Move the generic output from #5 to #6, to #7, …, to #12 and check the trigger LED. (test the generic outputs and VME control)

> TStest9(TS’s slot) this is the combination of TSsetup, TableLoad, and pulseLoop. Either “pass” or “fail” will be displayed at the end of the test.

1. TS front panel trigger input test, the Synchronous trigger input: The generic differential output is used as the input for the trigger. One cable connects the clock, and another single pair differential cable connects as trigger input. All the thirty inputs are enabled, and the generic outputs are enabled for about 2 minutes. This is tested by visually check the trigger LED (LEDA#3).

* Connect the TS front panel output to TS EXT front panel inputs using two pairs of twisted cables, one for clock, and another for trigger;
* Set up TS trigger, TSsetup(islot); EXTTableLoad(islot); TRGTableload(islot);
* Enable the trigger source \*(0x90300044)=0xffffffff;
* Start pulsing the front panel output “\*(0x9030004c)=0xffff; \*(0x9030004c)=0; sleep(1)”
* Move the trigger input from 1 to 2, to 3, to 4, …, to 15 and check the trigger LED.
* Move the clock and trigger input from 17 to 18, to 19, …, to 31 and check the trigger LED.

> TStest10(TS’s slot) this is the combination of TSsetup, TableLoad, and pulseLoop. Either “pass” or “fail” will be displayed at the end of the test.

1. TS VME/P2 trigger inputs (GTP inputs) test. The TI front panel FTDC connector outputs are used as the input for the TS GTP trigger inputs. One TI is set to generate 250 MHz clock, and another TI is set to generate 41.67 MHz clock. The 250 MHz is used as GTP input clock, and the 41.67 MHz (will be prescaled) is used as GTP trigger input. The thirty GTP inputs are enabled in sequence with each lasts ~10 seconds. This is tested by visually check the trigger LED (LEDA#3).

* Connect the TI front panel FTDC clock outputs to TS VME/P2 inputs using two twisted-pair cables; The 250MHz as clock, 41.67 MHz as trigger in.
* Set up TS trigger, TSsetup(islot); GTPTableLoad(islot); TRGTableload(islot);
* Start the VME/P2 trigger input prescale to 0xF (offset 0x54, 0x58, 0x5c, 0x60); (the trigger rate will be ~1.27 KHz)
* Enable the trigger source channel by channel \*(0x90300040)=(1<<iloop);
* Move the trigger input from 1 to 2, to 3, …, to 15 and check the trigger LED.
* Move the trigger input from 17 to 18, to 19, …, to 31 and check the trigger LED.

> TStest11(TS’s slot): this is the combination of TSsetup, TableLoad, and Trigger Input enable Loop. Either “pass” or “fail” will be displayed at the end of the test.

If the test fails at any step, stop and record the failure in the test summary file. The steps 1, 2 and 3 will not need a VXS crate. The steps 4, 5, 9, 10, and 11 do not require a full sized VXS crate. A T-frame crate is sufficient, and actually the T-frame crate is more convenient. The steps 6, 7 and 8 require the full sized VXS crate and SD board and TD board in place.