Introduction:

The PEPpo Helicity firmware will do the following when Bit 3 of CONFIG 1 (Run) is one:

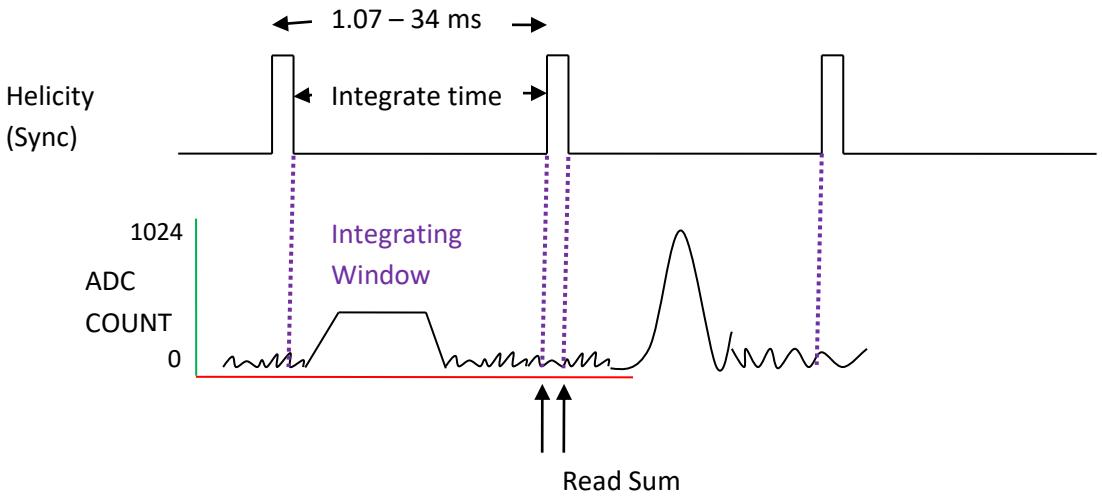
1. On falling edge of Helicity Trigger signal connected to Sync front panel input:
    a. Capture the Time Stamp (TS) .
    b. Capture and Increment the Trigger Number Counter (TN).
    c. Sum the ADC samples for all 16 channels.
2. On rising edge of Helicity Trigger signal
    a. Send TS, TN, all sixteen Sums to the Host computer.

The number of samples get added in the Sum for each trigger is depended on the Helicity window (30 – 960 Hz). In other word if the Helicity window is 30Hz, there will be 8,333,333 samples and the Maximum Sum value (for 12 bits ADC) is 3.413333×10^6. This requires 35 bits for Sum word. If the Helicity window is 960 Hz, there will be 260,416 samples. The Helicity signal and the Read Out are as shown in Figure 1.

When Run is turn on, the code wait for the Helicity Trigger signal to go high and then low before starting integration cycle. See Figure 2.

The ADC sample can be delayed by setting the ADC Sample Delay. Each count in this register delay the sample by 4nS. See Figure 3

Figure1: Helicity Trigger Signal and Read Out.



Integral = Sum of Samples inside Integrating Window from falling edge to rising edge of Helicity signal. Only Sum will be reported back.

Figure2: Config1 Bit 3 (Run) and Helicity Signal.

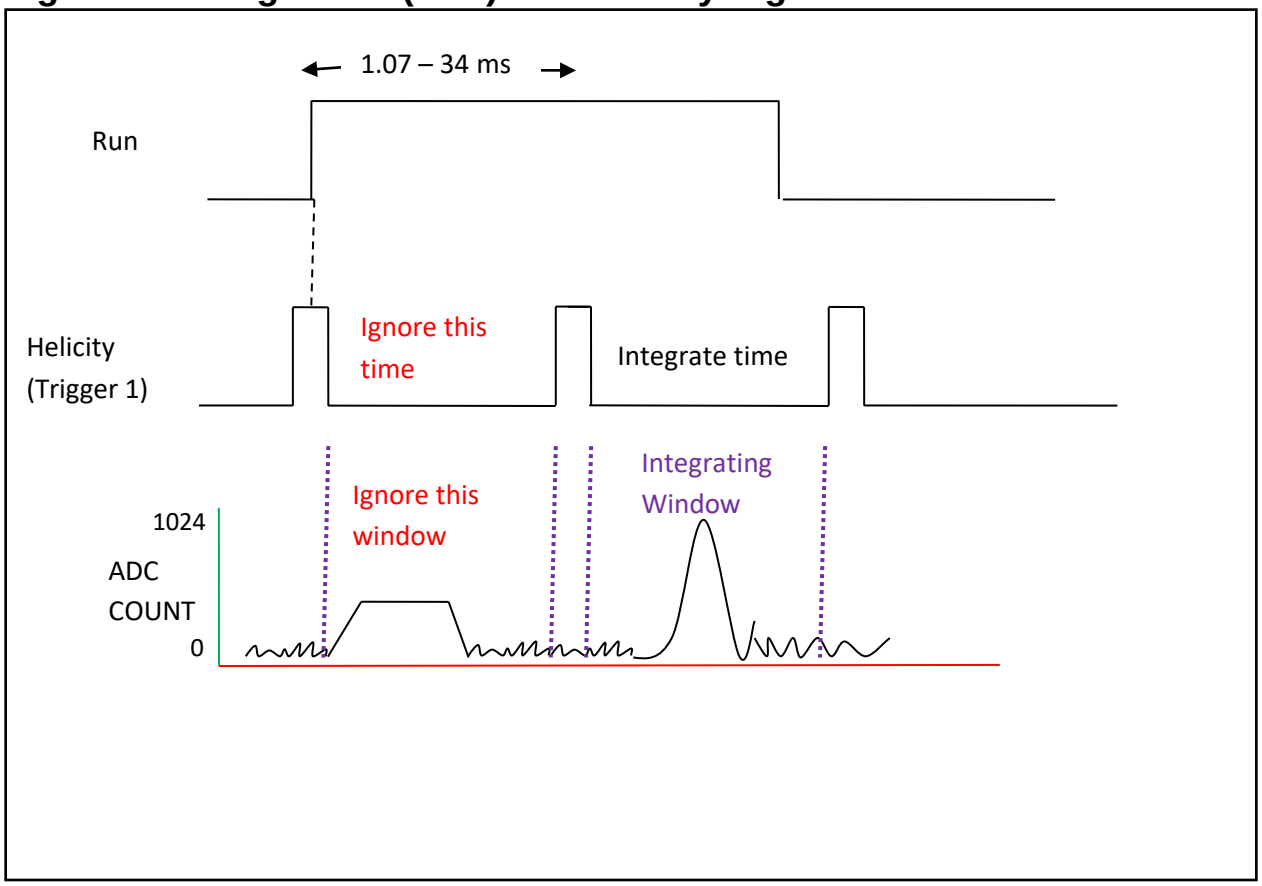
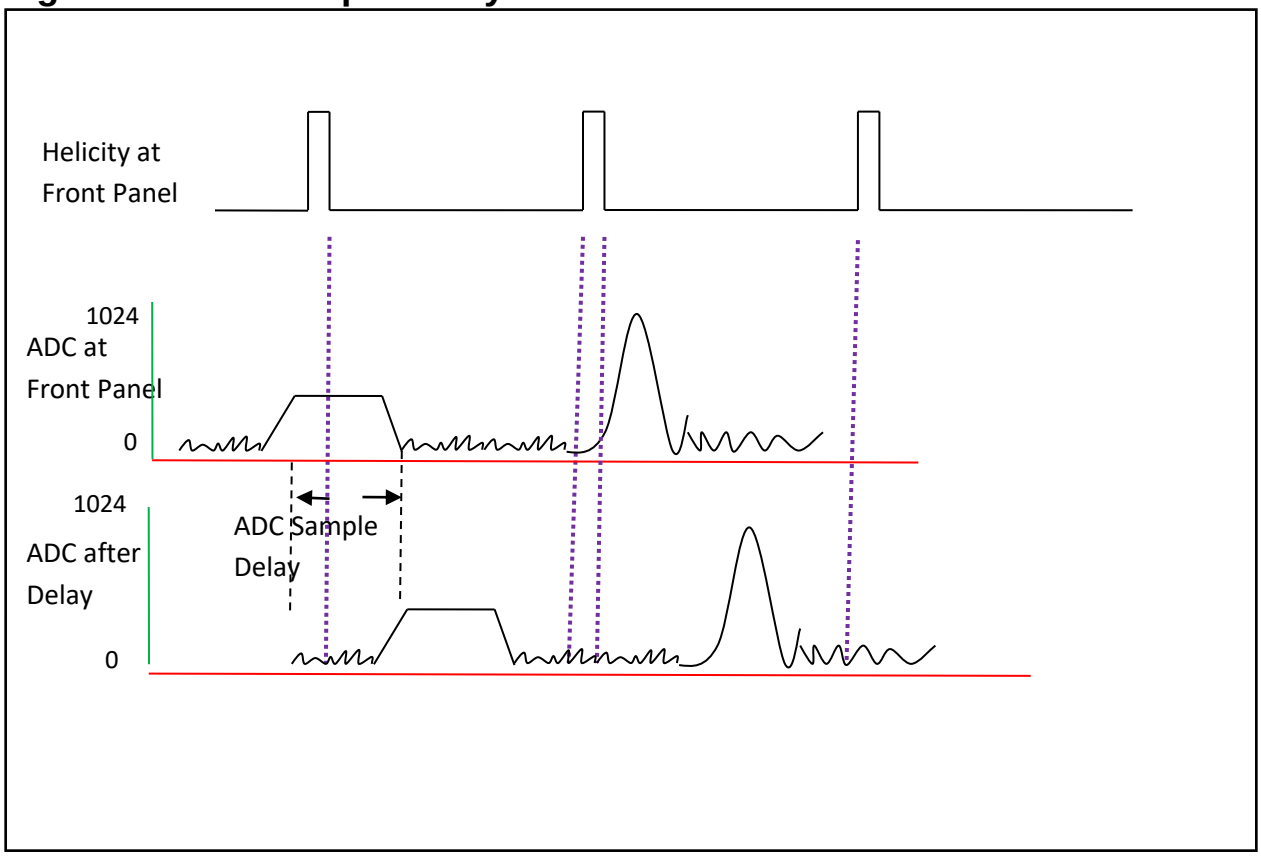


Figure 3: ADC Sample Delay.



Read Out Data Format.

Read out sequence per Event (trigger):

Event_Header (word 1) indicates the start of an event and bits are assigned as follow:
(35-32) = 1
 (31)   = 1
(30-27) = 2
(26-0) = trigger Number

Word 2 Time Stamp Upper 24 bits:
(35-32) = 0
 (31)   = 1
(30-27) = 3
(26-24) = 0
(23-0)   = Time Stamp Upper 24 bits

Word 3 Time Stamp Lower 24 bits:
(35-32) = 0
 (31)   = 0
(30-24) = 0
(23-0)   = Time Stamp lower 24 bits

Words 4,6,8,10,12,14,16,18 Sum Channel x Bits 35-32
(35-32) = 0
 (31)   = 1
(30-27) = 5
(26-23) = Channel #
(22-16) = 0
(15-0)   = Sum Bits 35-24

Word 5,7,9,11,13,15,17,19 Sum Channel x Bits 23 - 0
(35-32) = 0
 (31)   = 0
(30-24) = 0
 (23-0)   = Sum Bits 23-0

Word 20 Trailer Word
0x2E800000000

Control Bus Memory Map for FADC FPGA:

Name	Width (Bits)	Quantity	Access	Primary Address (Secondary Address)	Function
STATUS0	16	1	R	0x0000 (---)	Bits 14 to 0: Code Version Bit 15: 1= Command can be sent to AD9230
STATUS1	16	1	R	0x0001 (---)	zero
STATUS2	16	1	R	0x0002 (---)	zero
CONFIG 1	16	1	R/W	0x0003 (---)	Bit 3: 1:Run (trigger enable) Bit 12: Reset ADC IC
CONFIG 2			R/W	0x0004 (---)	When 1 ADC values = 0 Bit 0 → ADC 0 Bit 1 → ADC 1 Bit 2 → ADC 2 Bit 3 → ADC 3 Bit 4 → ADC 4 Bit 5 → ADC 5 Bit 6 → ADC 6 Bit 7 → ADC 7

					Bit 8 → ADC 8 Bit 9 → ADC 9 Bit 10→ ADC 10 Bit 11→ ADC 11 Bit 12→ ADC 12 Bit 13→ ADC 13 Bit 14→ ADC 14 Bit 15→ ADC 15
CONFIG 4	16	1		0x0005	7 => rising edge write to AD9230 ADC 6 => 1 write to all ADC 5 => 0 write to AD9230 1 read from AD9230 4 => 1 Reset ADC 3..0 => Select ADC to write to
CONFIG 5	16	1		0x0006	15..8 => Registers inside AD9230 7..0 => Data to write to register.
ADC Sample Delay	9	1		0x0008 (---)	Number of sample back from trigger point. This delay the sample to compensate for trigger path