Notes on the Caen TDC 1290 Resolution

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Introduction

In Hall D the Master Oscillator Distribution board (MO) accepts a sinusoidal control signal from the accelerator (499 MHz) and produces multiple logic level signals with frequencies that are integer divisors of the input signal frequency. The objective is to record the time of these reference signals in each detector subsystem, and thus identify the timing relationships among the subsystems. The subsystems use either the Caen TDC 1290 or JLab F1 TDC to record the times of these signals.

The selected dividing factor of 128 in Hall D produced a reference signal frequency of 3.89844 MHz (period = 256.513 ns) that was compatible with both types of TDCs. Capture windows of the TDCs were chosen large enough to include several rising edges of the periodic reference signal for each trigger.

When time differences of multiple edges within a capture window were computed for the TDC 1290, some anomalous results were found. Let *t_diff(n,1)* be the time difference between rising edge *n* and rising edge 1 in the capture window. The resolution of *t_diff(n,1)* was found to be a function of *n*. For some *n*, resolution values were significantly larger than that expected for the device (25 ps x 1.414).

Such behavior might result from jitter in the 499 MHz accelerator signal, or jitter in the distributed 3.89844 MHz reference signal, or characteristics of the TDC 1290 itself. The purpose of this study is to test the TDC 1290 in a controlled laboratory setting.

Setup

The MO module has been previously tested (F.J. Barbosa) and found to contribute a negligible amount of jitter (~ few ps) to the reference signal, so we used it with confidence in this test of the TDC 1290.

We first tried to duplicate the operating conditions in Hall D. The TDC 1290 was clocked at 41.66666666 MHz (250 MHz / 6) from an external high-precision clock generator (SRS-CG635). The 3.89844 MHz reference output of the MO was created from an input sinusoidal signal, 3V-pp @ 499.00 MHz (Agilent N5181A, jitter < 1 ps), and a dividing factor of 128. Short cables of good quality were used in all connections.

The TDC 1290 was programmed to be in high-resolution mode (~25 ps LSB). Rising edges within a capture window of 12 μs were recorded. The extended window allowed the capture of ~45 rising edges of the periodic reference signal for each trigger. A detailed study of *t_diff(n,1)* was thus possible. The actual LSB in this case was 23.4375 ps (24 ns /1024). A single channel of the TDC was tested (ch 0).

A trigger was generated internally by the TDC 1290 module with a software command. A total of 20,000 triggers were generated for each running condition. For simplicity, events were accepted for analysis only if the recorded times for all captured edges were ascending in value (i.e. no rollover events). Approximately 16,000 events satisfied this selection criterion for each run.

Results

Results for conditions matching those of Hall D are shown in **Table 1**. Note that the resolution varies with *n*, and is best when *t_diff* is very close to an integer number of 24 ns clock periods (**bold type**). *Excess* is defined as the number of LSB in the remaining fractional period. Two edges differ by an integer number of periods when *Excess* ~ 0 or ~1023. Most resolution values are significantly worse than the ~34 ps value that is expected from the LSB used.

Table 1. MO: 499 MHz, divider = 128; TDC clock = 41.6666 MHz; LSB = 23.4375 ps

Resolution: min = 27.2 ps max = 45.3 ps

n	*t_diff(n,1)* avg (LSB)	*Excess* (LSB)	σ(t_*diff*) (LSB)	Resolution (ps)
2	10944.59	705	2.32	38.5
3	21889.16	385	2.15	35.7
4	**32833.66**	**66**	**1.73**	**28.7**
5	43778.25	770	2.61	43.3
6	54722.82	451	2.13	35.3
7	65667.33	131	2.33	38.6
8	76611.91	836	2.64	43.7
9	87556.48	516	2.25	37.3
10	98501.03	197	2.67	44.3
11	109445.60	902	2.42	40.0
12	120390.15	582	2.35	39.0
13	131334.71	263	2.73	45.3
14	**142279.23**	**967**	**1.98**	**32.7**
15	153223.80	648	2.47	40.9
16	164168.37	328	2.56	42.4
17	**175112.88**	**9**	**1.64**	**27.2**
18	186057.45	713	2.59	43.0
19	197002.04	394	2.28	37.9
20	**207946.54**	**75**	**1.88**	**31.1**
21	218891.12	779	2.60	43.2
22	229835.70	460	2.09	34.6
23	240780.21	140	2.29	37.9
24	251724.78	845	2.48	41.1
25	262669.34	525	2.06	34.2
26	273613.88	206	2.55	42.2
27	284558.43	910	2.19	36.3
28	295503.01	591	2.22	36.8
29	306447.57	272	2.63	43.6
30	**317392.10**	**976**	**1.83**	**30.4**
31	328336.69	657	2.44	40.5

32	339281.25	337	2.53	41.9
33	**350225.75**	**18**	**1.72**	**28.5**
34	361170.35	722	2.67	44.2
35	372114.91	403	2.33	38.6
36	383059.42	83	2.04	33.8
37	394004.00	788	2.67	44.3
38	404948.57	469	2.17	35.9
39	415893.10	149	2.42	40.1
40	426837.65	854	2.53	41.9
41	437782.23	534	2.14	35.5
42	448726.76	215	2.57	42.6
43	459671.32	919	2.13	35.4
44	470615.91	600	2.22	36.8
45	481560.45	280	2.59	43.0

This behavior may be the result of imperfect compensation for the inherent integral nonlinearity of the TDC [1]. A compensation table loaded by the manufacturer is applied to the 1024 LSB that make up each TDC clock period (24 ns) [2]. When *t_diff* is exactly an integer number of TDC clock periods, the compensation that is applied to each edge will cancel (since the same LSB occurs for both edges). Assuming that the required compensation is a reasonably slowly changing function of LSB, edges that differ by nearly an integer number of clock periods should show a similar behavior.

We tested this hypothesis by adjusting the MO input signal to 500 MHz. The reference signal period is now 256.00 ns. Edges 4, 7, 10, 13, … differ from edge 1 by an integer number of 24 ns clock cycles (**bold type**). Results are shown in **Table 2**.

Table 2. MO: 500 MHz, divider = 128; TDC clock = 41.666 MHz; LSB = 23.4375 ps

n	*t_diff(n,1)* avg (LSB)	*Excess* (LSB)	σ(t_*diff*) (LSB)	Resolution (ps)
2	10922.67	683	2.24	37.1
3	21845.38	341	2.32	38.5
4	**32768.00**	**0**	**1.50**	**24.8**
5	43690.66	683	2.49	41.3
6	54613.36	341	2.52	41.8
7	**65535.98**	**0**	**1.75**	**29.0**
8	76458.65	683	2.55	42.3
9	87381.36	341	2.50	41.5
10	**98303.98**	**0**	**1.61**	**26.7**
11	109226.66	683	2.41	40.0
12	120149.37	341	2.32	38.4
13	**131072.00**	**0**	**1.31**	**21.8**

Results with NO compensation applied are shown in **Table 3**. Resolution has worsened significantly except for edges that differ by an integer number of TDC clock periods (**bold type**).

Table 3. MO: 500 MHz, divider = 128; TDC clock = 41.666 MHz; LSB = 23.4375 ps

(NO Compensation)

n	*t_diff(n,1)* avg (LSB)	*Excess* (LSB)	σ(t_*diff*) (LSB)	Resolution (ps)
2	10922.79	683	7.81	129.5
3	21845.58	342	7.65	126.9
4	**32767.99**	**0**	**1.50**	**24.8**
5	43690.79	683	7.90	131.0
6	54613.57	342	7.72	128.0
7	**65535.99**	**0**	**1.70**	**28.2**
8	76458.80	683	7.91	131.1
9	87381.57	342	7.70	127.7
10	**98304.00**	**0**	**1.52**	**25.2**
11	109226.79	683	7.87	130.4
12	120149.58	342	7.65	126.8
13	**131071.99**	**0**	**1.26**	**20.9**

The poorer resolution values shown in **Table 1** are most likely due to imperfect compensation for the inherent integral nonlinearity of the TDC.

Test: Effect of TDC clock frequency

It should be noted that the compensation table loaded by the manufacturer was determined when clocking the TDC at 40 MHz. Hall D and the above tests used a TDC clock frequency of 41.666 MHz (250 MHz global clock / 6). This may be a factor that contributed to the poorer resolution observed in Hall D and in **Table 1**.

To check this we repeated the measurement with the external TDC clock generator set to 40 MHz. Results are show in **Table 4**. It is clear from this data that the TDC performs at or better that the expected resolution (35 ps) across all edge differences.

Table 4. MO: 499 MHz, divider = 128; TDC clock = 40 MHz; LSB = 24.414 ps

Resolution: min = 25.1 ps max = 34.4 ps avg = 30.4 ps

n	*t_diff(n,1)* avg (LSB)	*Excess* (LSB)	σ(t_*diff*) (LSB)	Resolution (ps)
2	10506.80	267	1.48	25.6
3	21013.56	534	1.45	25.1
4	31520.34	800	1.76	30.4
5	42027.08	43	1.62	27.9

6	52533.89	310	1.86	32.2
7	63040.63	577	1.78	30.8
8	73547.41	843	1.96	33.8
9	84054.18	86	1.86	32.2
10	94560.98	353	1.99	34.4
11	105067.73	620	1.93	33.3
12	115574.50	887	1.95	33.7
13	126081.29	129	1.90	32.7
14	136588.07	396	1.87	32.3
15	147094.83	663	1.87	32.3
16	157601.59	930	1.76	30.4
17	168108.38	172	1.80	31.0
18	178615.14	439	1.64	28.2
19	189121.93	706	1.73	29.8
20	199628.68	973	1.52	26.2
21	210135.48	215	1.72	29.7
22	220642.24	482	1.56	26.9
23	231149.01	749	1.75	30.2
24	241655.77	1016	1.51	26.1
25	252162.55	259	1.78	30.8
26	262669.32	525	1.65	28.5
27	273176.11	792	1.88	32.5
28	283682.84	35	1.70	29.3
29	294189.65	302	1.91	33.0
30	304696.41	568	1.79	30.9
31	315203.19	835	1.93	33.3
32	325709.94	78	1.77	30.6
33	336216.73	345	1.91	33.0
34	346723.51	612	1.83	31.6
35	357230.27	878	1.84	31.8
36	367737.05	121	1.80	31.0
37	378243.82	388	1.78	30.8
38	388750.59	655	1.78	30.8
39	399257.35	921	1.74	30.0
40	409764.14	164	1.79	30.9
41	420270.92	431	1.68	29.0
42	430777.67	698	1.78	30.7
43	441284.43	964	1.61	27.7
44	451791.22	207	1.80	31.0
45	462297.99	474	1.65	28.5
46	472804.78	741	1.83	31.6
47	483311.51	1008	1.61	27.9

To check that these results are not an artifact of a subtle relationship between the period of the TDC clock and the edge period of the MO, the dividing factor of the MO was changed from 128 to 124. Results are shown in **Table 5**. The excellent performance of the TDC is repeated.

Table 5. MO: 499 MHz, divider = 124; TDC clock = 40 MHz; LSB = 24.414 ps

Resolution: min = 24.3 ps max = 34.5 ps avg = 30.2 ps

n	*t_diff(n,1)* avg (LSB)	*Excess* (LSB)	σ(t_*diff*) (LSB)	Resolution (ps)
2	10178.44	962	1.65	28.5
3	20356.88	901	1.89	32.6
4	30535.33	839	1.72	29.7
5	40713.75	778	1.80	31.1
6	50892.18	716	2.00	34.5
7	61070.62	655	1.78	30.8
8	71249.06	593	1.57	27.1
9	81427.49	531	1.75	30.2
10	91605.91	470	1.74	30.0
11	101784.35	408	1.56	27.0
12	111962.81	347	1.84	31.8
13	122141.23	285	1.98	34.1
14	132319.67	224	1.75	30.3
15	142498.12	162	1.76	30.4
16	152676.56	101	1.85	32.0
17	162854.99	39	1.59	27.5
18	173033.40	1001	1.41	24.3
19	183211.83	940	1.77	30.5
20	193390.27	878	1.88	32.4
21	203568.73	817	1.72	29.7
22	213747.15	755	1.85	31.9
23	223925.58	694	1.94	33.5
24	234104.03	632	1.67	28.9
25	244282.48	570	1.59	27.4
26	254460.89	509	1.72	29.6
27	264639.32	447	1.68	29.0
28	274817.78	386	1.64	28.4
29	284996.21	324	1.87	32.3
30	295174.64	263	1.91	33.0
31	305353.09	201	1.75	30.2
32	315531.52	140	1.76	30.4
33	325709.95	78	1.76	30.5
34	335888.40	16	1.50	25.9
35	346066.82	979	1.52	26.2

36	356245.25	917	1.82	31.3
37	366423.71	856	1.83	31.7
38	376602.13	794	1.78	30.8
39	386780.57	733	1.89	32.7
40	396958.98	671	1.86	32.1
41	407137.44	609	1.66	28.7
42	417315.87	548	1.61	27.9
43	427494.30	486	1.70	29.3
44	437672.74	425	1.67	28.8
45	447851.18	363	1.75	30.2
46	458029.63	302	1.89	32.6
47	468208.05	240	1.84	31.7
48	478386.49	178	1.77	30.6
49	488564.98	117	1.75	30.2

To be complete, we repeated the original measurement (**Table 1**) with a dividing factor of 124. Results are shown in **Table 6**. The poor resolution is consistent with data obtained with a dividing factor of 128.

Table 6. MO: 499 MHz, divider = 124; TDC clock = 41.6666 MHz; LSB = 23.4375 ps

Resolution: min = 24.1 ps max = 44.9 ps

n	*t_diff(n,*1) avg (LSB)	*Excess* (LSB)	σ(t_*diff*) (LSB)	Resolution (ps)
2	10602.52	363	2.34	38.7
3	21205.08	725	2.62	43.4
4	**31807.58**	**64**	**1.78**	**29.5**
5	42410.14	426	2.11	35.0
6	53012.70	789	2.71	44.9
7	63615.20	127	2.32	38.5
8	74217.74	490	1.97	32.7
9	84820.30	852	2.55	42.2
10	95422.79	191	2.63	43.5
11	106025.38	553	1.98	32.8
12	116627.92	916	2.15	35.7
13	127230.43	254	2.69	44.5
14	137832.99	617	2.16	35.8
15	**148435.52**	**980**	**1.62**	**26.8**
16	159038.04	318	2.55	42.3
17	169640.59	681	2.46	40.8
18	**180243.11**	**19**	**1.46**	**24.1**
19	190845.65	382	2.26	37.5
20	201448.21	744	2.67	44.3
21	**212050.71**	**83**	**1.93**	**32.0**

22	222653.27	445	2.06	34.1
23	233255.83	808	2.65	43.9
24	243858.32	146	2.43	40.3
25	254460.88	509	2.02	33.5
26	265063.43	871	2.43	40.3
27	275665.93	210	2.65	43.9
28	286268.49	572	2.04	33.9
29	296871.04	935	2.00	33.2
30	307473.57	274	2.64	43.7
31	318076.13	636	2.25	37.4
32	**328678.66**	**999**	**1.55**	**25.7**
33	339281.17	337	2.45	40.6
34	349883.76	700	2.50	41.4
35	**360486.25**	**38**	**1.64**	**27.2**
36	371088.80	401	2.19	36.3
37	381691.35	763	2.66	44.1
38	392293.84	102	2.12	35.2
39	402896.40	464	2.04	33.8
40	413498.95	827	2.59	42.9
41	424101.44	165	2.49	41.3
42	434704.01	528	2.06	34.2
43	445306.59	891	2.32	38.5
44	455909.07	229	2.62	43.4
45	466511.63	592	2.13	35.2
46	**477114.19**	**954**	**1.88**	**31.2**
47	487716.78	293	2.57	42.6

Recommendation: We should attempt to generate new compensation tables (1 per channel) for the TDC 1290 clocked at 41.666 MHz.

Test: Effect of a long cable on TDC resolution

We tested a 130 ft. twinax cable between the MO output and the TDC input to see if there is any degradation in resolution. The cable is the same type used in Hall D to distribute the reference signals from the MO. We performed the test with a TDC clock frequency of 40 MHz to isolate cable length as the only factor that can cause resolution change.

As a reference, a short cable run was made to confirm that the test system was stable and could reproduce results made several days earlier. **Table 7** illustrates TDC performance equivalent to that of **Tables 4** and **Tables 5**.

Table 7. MO: 499 MHz, divider = 128; TDC clock = 40 MHz; LSB = 24.414 ps

(short cable – average resolution = 29.7 ps)

n	*t_diff(n,1)* avg (LSB)	*Excess* (LSB)	σ(t_*diff*) (LSB)	Resolution (ps)
2	10506.80	267	1.48	25.5
3	21013.55	534	1.44	24.8
4	31520.32	800	1.65	28.5
5	42027.07	43	1.44	24.8
6	52533.88	310	1.67	28.8
7	63040.66	577	1.57	27.0
8	73547.44	843	1.74	30.1
9	84054.19	86	1.66	28.6
10	94560.98	353	1.77	30.6
11	105067.74	620	1.75	30.2
12	115574.52	887	1.80	31.0
13	126081.32	129	1.80	31.2
14	136588.07	396	1.81	31.3
15	147094.84	663	1.86	32.2
16	157601.61	930	1.82	31.4
17	168108.39	172	1.90	32.8
18	178615.14	439	1.81	31.2
19	189121.94	706	1.91	33.0
20	199628.68	973	1.74	30.0
21	210135.48	215	1.90	32.7
22	220642.24	482	1.73	29.9
23	231149.03	749	1.88	32.4
24	241655.77	1016	1.64	28.3
25	252162.55	259	1.84	31.8
26	262669.31	525	1.67	28.8
27	273176.10	792	1.85	31.9
28	283682.86	35	1.64	28.3
29	294189.66	302	1.80	31.1

30	304696.42	568	1.66	28.6
31	315203.20	835	1.79	30.9
32	325709.96	78	1.63	28.2
33	336216.75	345	1.76	30.3
34	346723.52	612	1.69	29.2
35	357230.29	878	1.73	29.8
36	367737.06	121	1.69	29.2
37	378243.83	388	1.70	29.3
38	388750.61	655	1.72	29.8
39	399257.37	921	1.69	29.2
40	409764.14	164	1.75	30.2
41	420270.89	431	1.65	28.5
42	430777.70	698	1.75	30.2
43	441284.44	964	1.59	27.5
44	451791.24	207	1.77	30.5
45	462298.00	474	1.63	28.1
46	472804.79	741	1.78	30.8
47	483311.52	1008	1.54	26.5

Table 8 shows results from the long cable test. Resolution is degraded only slightly compared to the short cable results.

Table 8. MO: 499 MHz, divider = 128; TDC clock = 40 MHz; LSB = 24.414 ps

(130 ft. cable – average resolution = 31.3 ps)

n	*t_diff(n,1)* avg (LSB)	*Excess* (LSB)	σ(t_*diff*) (LSB)	Resolution (ps)
2	10506.77	267	1.74	30.1
3	21013.55	534	1.97	33.9
4	31520.34	800	1.86	32.1
5	42027.10	43	1.61	27.8
6	52533.87	310	1.79	30.9
7	63040.64	577	1.91	33.0
8	73547.42	843	1.88	32.5
9	84054.18	86	1.68	29.0
10	94560.97	353	1.80	31.1
11	105067.74	620	1.97	34.0
12	115574.50	886	1.91	32.9
13	126081.27	129	1.78	30.7
14	136588.04	396	1.81	31.3
15	147094.82	663	1.90	32.9

16	157601.59	930	1.88	32.4
17	168108.37	172	1.78	30.8
18	178615.13	439	1.77	30.5
19	189121.92	706	1.85	32.0
20	199628.67	973	1.81	31.3
21	210135.45	215	1.76	30.5
22	220642.23	482	1.75	30.3
23	231149.02	749	1.84	31.8
24	241655.77	1016	1.74	30.1
25	252162.54	259	1.74	30.0
26	262669.32	525	1.71	29.6
27	273176.10	792	1.83	31.6
28	283682.87	35	1.78	30.8
29	294189.63	302	1.77	30.6
30	304696.39	568	1.76	30.3
31	315203.20	835	1.84	31.8
32	325709.94	78	1.82	31.4
33	336216.73	345	1.84	31.7
34	346723.51	612	1.80	31.1
35	357230.27	878	1.85	32.0
36	367737.06	121	1.88	32.5
37	378243.82	388	1.84	31.8
38	388750.59	655	1.81	31.3
39	399257.36	921	1.84	31.8
40	409764.15	164	1.88	32.4
41	420270.90	431	1.82	31.4
42	430777.68	698	1.80	31.1
43	441284.43	964	1.76	30.5
44	451791.24	207	1.83	31.7
45	462297.99	474	1.81	31.2
46	472804.75	741	1.78	30.7
47	483311.53	1008	1.71	29.5

Integral Nonlinearity (INL)

The designers of the HPTDC believe that the INL observed in high resolution and very high resolution modes is caused by crosstalk from the logic part of the chip [1]. Because it is stable the nonlinearity can be compensated for by a look up table (LUT). The curve is periodic so the LUT will cover only the bins in a clock period.

A code density test is used to measure the timing non-linearity of a single channel of an HPTDC chip. A code density test is a statistical test that can be used to identify the relative widths of the timing bins. A large number of hits that are random in time are generated. If the generated hits are asynchronous with the clock of the HPTDC and all time bins are equally wide, then each bin of a histogram of the number of hits per timing bin will have the same number of entries. However, if the time bins vary in width, the histogram bins for wider time bins will collect relatively more hits than the histogram bins for narrow time bins. In very high resolution mode there are 1024 bins per clock cycle so only the lowest 10 bits of the reported TDC time (21 bits) are utilized in binning the data for the code density test.

Define the following:

$n(i)$ = number of hits in bin i (i = 0 - 1023)

$$N(k) = \sum_{i=0}^{k-1} n(i) \quad (k = 1 - 1023), \quad N(0) = 0$$

N_{Total} = total number of hits

For perfect bins of uniform width, each bin would have a count close to $N_{Total}/1024$. Set the sum $N(k)$ of k actual bins equal to the sum of kp uniform bins (where kp is permitted to have a fractional part):

$$N(k) = kp\, N_{Total}/1024$$

$$kp = 1024\, N(k) / N_{Total}$$

We define the integral nonlinearity as:

$$INL(k) = k - kp$$

In the INL test setup TDC hits are generated with a random pulse generator (BNC DB-2 and 8010) set to an average rate of about 1 MHz. Triggers at a rate of 9,999 Hz are generated with a separate pulse generator. A 6 us capture window programmed into the TDC ensures that the most of the triggers will have at least one hit recorded. To protect against any unexpected time correlations between consecutive hits captured in the window, only the *first* hit detected in the window is used in the INL analysis. As in earlier tests, the TDC 1290 is clocked with an external high-precision clock generator (SRS-CG635). About 30M or more TDC hits were recorded in each INL test. For equal width bins the average bin population is about 30K, so statistical fluctuations alone (<1%) have negligible effect on the INL measurements.

Figure 1 shows the measured INL of a single TDC channel clocked at three different frequencies. Compensation from the table stored on the TDC 1290 module is turned OFF. Clearly the INL of the HPTDC chip is frequency dependent. Note that in this Figure and ALL Figures below, the vertical appearing lines are simply data connector lines, not error bars. However, the level of raggedness in the INL data can be taken as a measure of the uncertainty in the INL computations.

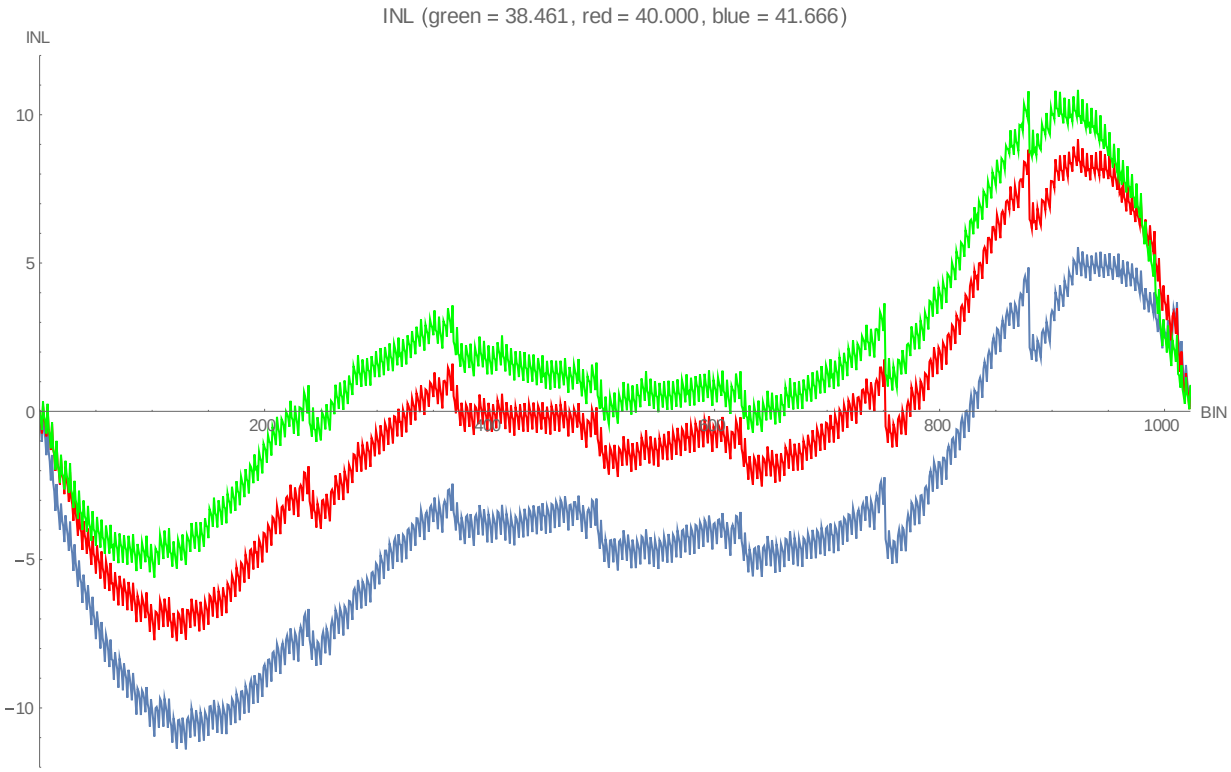

Figure 1. INL dependence on TDC clock frequency. (Green = 38.461 MHz, Red = 40.00 MHz, Blue = 41.666 MHz)

The INL data (*INL(k), k=0 – 1023*) is written to a file and can be used to compensate for INL in subsequent data runs. Let *time* be a reported TDC hit (21 bits). Explicitly:

$k = time \;\&\; (0x3FF)$ (bin within clock cycle)

$kp = \text{round}\,(k - INL(k))$ (corrected bin - round to nearest integer)

$time' = (time \;\&\; (0x1FFC00)) \mid kp$ (compensated time)

or simply

$time' = time - \text{round}\,(INL(k))$

INL Results

Figure 2 shows the measured INL of a TDC channel clocked at 41.666 MHz. Compensation is applied from the table stored on the TDC 1290 module. Note that the table compensation values were determined by CAEN while clocking the module at **40.00 MHz**. Clearly the compensation is inadequate. Time difference errors of up to ~100 ps (4 bins) can occur.

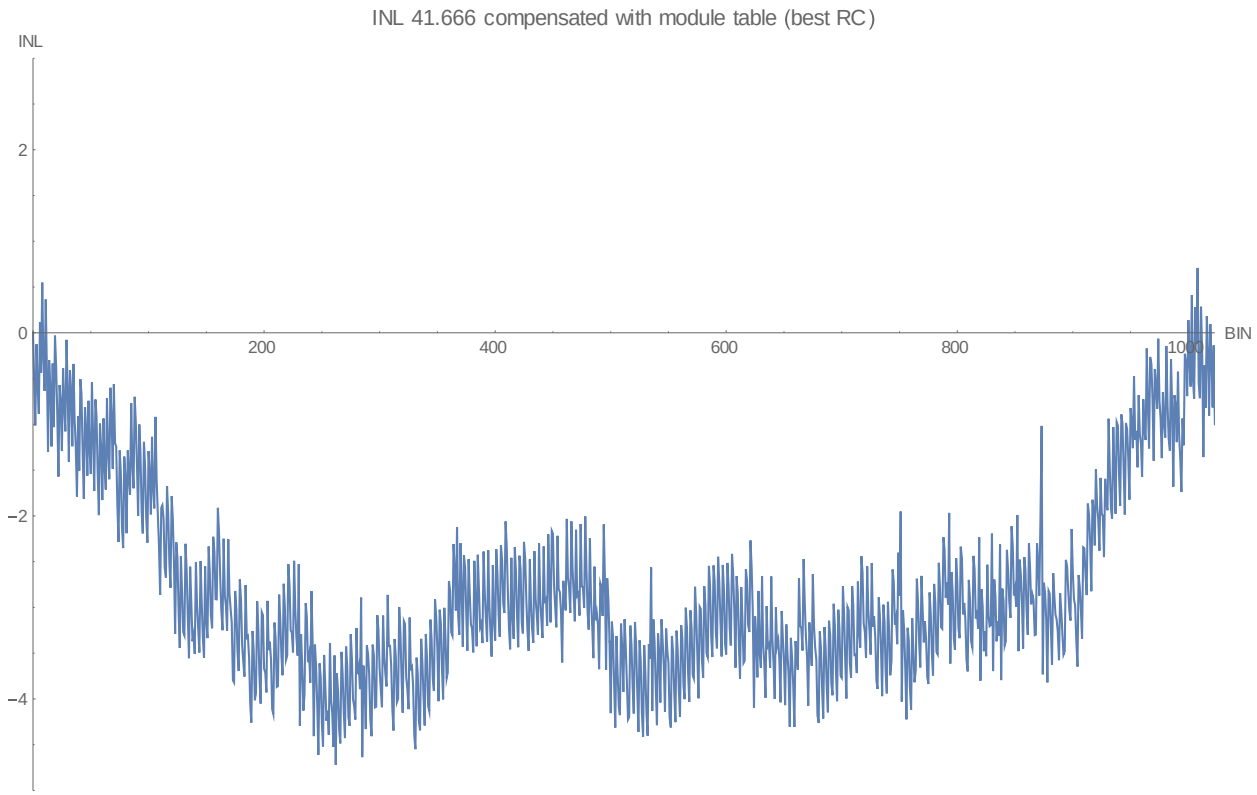

Figure 2. INL @ 41.666 MHz after compensation with module table.

Figure 3 shows the measured INL of a TDC channel clocked at 40.00 MHz. Compensation is applied from the table stored on the TDC 1290 module. The compensation is significantly better than at 41.666 MHz.

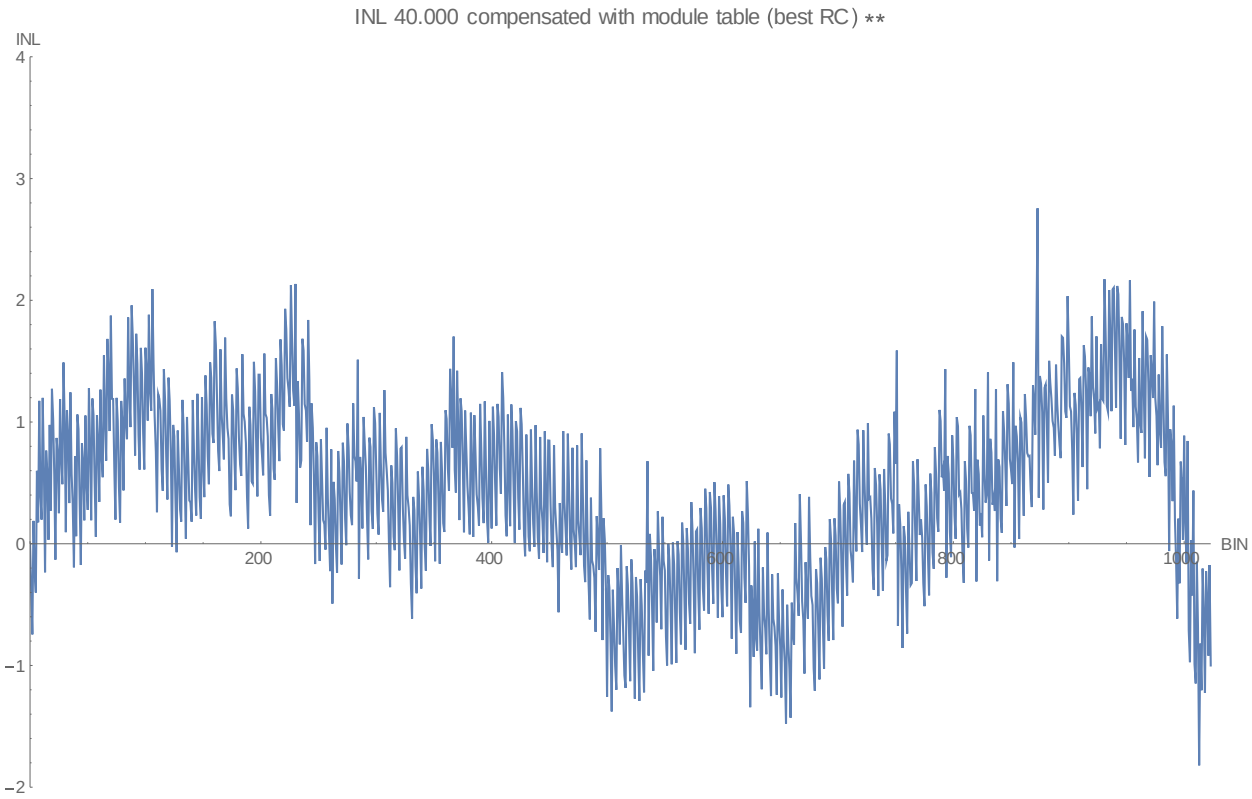

Figure 3. INL @ 40.000 MHz after compensation with module table.

Figure 4 shows the measured INL of a TDC channel clocked at 40.00 MHz. The module's compensation table is turned OFF. Compensation from an external table obtained in a separate run as described above is applied. Results are excellent.

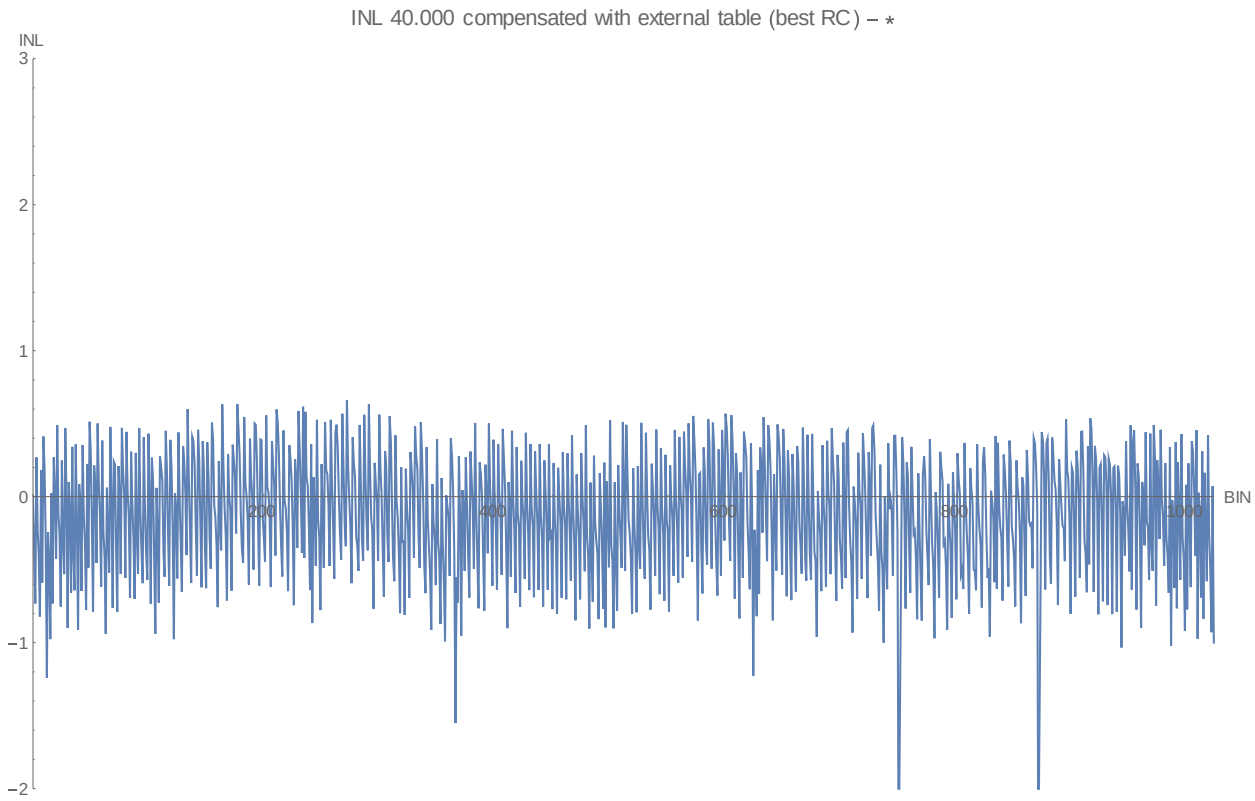

Figure 4. INL @ 40.000 MHz after compensation with external table.

Figure 5 shows the measured INL of a TDC channel clocked at 41.666 MHz. The module's compensation table is turned OFF. Compensation from an external table obtained in a separate run as described above is applied. Results are excellent.

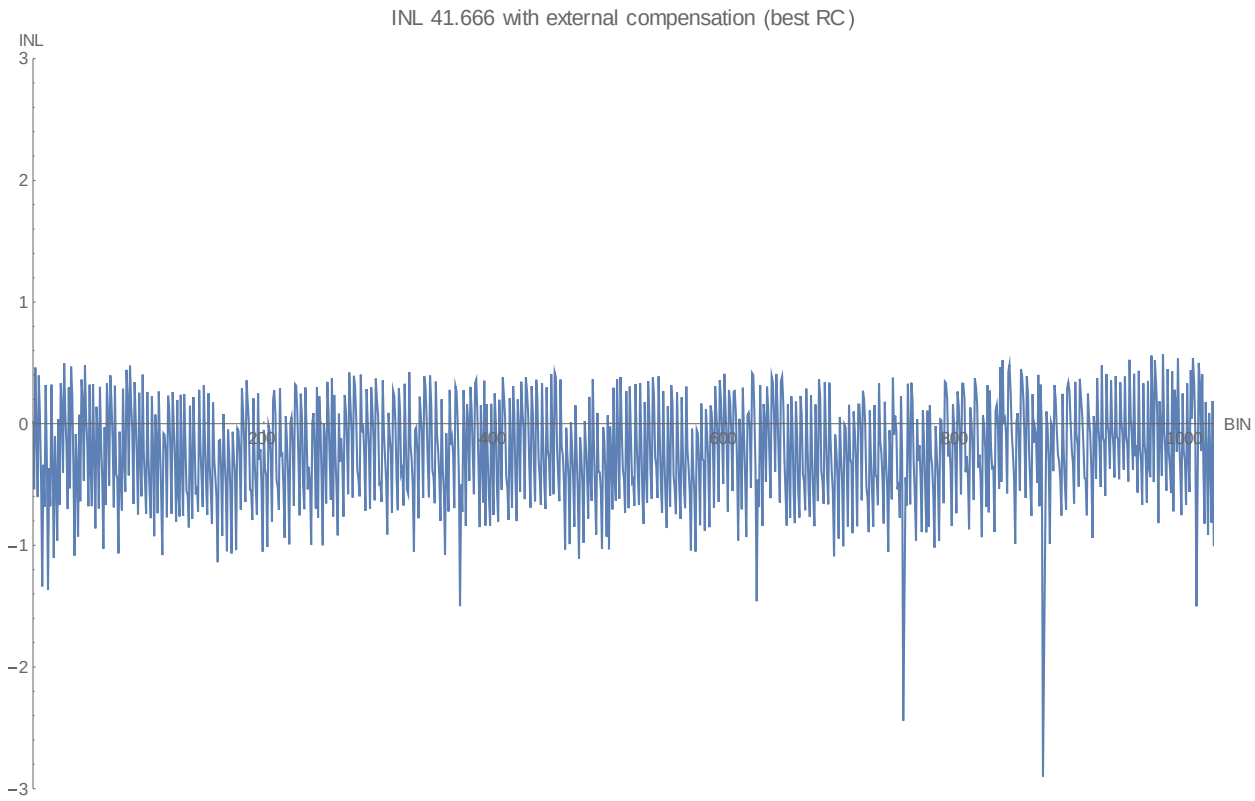

Figure 5. INL @ 41.666 MHz after compensation with external table.

Master Oscillator Results with the Reference Signal

The 3.89844 MHz reference output of the MO was again applied to the TDC channel. The INL data for this channel was determined by the code density test as described above. Compensation based on that data was applied instead of using the module's internal table. The results are shown in **Table 9** and are quite different from those of **Table 1** (internal table compensation). There is no significant variation of resolution with *n*, and the average resolution value is good.

Table 9. MO: 499 MHz, divider = 128; TDC clock = 41.6666 MHz; LSB = 23.4375 ps (external compensation)

Resolution: min = 28.8 ps max = 35.9 ps avg = 33.1 ps

n	*t_diff(n,1)* avg (LSB)	*Excess* (LSB)	σ(t_*diff*) (LSB)	Resolution (ps)
2	10944.54	705	1.88	31.2
3	21889.13	385	2.07	34.3
4	32833.66	66	1.82	30.2
5	43778.20	770	2.14	35.5
6	54722.78	451	2.16	35.9
7	65667.34	131	2.00	33.2
8	76611.88	836	2.09	34.6
9	87556.43	516	2.10	34.9
10	98501.01	197	2.01	33.4
11	109445.54	902	1.87	31.0
12	120390.08	582	2.04	33.9
13	131334.67	263	2.02	33.5
14	142279.20	967	1.74	28.8
15	153223.75	648	2.07	34.4
16	164168.36	328	2.09	34.7
17	175112.88	9	1.75	29.0
18	186057.42	713	2.13	35.2
19	197002.01	394	2.10	34.9
20	207946.55	75	1.82	30.2
21	218891.08	779	2.08	34.6
22	229835.65	460	2.07	34.3
23	240780.21	140	1.90	31.5
24	251724.74	845	1.98	32.7
25	262669.30	525	2.04	33.7
26	273613.88	206	2.01	33.3
27	284558.41	910	1.86	30.8
28	295502.95	591	2.07	34.4
29	306447.56	272	2.09	34.7
30	317392.09	976	1.78	29.5

31	328336.62	657	2.11	35.0
32	339281.23	337	2.10	34.8
33	350225.75	18	1.74	28.9
34	361170.30	722	2.10	34.8
35	372114.88	403	2.07	34.3
36	383059.41	83	1.80	29.8
37	394003.95	788	2.05	34.0
38	404948.53	469	2.05	33.9
39	415893.09	149	1.91	31.6
40	426837.63	854	1.97	32.7
41	437782.17	534	2.08	34.4
42	448726.75	215	2.05	33.9
43	459671.29	919	1.87	31.1
44	470615.84	600	2.11	34.9
45	481560.43	280	2.10	34.8

RC Delay Line Calibration

The very high resolution of the TDC is obtained by performing multiple sampling of the DLL signals, controlled from a precisely calibrated delay line **(Figure 6**) [2]. The interpolation within a DLL cell is obtained by sampling the DLL signals four times, equally spaced over the interval of a delay cell (using four cascaded TDC channels in order to obtain one *very high* resolution channel). The sampling signals should have very small delays (~25 ps) and high precision and stability. This is done using an R-C delay line having small dependencies on temperature and supply voltage. On-chip interpolation is performed over the measurements to compress them into one single very high resolution time measurement.

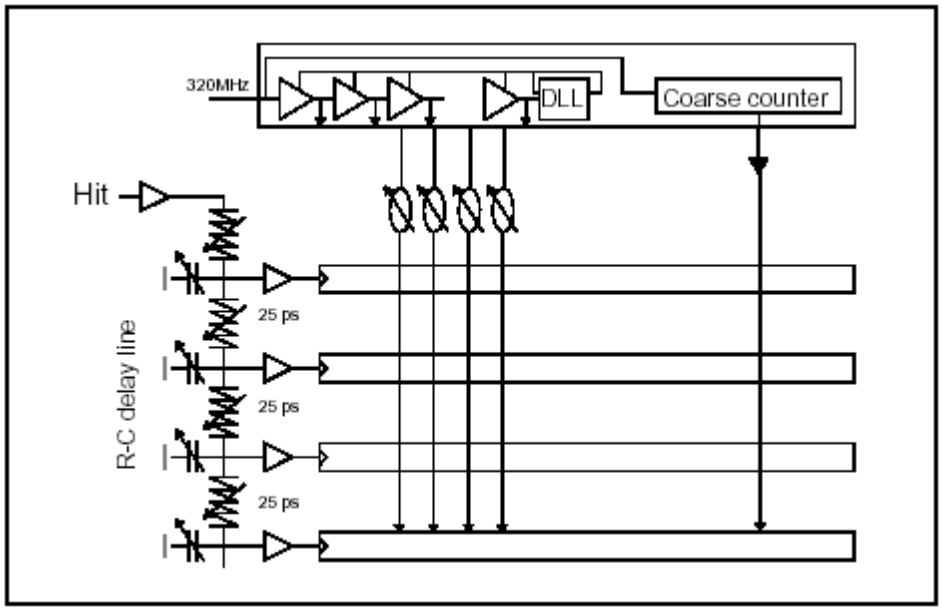

Figure 6. R-C delay lines in Very High resolution mode

Because there are process variations of the R-C delay line, a calibration of its parameters should be done. The calibration constant is limited to 4 x 3 bits used to control the four sampling taps from the R-C delay line. The constant is shared by the 8 very high resolution channels of the chip.

A code density test can be performed on the lowest 2 bits of reported hit times to estimate the best calibration constant. Since the calibration constant is shared across the chip, hits from all 8 channels contribute to a single code density histogram. Some effort should be made to ensure that the channels contribute in roughly equal amounts. A flat histogram is the ideal result. A quantitative measure of flatness is described below.

$n(i)$ = number of hits in bin i (i = 0 - 3)

$N_{Total} = n(0) + n(1) + n(2) + n(3)$

$d(i) = \text{ABS}((n(i) / N_{Total}) - 0.25)$

$d_{Total} = d(0) + d(1) + d(2) + d(3)$ (total deviation)

The best RC calibration constant should minimize the total deviation, d_{Total}. The 4096 possible RC constant values can tried with an automated process, and the optimum value reported.

It has been observed that if an RC calibration is performed *without* an INL correction applied to the hits, no reasonable degree of flatness can be achieved. In particular, bin 2 had only a fraction (10%) of the hits of the other bins no matter what RC constant was used.

For the 41.666 MHz results shown above (**Figure 5**), the best RC constant was chosen while applying the compensation table stored on the module and clocking the module at 41.666 MHz. The INL data at 41.666 MHz was then collected using this RC calibration value.

References

1. HPTDC – High Performance Time to Digital Converter, Version 2.2, March 2004
   http://tdc.web.cern.ch/tdc/hptdc/docs/hptdc_manual_ver2.2.pdf

2. Caen V1290 User Manual
   http://www.caen.it/servlet/checkCaenManualFile?Id=8653