**Vme LED Driver (VLD) production test**

William Gu

Feb. 7, 2022

1. **Introduction**

The VLD board, designed for HallC NPS experiment, is a VME64 6Ux160mm single width board. Figure 1 shows the VLD PCB, and its major components.



Figure The Vme LED Driver board, and its major components

The VLD production tests cover all the functions and the IO connectors. The software is in trigger.c, with function names: VLDtest1, VLDtest2, VLDtest3, VLDtest4, VLDtest5, VLDtest6, VLDtest7, and VLDtest8.

1. **Test setup**

The T-frame crate with DAVW5 VME-CPU (VxWorks), a multimeter, an oscilloscope, a TI board, and the two LED cables are needed for the test. Figure 2 shows the test setup.



Figure The VLD test setup, T-frame crate, VME\_CPU, Multimeter, Oscilloscpe, and the LED cable

1. **Test processes**
   1. Pre/power-up test: (VLDtest1)

Visually check the PCB;

Measure the resistances between all the power rails and the ground, no SHORT;

Mount the VLD front panel;

Set the switch#SEN to the left to enable flash memory#1;

set the Geographic address by switch SGA (located at the very top of the PCB), if the VME crate is NOT vme64X compatible (the geographic address is used for firmware loading);

set the VME address space VME\_ADD(23:19) by switch S2 (located between the FPGA and P0/P2), if the VME crate is NOT vme64X compatible (the Add(23:19) should be set the same as the Geographic Address for VME access).

Plug in and power up the VME crate;

Check the VME crate current draw;

Check the Voltages of all the power rails; All the 'Power Good' LEDs should be OFF, the FPGA\_done should be ON;

* 1. FPGA firmware loading (VLDtest2)

T-frame crate setup: (software): Make sure that the vld.svf is symbolically linked to a valid VLD firmware file (NPSVLD21.svf for example). Telnet to DAVW5.

DAVW5> ld < usrTempeDma\_AM.o

DAVW5> ld < trigger.o

DAVW5> VLDtest2(VLD\_slot)

This will load vld.svf (symbolic link to NPSVLD21.svf ). The process takes about 15 minutes. This load the SPI flash memory via FPGA JTAG port (indirect PROM loading) using the VME emergency loading (discrete VME to JTAG engine). During the flash memory loading, the FPGA DONE led will go off (the FPGA is programmed with a xilinx bridge firmware), and come back ON at the end of the flash memory loading.

After the firmware is loaded, press the PROGRAM push button switch to load the FPGA with the flash memory firmware.

If the DONE led goes OFF, the FPGA is programmed. The top LED (in the QUAD-LED region, to the front panel) should be ON to indicate the VLD FPGA is ready.

* 1. VLD VME register test: (VLDtest3)

DAVW5> VLDtest3(VLD\_slot)

This will fully test the VME64 data bus and address bus. The test will perform VLD vme register read and write with 32-bit data trying to uncover bit stuck, neighboring bits shorts etc. If the terminal does not print mismatch (between write and read), the register test has passed.

* 1. Bleaching regulator test (VLDtest4)

DAVW5> VLDtest4(VLD\_slot)

This test will set all the five bleaching regulators with all the possible amplitude settings (0-7 for amplitude, and 0x8 for enable). A multimeter is used to measure the bleaching amplitude (and the bleaching current, via a 30 Ohm serial resistor). Visually, the LED brightness changes as the setting changes. When the amplitude is set to 0 to 7, all the LEDs should be OFF (bleaching is not enabled). When the amplitude is set to 8 to 15, all the LEDs should be ON, and the LED brightness decreases (setting 8 is the brightest, and setting 15 is the dimmest), and the BLEACHING LEMO output should be ON (-0.8V at 50 Ohm termination). The following table is an example of the bleaching regulator measurement:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Regulator  setting | Bottom\_OnBoard | | | | TOP\_OB | | TOP\_FP | MID\_FP | BOT\_FP |
| V\_RD | V\_DR | V\_RC | I(mA) | V | V\_load | V | V | V |
| 0-7 |  |  |  |  |  |  |  | 146 |  |
| 8 | 4673 | 4437 | 3266 | 39 | 4819 | 4663 | 4845 | 4831 | 4842 |
| 9 | 4601 | 4368 | 3243 | 37 | 4606 | 4593 | 4640 | 4621 | 4633 |
| 10 | 4396 | 4165 | 3173 | 33 | 4389 | 4384 | 4423 | 4404 | 4416 |
| 11 | 4179 | 3952 | 3102 | 28 | 4173 | 4166 | 4207 | 4188 | 4198 |
| 12 | 3964 | 3742 | 3027 | 24 | 3957 | 3950 | 3991 | 3972 | 3981 |
| 13 | 3748 | 3531 | 2949 | 19 | 3740 | 3733 | 3775 | 3755 | 3764 |
| 14 | 3533 | 3323 | 2869 | 15 | 3523 | 3516 | 3598 | 3539 | 3546 |
| 15 | 3317 | 3116 | 2789 | 11 | 3306 | 3299 | 3341 | 3322 | 3328 |

The units are in mV. V\_RD is the regulator output, which is measured at the anode of the Diode (between the regulator and the diode). V\_DR is the voltage at the cathode of the diode (between the diode and the current limiting resistor). V\_RC is the voltage at the front panel connector (between the current limiting resistor and the connector). The bleaching current is voltage drop over the current limiting resistor divided by its resistance (30 Ω ±1%), that is, .

* 1. Calibration DAC and buffer tests (VLDtest5)

DAVW5> VLDtest5(VLD\_slot)

This test will load the DAC values 00...00\_0123\_2345\_4567...ffffffff…7654\_5432\_3210\_00…00 to the memory and generate 2ns wide pulse for every value. To check the pulse on the Channel #1 of any connector using the oscilloscope. The pulse should look something like the figure 3.

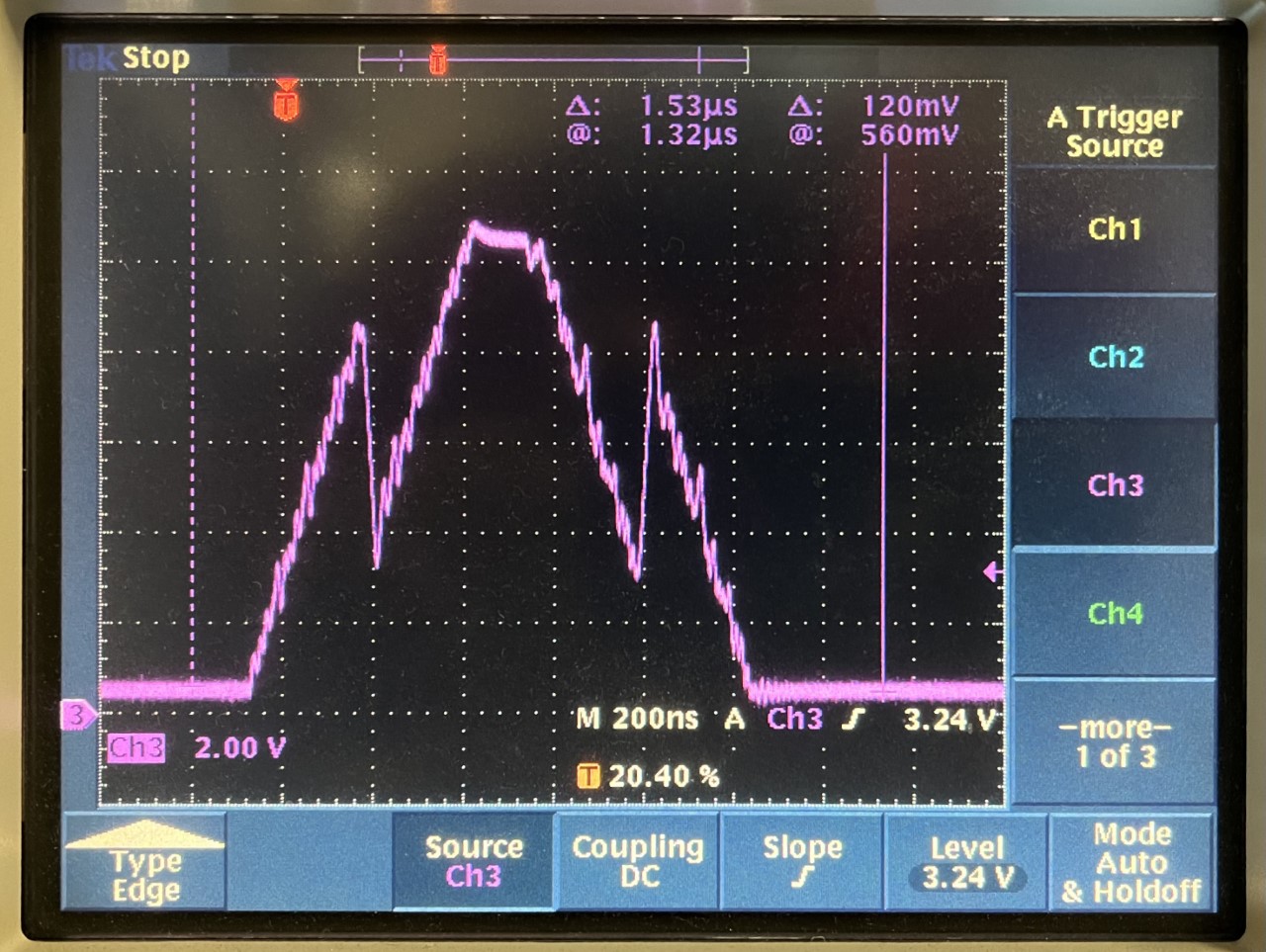


Figure A typical Calibration pulse

3.6 Individual channel test (VLDtest6)

DAVW5> VLDtest6(VLD\_slot)

This test will loop over the five connectors, from Top\_FrontPanel, Middle\_FP, Bottom\_FP, Top\_OnBoard, to Bottom\_OB.

For each connector, the program will loop over all the 36 channels with the calibration pulse. After the 36 channels calibration, the bleach mode is turned on, with amplitude looping over 0111 to 1000, to 1001, …, to 1111, and disabling the bleach mode at the end. So, the LED will be lit up from 1, to 2, …, to 35, and to 36, then all the 36 LEDs are lit up, with brightness going dimmer simultaneously.

In addition to the cable LED ON/OFF visual check, the LEMO outputs should also be checked. The LEMO outputs are NIM level, Trigger\_Output, and Bleaching\_in\_progress. Here is a scope capture of the Trigger\_output

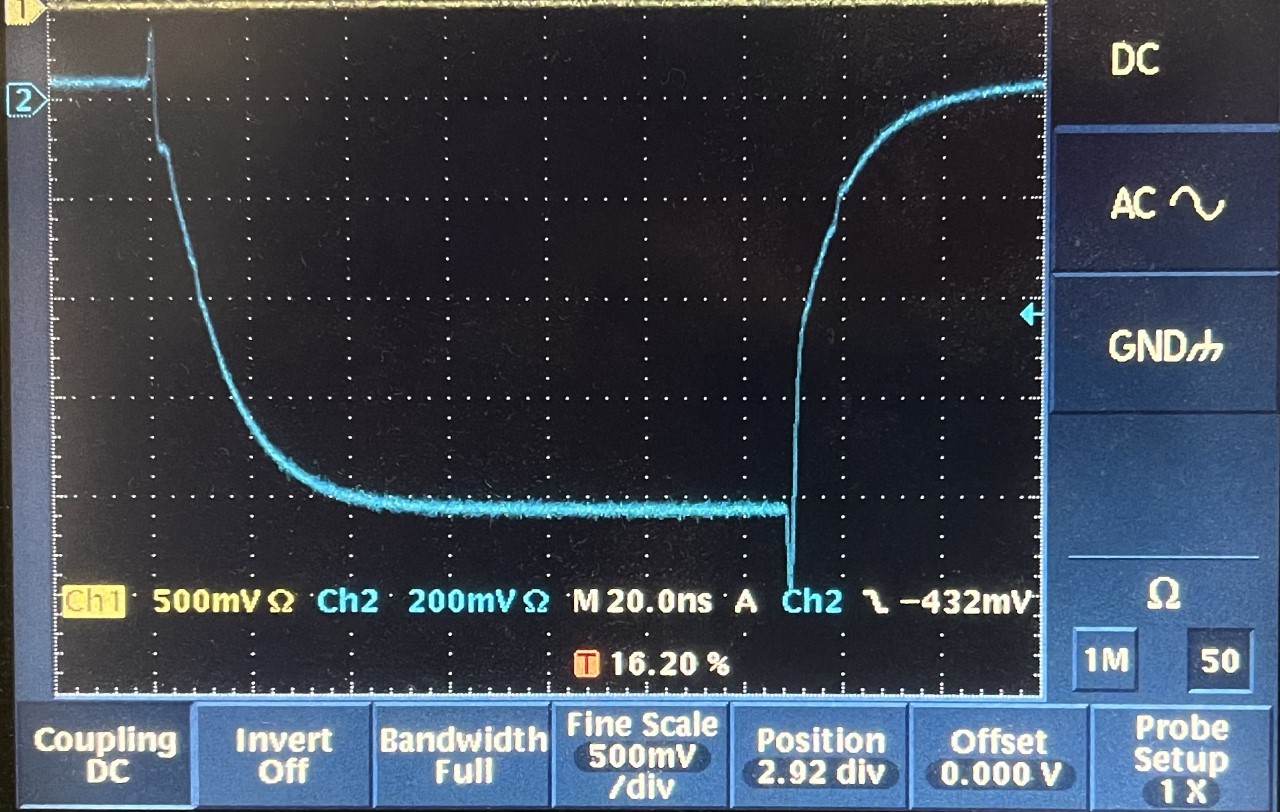


Figure The LEMO output of the TRIGGER signal

The rising and falling edges of the NIM output is very slow (~20ns). After replacing the RF04NL and RF14NL with 0.22uF capacitors, the edges of the NIM outputs are much better (~ 2ns) as shown in the next figure.



Figure 5 After replacing the RF04NL, RF14NL with 0.1uF cap, the edges are much better.

3.7 The front panel LEMO input test (VLDtest7)

Using a multimeter, check the SN65LVDS348 reference voltage, and fill this table

|  |  |  |  |
| --- | --- | --- | --- |
| SWIN position | Left (closer to the front panel) | Middle | Right (closer to the center of the PCB) |
| Vref (SN65LVDS348) | + 1.18 V (LVTTL) | - 0.36 V (NIM) | - 1.18 V (ECL) |

Test the front panel inputs:

DAVW5> VLDtest7(VLD\_slot)

This test will start with VLDtest5, then change the clock from VME clock (frequency \*5), to on-board oscillator, then to the front panel input.

If the front panel input comes from the TI (no 50 Ohm termination is allowed), which may be set to 42 MHz, the pulse will be six times wider, because the VLD clock is virtually six times slower.

After the clock test, it will change the trigger from internal random trigger generator to Front Panel trigger inputs. Following the screen display to determine if the test is successful.

add the heat sink to the FPGA

3.8 More calibration pulser test with long cables (VLDtest8)

DAVW5> VLDtest8(VLD\_slot)

This test will loop over dozens pulse size setting on a specific channel with a long cable to the LED. The pulse size, probed on the long cable, should become bigger. Figure 6 is the setup with a typical pulse capture on the scope.

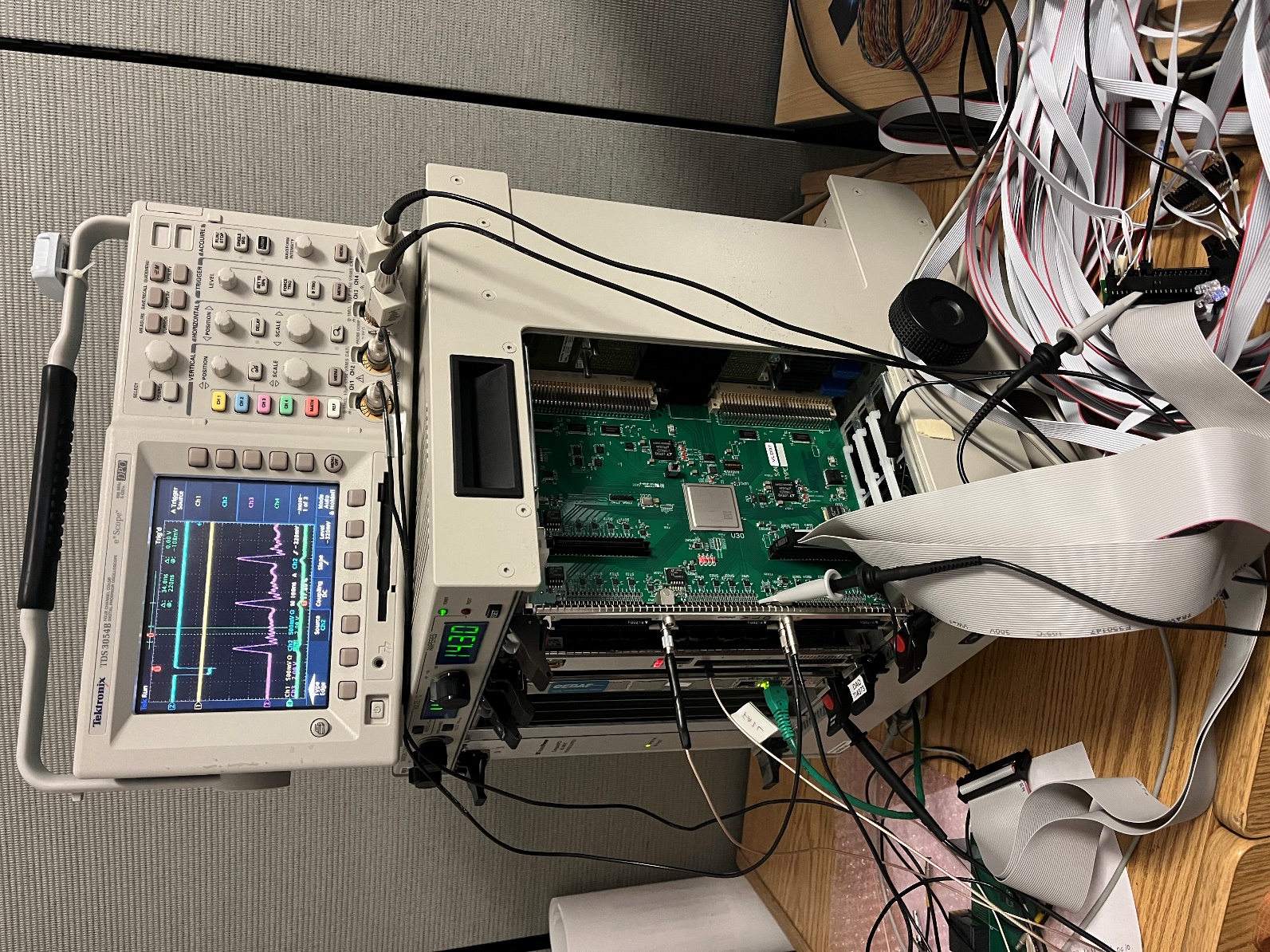


Figure 6 The pulse shape and the long cable test setup.

1. **End of test**

After the test, report the board test result. If the board passed all the tests 3.1 – 3.8, and no dead channel from test 3.6, the board have passed the production test. For the good board, add the heat sink for the FPGA, add the label on the front panel (HallC, VLD#nn, where the nn will match with the on-board sticker (01 – 12), Advanced Assembly production serial number).

1. **VLD production test summary**

Twelve VLDrev2 boards are make (#1 as the first article, #2-#12 as the second article). They are the same. There are two modifications from the schematics designs:

1. The RF04NL and RF14NL were changed from 14K resistors to 0.22 uF capacitors. This has improved the NIM output (LEMO) rising edge and falling edge dramatically (from ~20ns to ~2ns).
2. The RFP09 and RFP10 value was changed from 100 Ohm to 50 Ohm. From the assembly house, these two resistors were set to DoNotInstall, so that I can test the ECL input (from the TI output). After the test, two 50 Ohm resistors were loaded to test the NIM level input.

The Assembly house (Advance Assembly) did a good job. There is no major problem in the PCB nor the assembly. Two cold solder joints were found on (VLD#8 and VLD#11) the bleaching zero ohm resistors.

Further comments:

1. The front panel is very tight (to fit the three P50E-080 high density connectors and the two dual LEMO connectors, which leaves no extra space on the VME 6U front panel). This means no tolerance in front panel design.
2. The VLDs are configured to use the Front Panel cables only. If the on-board cable (another 72 channels) connectors are used, the bleaching fuse needs be changed from 5A to 10A rated, as the total bleaching current could be about 7A per board at the highest designed bleaching current.

Refer to LEDCalibPulse.ppt file for the detailed pulse shape and test results.