Nuclear Physics Division

Description and Technical Information for the VXS-based Electron Trigger and Readout Card (VETROC)

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1 Introduction

The VETROC (VXS-based Electron Trigger and ReadOut Card) is being designed for HallA Compton Polarimeter (Robert Michaels, Alexandre Camsonne, and Sirish Nanda: VETROC for Hall A Compton). The electron detector is a 4-plane silicon microstrip detector with 192 (8x24) strips per plane.

This board is further expanded so that it can be used as an generic IO board. Sixty-four channels any-level (TI term, differential signal in with a common mode of -4 to +5V) inputs are built on the board. Up to 64-channels can be added via two mezzanine boards through the front panel. Up to 80 channels can be added the VME P2 backplane IO card. Depending on the mezzanine and IO cards design, the 144 channels can be inputs or outputs or combination of the inputs and outputs. The mezzanine design is compatible with the CAEN1495 mezzanine, so the CAEN1495 mezzanine boards can be used on the VETROC board.

With its powerful FPGA (XC7A200T) on board, the board can do a lot of signal processing. In the foreseeable future, this board can be used as a multichannel TDC board with a resolution of ~10s ps. With the high speed serial connections, (both the backplane and the front panel), it is not hard to program it into a generic DAQ board. is a replacement for the original ETROC board.

This board has the optional TI (Trigger Interface) interface (depending on the firmware implementation and front panel space allocation). It can be used to drive a TI board or receive from a TI board.

2 PCB design of the VETROC module

VETROC is designed as a VXS payload board. It also works in a standard 6U VME64 crate. It is used for the trigger and readout. Figure 1 is the VETROC diagram.

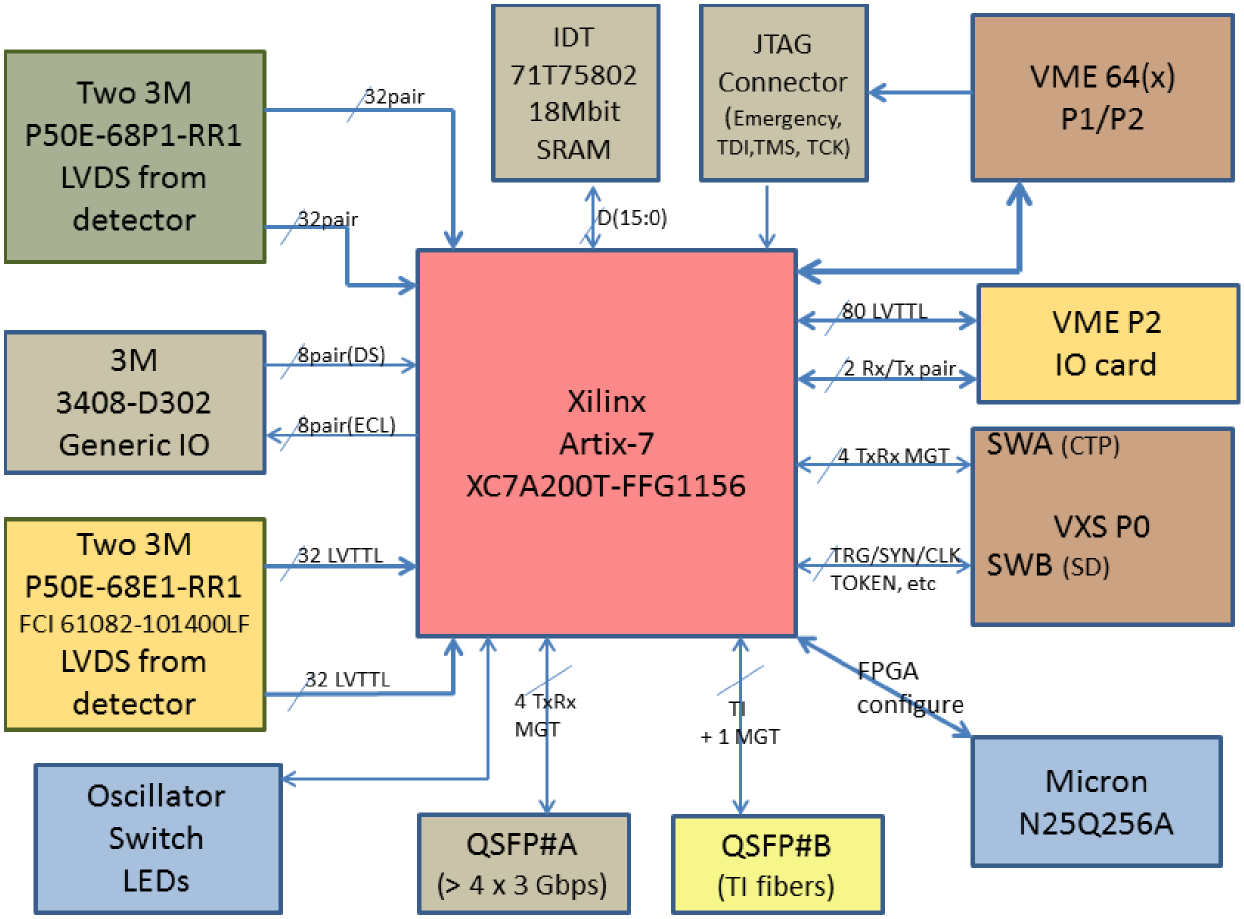

Figure 1: VETROC fuctional diagram

Figure 2 is the routed VETROC board with the front panel drawing:

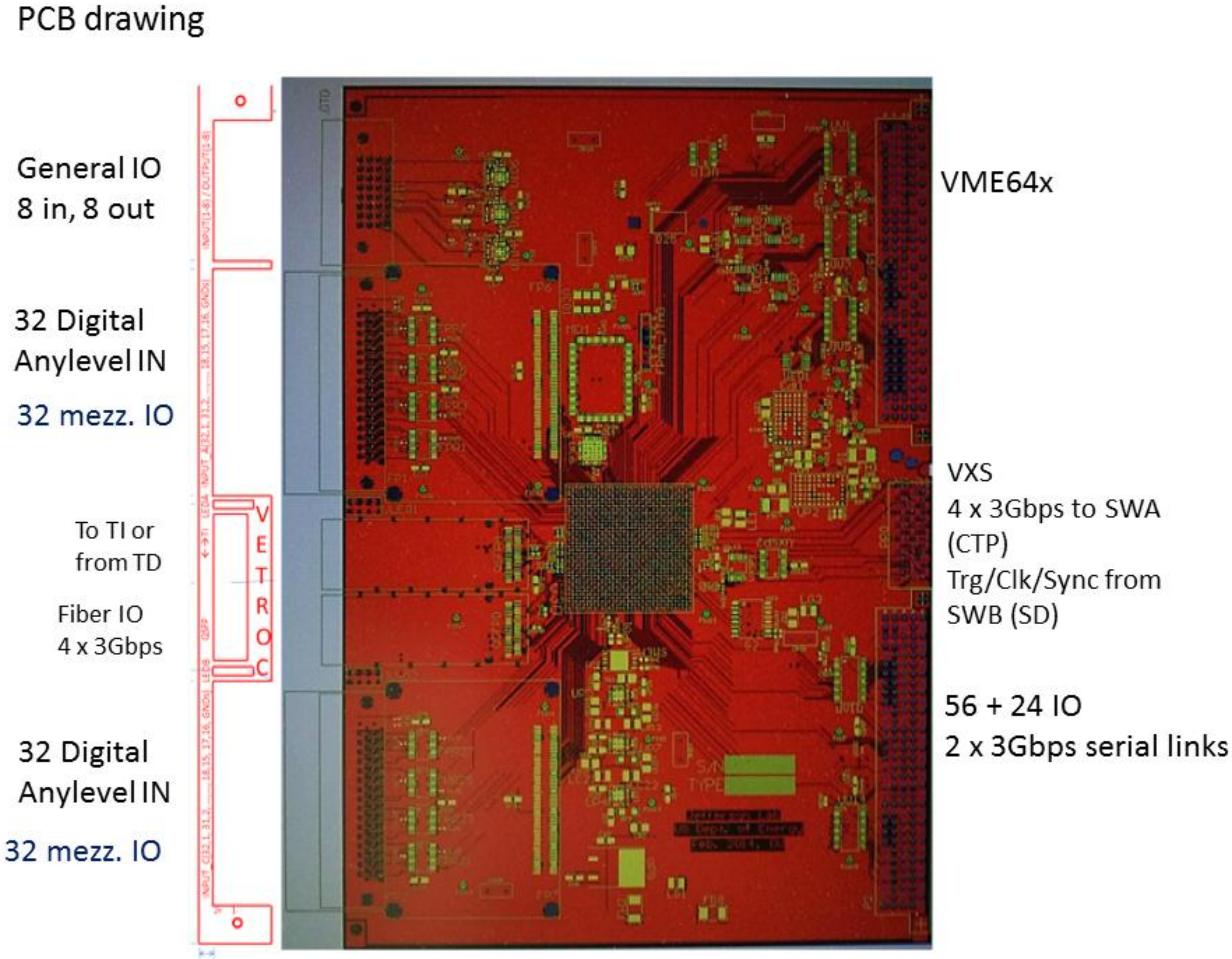

Figure 2: VETROC and its front panel drawings

The Xilinx Artix-7 XC7A200T-FFG1156 FPGA is chosen for signal processing. It is less expensive, and it has enough IO and resources for signal processing. The Micron N25Q256 serial flash is used to save the FPGA configure data. This memory supports 4-bit wide FPGA load.

Two sets of 32-pair differential signals are received using two 3M Pak 50 Boardmount Plug connectors (P50E-68P1-RR1-EA). The signals are converted to LVTTL on the PCB by TI SN65LVDT352, which translates any differential signals (LVDS, LVPECL, ECL) to LVTTL. Because of the LVTTL translation, it is better to keep the signal at 100 MHz or lower. (An upper limit can be obtained by the PCB test).

Two mezzanine boards (with up to 32 channels each) can be plugged to further increase the IO capability of the front panel. The mezzanine board uses FCI61082-101400LF connector, which is fully compatible with the CAEN 1495 mezzanine card. This saves time to develop our own mezzanine card to expand the IO.

To further expand the IO capability, a VME P2 backplane IO card can be developed. This IO card can have up to 80 channels, and two pairs of high speed serial links.

Two sets of four LEDs are used to indicate the board status, which is directly from the FPGA. One set of the LEDs could be 'board ready', 'VME DTACK', 'Trigger' and 'Board error/Reset'.

One 3M 3408-D302 connector and two QSFP connectors are also loaded on the front panel. The 3M 3408-D302 connector has 8 generic differential signal inputs, and 8 ECL output, which are connected to the FPGA through TI SN65LVDT352 receiver and On-Semi MC100EP91 driver respectively. The first QSFP connector has 4 MGT (Multi-Gigabit Transceivers) connected to the FPGA directly, which can support more than 3 Gbps each. The other QSFP is compatible with Trigger Interface (TI). Depending on the application, this QSFP can accept the TI input from a TD/TImaster, or drive a TI for a small self-contained test setup.

An external memory, IDT71T75802 (18 Mbit) is added to expand the FPGA memory capacity.

The VME64x is implemented, which uses the Geographic address and +3.3V supply. The board is compatible with standard VME64 backplane. If the board is plugged in the VME64 crate, the onboard DC-DC converter can be used to get the +3.3V power from the +5 supply. Five bits of the on-board switch are used to set the A24 (A23-A19) address space.

The VXS P0 connector are used to send the channel ‘HIT’ information to Crate Trigger Processor (CTP in Swich slot#A), and get the readout information from the Signal Distribution board (SD in Switch slot#B).

3 Functional Descriptions

3.1 FPGA programming

The FPGA XC7A200T needs about 80Mbit to configure. This configure data is saved in the Micron N25Q256, which is 256 Mbit. The memory can save two versions of the FPGA configure file. This can supply a fall back design, which is especially useful when the board is used in an area that is difficult to access (need be tested).

The FPGA is programmed in Master SPI mode with external clock of 33MHz and 4-bit wide data loading. The expected FPGA program time is less than one second. The Micron memory can be loaded by the iMPACT software through the on-board JTAG connector. The iMPACT software will load a special firmware to the FPGA through the JTAG connector and program the memory through the special firmware.

A VME Memory loading interface can be implemented in the FPGA firmware. If so, the Memory (and the FPGA) can be reloaded remotely if the FPGA is working.

To make it more robust for remote programming, a hardware (discrete logic) VME to JTAG engine is implemented on the board (copied from TS/TI/TD design) using the custom defined address modifier code (AM = 19), which will not get confused with the standard (VME specified) A24 address modifier codes. This engine can load the FPGA firmware even if the memory is corrupted (or simply, the memory is empty) and the FPGA failed to be loaded by the memory. The engine has been tested on TI to load the Xilinx PROM successfully. It should be able to load the FPGA. In the JTAG engine, the VME data bit[1] is used for TDI, bit[0] is used for TMS, and all the other bits are unused. The higher bit of A24 address should match with the geographic address, and the lower A24 address is set to be 0x0FFFC.

3.2: Clock Distribution

There are three main clock sources for the PCB. As a VXS payload board, it gets the clock (250 MHz) via VXS P0 backplane from SD/TI board. For the test or application without the VXS crate, an on-board oscillator (250MHz) is implemented. The third source is the optional front panel TI fiber. Only one clock source is selected as the FPGA clock, which pipelines the trigger and readout logic. The clock source is selected by FPGA and buffered by the cross-point switch Micrel SY58040. The SY58040 will send three clocks to the FPGA, one for the FPGA internal logic, one for the north MGT blocks, and the other for the south MGT blocks; one clock to the front panel QSFP when the TI interface is used.

3.3 Trigger logic

Up to 208 channel (64 built in on the board, 64 front panel mezzanine card, and 80 VME P2 IO card) detector signals can be received as LVTTL on the FPGA. TI SN65LVDT352 is the receiver, which accepts almost any differential signals (LVDS, LVPECL, ECL etc.). The 208 signals will be processed in the FPGA.

The simplest processing will be to find the HIT signals on these channels and send the HIT information to CTP via VXS P0 connector.

If the inputs are aligned (detector positional alignment), the board can perform some track finding logic. In this case, the front panel connectors (64 built-in plus 64 mezzanine) can be used to connect to the detector, and the VME P2 IO card can be used to connect to the other VETROC boards for 'right' and 'left' of the detector for track overlap. If the number of overlapping channels is large, the QSFP option can be used, which can pack in more channels. The track segment can be sent to the CTP or even the SSP directly.

3.4 VME interface

The VETROC board is a VXS payload slot board. It is compatible with VME64x backplane. Normally, it is a VME slave board, with interrupt capability.

The VETROC can also be a master VME board. It supports single level bus request (BR3, level 3) only, as we do not expect many boards to be a VME master in the crate. The VME master capability has not been tested yet.

For simplicity, three kinds of VME address modifier codes are implemented. (1), User defined address modifier. (0x19,0x1A, 0x1C and 0x1D) This is similar to the A24 address modifier. It is used to load the FPGA by the onboard discrete logic (also called emergency JTAG engine). (2), Standard A24 address modifier. This is used to readout the registers on the FPGA, slow controls of the board. (3), A32 data transfer. This is used to transfer data to the ROC (Read Out Controller). This is implemented the same way as other ADC/TDC board, so the ROC needs only one read to get all the front end boards' data out for higher efficiency.

3.5: Readout logic

The readout is initiated by the readout trigger from TI via SD and VXS P0 backplane. The channel HIT information (which channel, what time) can be readout via VME A32. The readout logic can be borrowed from other projects. The readout trigger can be used as time_0 for the channel hit information if the resolution requirement is less than 4ns.

4. Specification Sheet

4.1 Mechanical

- Single width VITA 41 Payload Module. It will be positioned in PP1-PP16 in VXS crate; it can also be plugged into any slots in standard VME crates without VXS.

4.2 High speed serial P0 inputs and outputs:

- Switch slot#A (CTP) four lane MGT connections
- Switch slot#B (SD) compatible connections.

4.3 Front panel inputs and outputs:

- 2 x 32 LVDS detector inputs;
- 8 generic differential signal inputs;
- 8 generic ECL outputs.
- 4 channels of MGT on one QSFP, TI or TImaster fiber IO on the other QSFP.
- 2 optional mezzanine board with up to 32 channels each.

4.4 LED Indicators: Front Panel (FPGA controlled):

- Set #1:
  - Bit 1 (close to the PCB): FPGA programmed and the clock (DCM locked) is ready;
  - Bit 2: VME DTACK, VME activity;
  - Bit 3: Readout trigger is detected;
  - Bit 4: MGT Rx error;
- Set #2:
  - Bit 1 On board IO activity;
  - Bit 2: Mezzanine board activity (on: mezzanine card plugged, flash: activity);
  - Bit3: VME P2 IO card activity (on: mezzanine card plugged, flash: activity);
  - Bit 4: TI interface activity.

On board:

- Power OK near each regulator and DC-DC converter (The LED is OFF when the power is OK);
- FPGA program DONE (The LED is OFF when programmed);

4.5 Programming:

- VME to JTAG A24D32 with user defined AM (Address Modifier) for remote FPGA firmware loading.
- onboard JTAG connector to FPGA;
- Custom VME to Micron memory engine will be implemented in the FPGA using A24D32 for memory loading (FPGA firmware);
- Up to two revisions of the FPGA firmware can be stored in the memory simultaneously.

4.8 Power requirements:

- +5v @ 1 Amps; -12V @ 0.25 Amp; +3.3V @ 2 Amps
- With Optional DC-DC converters for +3.3V, +5V @ 3A, +3.3V is not required from backplane.
- Local regulators for other required voltages: +1.0V, +1.2V, +1.8V, +2.5V, and -5V.

4.9 Environment:

- Forced air cooling;
- Commercial grade components (0-75 Celsius or better)

5 VETROC operation procedures:

The VETROC needs to be properly set, and plugged into the proper crate and slot. Damage may happen to the VETROC, the crate, or other PCBs in the crate if the right procedure is not followed.

5.1 VETROC Power supply:

The VETROC can use +3.3V directly from VME64x crate. It can also generate its own +3.3V supply by a DC-DC converter. Proper settings are needed to avoid damage to the board or backplane.

If the VME64x crate +3.3V power is used for the VETROC:
(1). The fuse, FG1 is stuffed;
(2). The DC-DC converter UP2 is removed.

If the VME64x crate +3.3V power is not used, or +3.3V is not available from the backplane:
(1). The fuse, FG1 is removed;
(2). The UP2 is stuffed.

The default setting for the VETROC is assuming that there is no +3.3V from the backplane.

5.2 FPGA program mode setting:

The FPGA program can be set to MasterSPI mode or JTAG mode. For MasterSPI mode:

(1). Remove RBJ3;
(2). Load RBJ4.

For JTAG mode:

(1). Remove RBJ4;
(2). Load RBJ3.

5.3 Local trigger and SD link:

The VETROC can send the local trigger information (for example: a track segment) to the SD. The source could be a standard FPGA IO pad, or a MGT high speed differential PAD. (VXS P0 pin#D15/E15)

For LVDS driver (driven by a DS90LV031A):

(1). Remove CGT1 and CGT2;
(2). Load RS01 and RS02.

For MGT high speed driver:

(1). Remove RS01 and RS02;
(2). Load CGT1 and CGT2.

The VETROC can also receive from SD. The receiver could be a standard LVDS IO, or a MGT high speed differential PAD. (VXS P0 pin#A15/B15)

For LVDS signal receiver:

(1). Remove RS07 and RS08;
(2). Load RS03 and RS04.

For MGT high speed receiver: (it is a receiver, not driver)

(1). Remove RS03 and RS04;
(2). Load RS07 and RS08.

5.4 VETROC 8-bit switch S2 setting:

Bit[8:4]: set the VME A24 address space A[23:19] when the VETROC is in non-VME64x crate. If it is in VME64x crate, the geographic address is used, the switch is not used.

5.5 VME to JTAG discrete logic:

For standard A24 address modifier (0x39 etc.), load RB41 and remove RB42; For user defined address modifier (0x19 etc.), load RB42 and remove RB41.

6. VME Programming Requirements (This part will be updated as the firmware develops)

The VETROC supports three categories of Address Modifier codes: the user-defined codes (A24) for emergency firmware loading; Standard A24 for FPGA register read/write and slow control; A32 block transfer for VME data readout.

6.1 VME to JTAG emergency loading:

The AM[5:0] user defined codes are used for this logic. This works even before the FPGA is programmed and working. It is almost the same as A24D32 mode. The valid AM codes are: 0x19, 0x1A, 0x1D and 0x1E. These AM codes are user defined, and similar to the AM codes 0x39, 0x3A, 0x3D and 0x3E.

The valid address bits are A[31:24] do not care; A[23:19]=GA[4:0] for VME64x crates, or A[23:19]=0 for non-VME64x crates; A[18:2]=b'00011111111111111.

VME Data bit[1] is TDI; VME data bit[0] is TMS.

For example, if the board is in slot#5 (that is ~GA(4:0)= 11010), you need write to A(23:0)=0x28fffc. If data(1:0)=00, both TMS and TDI will be low; if data(1:0)=01, TMS is high, TDI is low; if data(1:0)=10, TMS is low, TDI is high; if data(1:0)=11, both TDI and TMS are high. The normal A24 address should try to avoid this address (0x0fffc).

A more advanced example: Instruction register shift (8-bit, shift in 0x5a) starting from/end up at the 'reset idle' mode: 14 consecutive writes to the address 0x28fffc with AM=0x19, 1a, 1d or 1e, the data are 1, 1, 0, 0, 0, 2, 0, 2, 2, 0, 2, 1, 1, 0 respectively.

Data	1	1	0	0	0	2	0	2	2	0	2	1	1	0
TMS	H	H	L	L	L	L	L	L	L	L	L	H	H	L
TDI	0x	0x	0x	0x	0	1	0	1	1	0	1	0	0x	0x

- "TMS H" means logic High, "TMS L" means logic Low, "TDI 0" means 0 or Low, "TDI 1" means 1 or High, and "TDI 0x" means DO NOT CARE by the JTAG, but the set value is 0.

6.2 Configuration Registers:

A24D32 are used for register read/write. Similar to the emergency loading logic, the base address is determined by the Geographic Address in VME64x crate, and external switch for non-VME64x crate. That is, A[23:19]=GA[4:0], or SW[8:4].

- Address offset: 0x00000: Board ID:

Bit 7-0 (R/W): Crate ID; Reset default 0x00;

Bit 12-8 (R): A24 address, higher 5 bits; Reset default 000

Bit 23-16 (R): PCB related setting, 0x01: production board, 0x00; prototype board;

Bit 31-24 (R): Board type: 0x71: TI, 0x75: TS, 0x7D: TD, 0x??: VETROC.

6.3 VME data acquisition:

For data acquisition, the A32 block reads are used. The base address is set by the upper 9 bits of A24 register 0x00010, that is A[31:23] = RegData[31:23] of A24=0x00010.

7 Pin out tables:

7.1 VXS P0 Pinout Table

Payload slot#18, TI or TImaster			
Pin name	Signal Description	Signal Level	Direction
DP1 (A1+, B1-)	CTPRX1		← SWA
DP2 (D1+, E1-)	CTPTX1		→ SWA
DP3 (B2+, C2-)	CTPRX2		← SWA
DP4 (E2+, F2-)	CTPTX2		→ SWA
DP5 (A3+, B3-)	CTPRX3		← SWA
DP6 (D3+, E3-)	CTPTX3		→ SWA
DP7 (B4+, C4-)	CTPRX4		← SWA
DP8 (E4+, F4-)	CTPTX4		→ SWA

SE1 (G1)	STAT_OUT	LVTTL (+3.3V)	→ SWA
SE2 (G3)	STAT_IN	LVTTL (+3.3V)	← SWA
DP23 (B12+, C12-)	Readout TRIGGER	LVPECL(DP)	← SWB
DP24 (E12+, F12-)	SYNC	LVPECL(DP)	← SWB
DP25 (A13+,B13-)	CLOCK	LVPECL(DP)	← SWB
DP26 (D13+, E13-)	Trigger2	LVPECL(DP)	← SWB
DP27 (B14+, C14-)	TOKEN_IN	LVPECL(DP)	← SWB
DP28 (E14+, F14-)	TOKEN_OUT	LVPECL(DP)	→ SWB
DP29 (A15+,B15-)	SD_Link	LVDS/MGT	← SWB
DP30 (D15+,E15-)	TrigOut	LVPECL/MGT	→ SWB
SE7 (G13)	Busy_Out	LVTTL	→ SWB
SE8 (G15)	Stat_IN	LVTTL	← SWB

Appendix D: Document revision history:

Jan. 13, 2014: Initial document;

Mar. 5th, 2014: updated as the board was redesigned to add more IO.