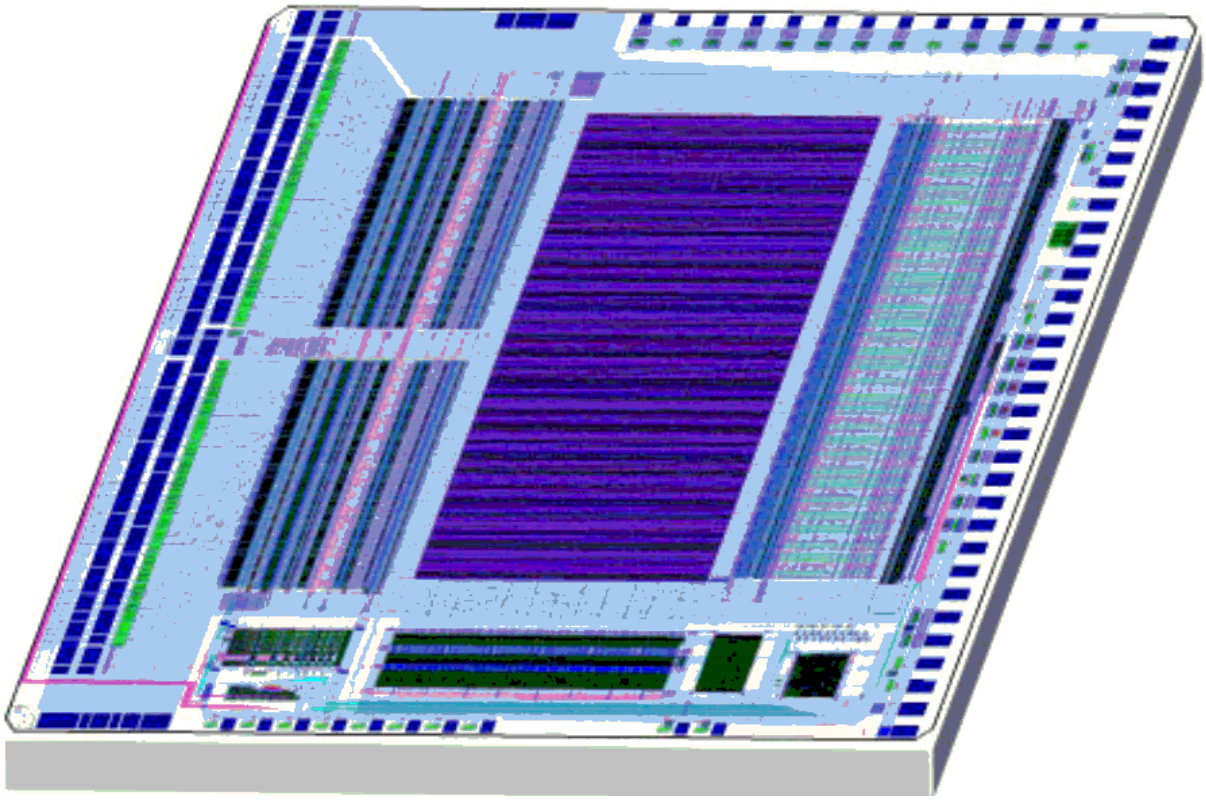
APV25-S1 User GuideVersion 2.2

Author: Lawrence Jones (RAL) l.l.jones@rl.ac.uk

Date: 5th Septemeber 2001



Revision History:

Version 1.0	14/4/2000	First web version
Version 2.0	7/2/2001	Revised pdf version including new bias settings
Version 2.1	10/7/2001	Revised pdf version including new bias settings suited for higher rate running, external and internal reference currents.
Version 2.2	5/9/2001	Further revision of bias settings

Table Of Contents

1. INTRODUCTION

The APV25-S1 is an analogue pipeline ASIC intended for read-out of silicon strip detectors in the CMS tracker. The architecture of the CMS tracker read-out system is based on analogue processing of data in the detector prior to transmission in analogue form to the DAQ.

The chip contains 128 channels of preamplifier and shaper driving a 192 column analogue memory into which samples are written at the LHC 40MHz frequency. Thus the memory always contains a record of the most recent beam crossings that the chip has sensed. A data access mechanism allows the marking and queueing of requested memory locations for output. Requested samples from the memory can then be processed with a FIR filter (APSP). This is a switched capacitor network which deconvolves the shaping function of the preamplifier and shaper stages to give a pulse shape confined to one 25ns period. After the APSP data is held in a further buffer until it can be read out through an analogue multiplexer.

The APV25-S1 also contains features required for eventual use in CMS including a programmable bias generator, an internal test pulse generation system, and a slow control communication interface.

2. PHYSICAL SIZE AND PAD LAYOUT

The size of the APV25-S1 chip (not including scribe channels) is 8055 X 7100 square microns. It is fabricated on a 0.25um (deep sub-micron), 3-layer metal process. The wafers are of 8 inch type. Two larger pictures of the APV25-S1 are available; a plain image and an annotated one, see web for details.

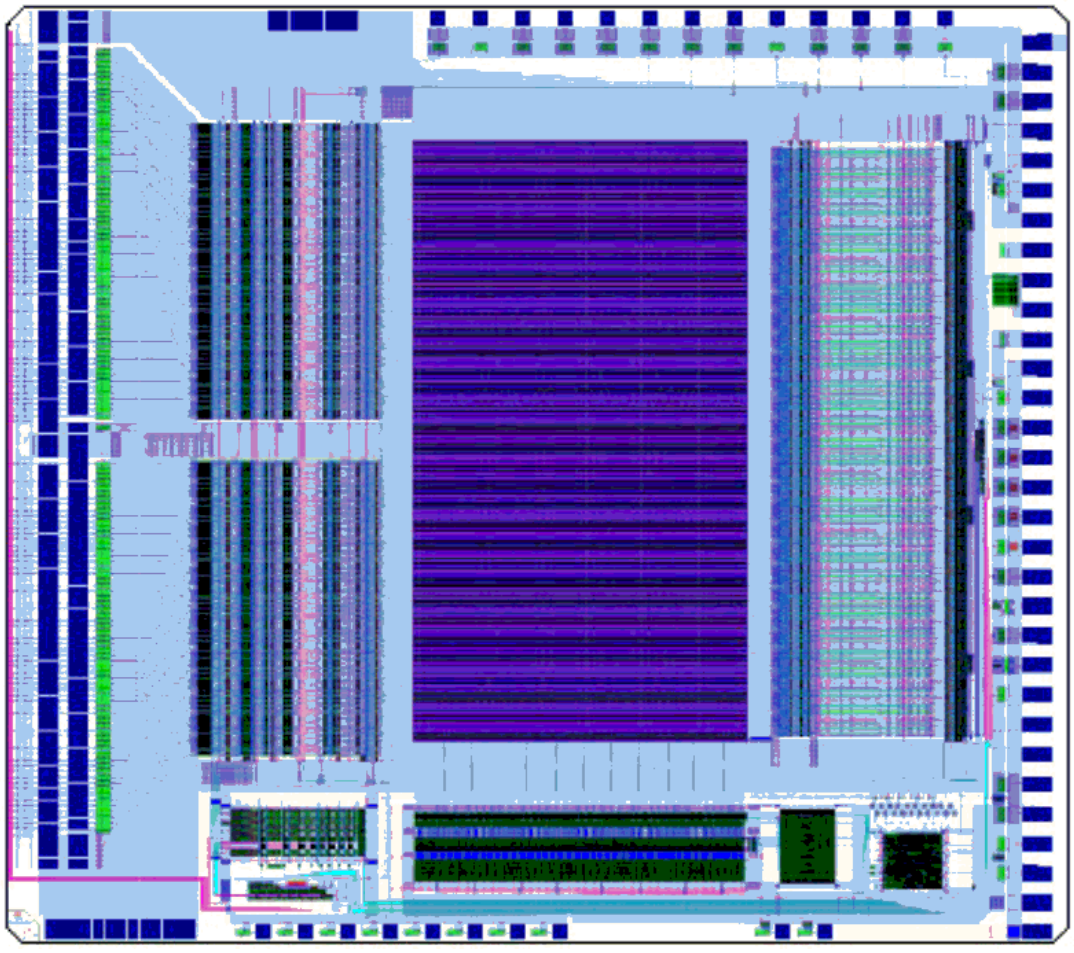


Figure 1: APV25 Layout

2.1 Pad Layout

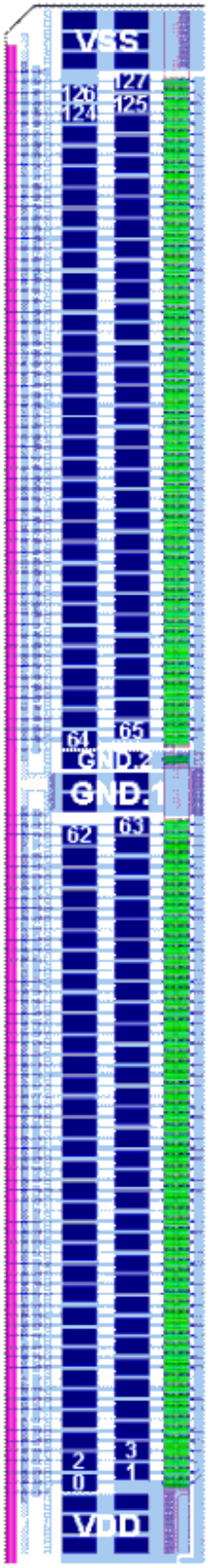


Figure 2: Front-end Pads

Front End Pad Layout

The 128 analogue inputs are grouped into 2 sections. The sections are arranged in two staggered rows with even numbered pads on the outside and odd numbered pads on the inside. The first section contains pads 0-63, and the second pads 64-127. The two groups are separated by a set of GND pads. These supply the preamplifier and shaper stages. GND.1 supplies the preamplifier input FET and GND.2 supplies the inverting stage of the preamplifier. The power pads contain passivation openings on the same pitch as the input pads. Analogue inputs have diode protection to VSS and VDD.

- Pad Size and Pitch
- Size 136 x 58um
- Pitch 44um

Back End Pad Layout

The remaining IO and power supply pads are located down the back edge of the chip. There are 31 of these and the full list is described in the next section.

- Pad Size and Pitch
- Size 95 x 95um
- Pitch 225um

The clock and trigger inputs are of LVDS type. The remaining digital inputs require switching between VDD and VSS. Input pads of type *Pull-up* default to VDD if left unconnected. Pads of type *Hysteresis* have a hysteresis characteristic because the expected signal edges on these may be slow.

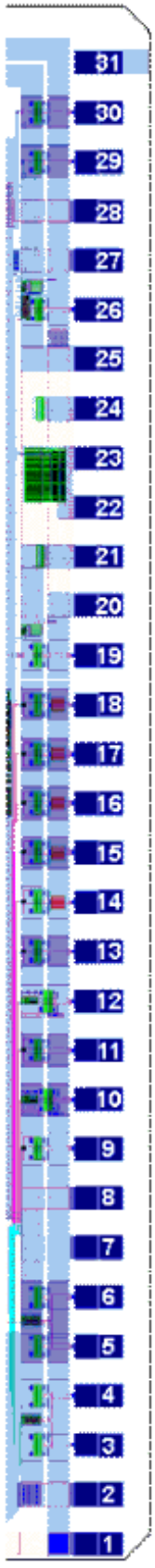


Figure 3: Back-end Pads

2.2 BACKEND PAD DEFINITION

The following table lists all the pads at the back of the chip. These are all the IO signals and power supplies required for the chip other than the front end where power is picked up on that side. For pad positions refer to figure 3.

Pad Position	Name	Type		Value	Function
1	VSS	Power	-	-1.25V	Negative Digital Supply
2	VDD	Power	-	+1.25V	Positive Digital Supply
3	TRIG-	Dig. Input	LVDS	-	Negative Trigger Input
4	TRIG+	Dig. Input	LVDS	-	Positive Trigger Input
5	CLK-	Dig. Input	LVDS	-	Negative Clock Input
6	CLK+	Dig. Input	LVDS	-	Positive Clock Input
7	VDD	Power	-	+1.25V	Multiplexer Positive Supply
8	VDD	Power	-	+1.25V	Positive Analogue Supply
9	RST	Dig. input	-	+/-1.25V	Reset Input (active low)
10	OUTE	Dig. Output	Open Drain	+/-1.25V	Analogue Data Active (active low)
11	SDAIN	Dig. Input	Hysteresis	+/-1.25V	I2C Data Input
12	SDOUT	Dig. Output	Open Drain	+/-1.25V	I2C Data Output
13	SCLK	Dig. Input	Hysteresis	+/-1.25V	I2C Clock
14	ADD0	Dig. Input	Pull-up	+/-1.25V	Chip address bit (active low)
15	ADD1	Dig. Input	Pull-up	+/-1.25V	Chip address bit (active low)
16	ADD2	Dig. Input	Pull-up	+/-1.25V	Chip address bit (active low)
17	ADD3	Dig. Input	Pull-up	+/-1.25V	Chip address bit (active low)
18	ADD4	Dig. Input	Pull-up	+/-1.25V	Chip address bit (active low)
19	MUXOUT	Ana. Output	-	-	Output of Multiplexer
20	VSS	Power	-	-1.25V	Output Buffer Negative Supply
21	VDD	Power	-	+1.25V	Output Buffer Positive Supply
22	OUT-	Ana. Output	-	-	Output Buffer Negative Output
23	OUT+	Ana. Output	-	-	Output Buffer Positive Output
24	VSS	Power	-	-1.25V	Output Buffer Negative Supply
25	VDD	Power	-	+1.25V	Output Buffer Positive Supply
26	IREF	Ana. Bias	-	+128uA	Analogue Reference Current
27	VSS	Power	-	-1.25V	Multiplexer Negative Supply
28	VSS	Power	-	-1.25V	Analogue Negative Supply
29	IREFBIAS	Ana. Bias	-	0V or +1.25V	Chip Bias Control (see section 6.0)
30	GND	Ground	-	0V	Analogue Bias
31	VSS	Bias	-	-1.25V	Chip Guard Ring Bias

Table 1: Definition of Back-End Pads

2.3 Power Supply Provision

Nominal values for VDD, GND and VSS are +1.25V, 0V and -1.25V as in table 1. As already noted the GND supply at the front edge of the chip is split into GND.1 and GND.2 which is done to interrupt a positive feedback path which can cause instability. If it is not possible to provide a low impedance path (< 10 mΩ) from the supply to a common GND bond area at the front edge of the chip it is better to split the bond area and provide the GND.2 supply via a 100Ω (approx.) resistor from VDD. This has been found to ensure stable behaviour for multi-chip hybrids.

3. TEST PAD DEFINITION

Along the top and bottom sides of the APV25-S1 there are additional pads that were included in case there were problems with the chip. They were intended to be available to use as either: probe points to measure interval voltages and currents in the chip, bias points (should the need arise to override the on chip bias system) or alternatively be used to introduce additional decoupling if required. In practise it should not be necessary to override the internal bias or apply addition decoupling so they can be left unconnected. However for completeness they are listed below:

3.1 Top Side Test Pads

There are thirteen diode protected analogue pads: They are labelled B to N in figure 4.

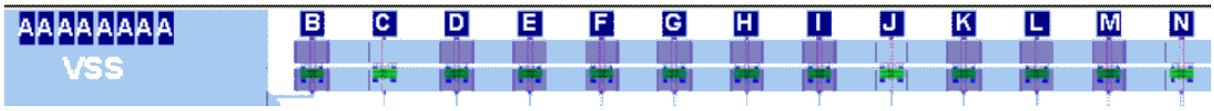


Figure 4: APV25-S1 Top Pads

The thirteen pads are listed in the table below. Pads IPRE, VFP, IPSF, ISHA, VFS, IPSP, VPSP and IMUXIN are all outputs from the APV25-S1 bias generator. Pads NP2, NS2 and NA2 are all internal bias nodes within the preamplifier, shaper and APSP respectively. Pad IREFIN connects to the output of the chip reference current pad. Pad IMUXOUT connects to the output from the multiplexer output bias circuit.

Pad Position	Name	Type	Function
A	VSS	Supply	Analogue Negative Supply (-1.25V)
B	IPRE	Analogue	Preamp Input FET Current Bias
C	NP2	Analogue	Internal Preamplifier Bias Node
D	VFP	Analogue	Preamp Feedback Voltage Bias
E	IPSF	Analogue	Preamp Source Follower Current Bias
F	ISHA	Analogue	Shaper Input FET Current Bias
G	VFS	Analogue	Shaper Feedback Voltage Bias
H	NS2	Analogue	Internal Shaper Bias Node
I	IPSP	Analogue	APSP Current Bias
J	NA2	Analogue	Internal APSP Bias Node
K	VPSP	Analogue	APSP Voltage Level Adjust
L	IMUXIN	Analogue	Multiplexer Input Current Bias
M	IREFIN	Analogue	Chip Reference Current
N	IMUXOUT	Analogue	Multiplexer Output Current Bias

Table 2: Definition of Top Test Pads

In addition there are 8 pads (all marked A) which connect to the negative analogue supply VSS.

3.2 Bottom Side Test Pads

Along the bottom side of the APV25-S1 there are ten diode protected pads. There are six analogue pads and four digital pads (DEL1, DEL2, WPTOK, TPTOK).

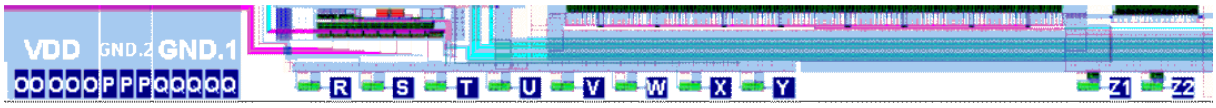


Figure 5: APV25S1 Bottom Test Pads

The pad CAL7 connects to the output from the edge generator of channel 7 of the calibration circuit. The two pads DEL1 and DEL2 connect to outputs from the variable delay line in the calibration circuit. DEL1 is the inversion of the delay selected from the variable delay line, and DEL2 is the output from the last stage of the variable delay line. CALBIAS is the voltage on the storage capacitor in the calibration circuit charge pump. ICAL is the current bias node to the calibration circuit.
In addition there are 5 pads (marked O) which connect to the positive analogue supply VDD, 3 pads (marked P) which supply GND to the front-end inverter stage, and 5 pads (marked Q) which supply GND to the Preamplifer input transistor.

Pad Position	Name	Type	Function
O	VDD	Supply	Analogue Negative Supply (-1.25V)
P	GND.2	Ground	Supply to front-end inverter stage (0V)
Q	GND.1	Ground	Supply to Preamplifier input transistor (0V)
R	ISSF	Analogue	Shaper Source Follower Current Bias
S	IPCASC	Analogue	Preamp Cascode Current Bias
T	ISPARE	Analogue	Spare current from Bias Generator
U	CAL7	Analogue	Output from channel 7 of calibration circuit
V	DEL1	Digital	Output from variable delay line
W	DEL2	Digital	Output from variable delay line
X	CALBIAS	Analogue	Voltage on calibration storage capacitor
Y	ICAL	Analogue	Current bias to calibration circuit
Z1	WPTOK	Digital	Output from Write Pointer (open-drain)
Z2	TPTOK	Digital	Output from Trigger Pointer (open-drain)

Table 3: APV25S1 Bottom Test Pads

4. LOGIC LEVELS

4.1 Digital Input

There are three type of logical inputs:

- Low voltage differential for fast signals (clock and trigger)
- CMOS type pull-ups for signals that require hard wiring
- Hysteresis pads for slow-edged signals (I2C and power-on-reset)

4.1.1 Low Voltage Differential Signal (LVDS)

These pads (*"CLK+* & *CLK-"*and *"TRIG+* & *TRIG-"*) are used on those inputs that are active during the sensitive acquisition time of the chip and are designed to minimise interference.

The CMS Inner Tracker LVDS specification states that the signals are modulated on the transmission media as a low amplitude differential signal (400mV). The transmission media should be twisted pair cable with 100 Ohms characteristic impedance. The line driver should be a constant current mode driver providing a 4mA output current to the transmission media. The cable should be terminated to 100 Ohms at the receiving end, where the terminating resistor converts the current into a voltage. The LVDS signal should have a typical offset voltage of 1.2V above VSS and the receiver should tolerate +/- 1V noise between the driver's VSS and the receiver's VSS.

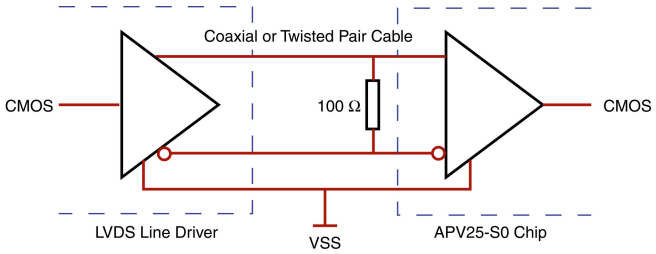


Figure 6: LVDS Point to Point Connection

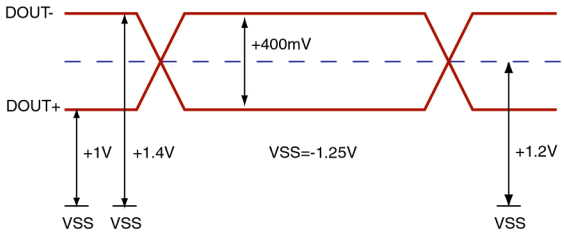


Figure 7: LVDS Signal Levels

4.1.2 Input with Pull-up

These pads are used for defining fixed chip configurations (e.g. defining a chip address). Internal 50kOhm resistors pull these inputs to VDD if they are left unconnected. This may be overridden by tying the pad to VSS. Note the chip address bits are inverted (i.e. VSS = logic 1).

4.1.3 Input with Hysteresis

These pads are used where control signals switch slowly (e.g. I2C lines). The pads are designed to have a hysteresis difference of at least -0.75V to +0.75V.

Input Transition	Switching Voltage
Low to High	+0.75V
High to Low	-0.75V

Table 4: Hysteresis Switching Levels

4.2 Digital Output

The digital outputs are open drain circuits. They require external pull-up resistors to operate.

4.3 Analogue Output

These pads (IOUT+, IOUT-) provide a differential current output for the analogue data from the APV25-S1 chip.

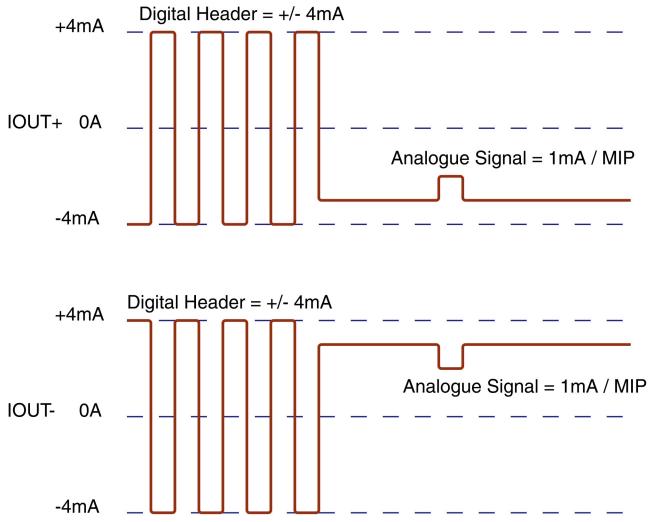


Figure 8: Analogue Output Levels

Data transmitted through *IOUT+ and IOUT-* are composed of two parts - a digital header followed by the analogue channel data. The digital header takes the values of +/- 4mA. The analogue dc level is programmable through I2C to be between the two digital levels, and the signal gain on top of this should be approximately 1mA / mip (also programmable to +/-30%).

Note: If the APVMUX chip (or another active receiver) is not being used to read out the APV25-S1 then both IOUT+ and IOUT- should be terminated to mid supply ((VDD+VSS)/2) with 50 Ohms.

5. CONTROL INTERFACE

The chip configuration, bias settings and error states are handled over a two wire serial interface designed to conform to the Philips I2C standard.

5.1 I2C standard

This is specified completely in the Philips data books and is not repeated here. The APV25-S1 may only act as a slave device and is addressed using the standard 7-bit mode where the most significant bits are "01". The remaining five bits are defined by bonding out the address pads of the chip. The address "11111" is reserved for global addressing where all connected APV25-S1s will respond. Consequently, a maximum of 31 chips can share the same controller and maintain unique addresses.

5.2 Communicating with the APV25-S1

The APV25-S1 has a command register which must be programmed before data may be transferred. This command determines which of the other chip registers is to be accessed and specifies the direction of data transfer. The least-significant bit of the command determines whether a *read* will occur (bit set to 1) or whether a *write* will occur (bit set to 0). A complete table of commands is listed in a following section.

5.2.1 Writing to the APV25-S1

Data is written to the APV25-S1 in an I2C transfer comprising three 8-bit data packets. These are:

- Chip address (read bit low)
- Command (read bit low)
- Value

5.2.2 Reading from the APV25-S1

To read from the APV25-S1 the command register must first be written to. Reading therefore requires two separate I2C transfers

Transfer1 - write to command register

- Chip address (read bit low)
- Command (read bit high)

Transfer2 - read data back

- Chip address (read bit high)
- 8-bit data

Subsequent reads of the same register are possible without reprogramming the command register.

If the chip is addressed globally then all APV25-S1s will respond, and since the output is of open-drain type, then the logical AND of all the addressed chips will be sensed. This is useful for addressing the error registers within all chips at the same time.

5.3 Command Register Codes

The command register codes are 8-bit with the last bit determining the direction of transfer. The codes are listed in the table below with most-significant-bit first. For read operations X=1, and for write operations X=0. There is one exceptions to this, the *Error* register is read only.

Register	Command Code	Function
IPRE	001 0000 X	Preamp Input FET Current Bias
IPCASC	001 0001 X	Preamp Cascode Current Bias
IPSF	001 0010 X	Preamp Source Follower Current Bias
ISHA	001 0011 X	Shaper Input FET Current Bias
ISSF	001 0100 X	Shaper Source Follower Current Bias
IPSP	001 0101 X	APSP Current Bias
IMUXIN	001 0110 X	Multiplexer Input Current Bias
ISPARE	001 0111 X	Not Used
ICAL	001 1000 X	Calibrate Edge Generator Current Bias
VFP	001 1001 X	Preamp Feedback Voltage Bias
VFS	001 1010 X	Shaper Feedback Voltage Bias
VPSP	001 1011 X	APSP Voltage Level Adjust
CDRV	001 1100 X	Calibrate Output Mask
CSEL	001 1101 X	Calibrate Delay Select
MODE	000 0001 X	Mode of Operation of Chip
LATENCY	000 0010 X	Delay Between Write and Trigger Pointers
MUXGAIN	000 0011 X	Sets Gain of Multiplexer
ERROR	000 0000 1	Holds Error Flags

Table 5: Definition of I2C Command Codes

5.4 Error Register Definition

Only two bits of the error *register* are used in the APV25-S1.

Bit number	Function	Value = 0	Value = 1
7	Not Used	-	-
6	Not Used	-	-
5	Not Used	-	-
4	Not Used	-	-
3	Not Used	-	-
2	Not Used	-	-
1	FIFO error	OK	Overflow
0	LATENCY error	OK	Error

Table 6: Definition of Error Register

5.4.1 FIFO error

A record is kept of the number of addresses stored in the FIFO. When this reaches 31 the next address written will cause a FIFO error. In *deconvolution* and *multi* mode, three addresses are stored for each trigger, therefore the limit is ten triggers. For *peak* mode, only one address is stored for each trigger, and therefore the limit is 31.

5.4.2 Latency error

The separation between trigger and write pointers should always be equal to the value programmed into the latency register. This is checked every time the pointers complete a full cycle of the pipeline (at least once every 192 clock cycles). If the latency between trigger and write pointers does not match the register then an error is flagged.

Either of these types of error will lead to pipeline failure. The error bits are active low so that it is possible to read a group of APV25-S1 at the same instant with a global read operation, the "wire-AND" of the open-drain outputs pulls the output low if any of the chips has an error. The only method of clearing the Error Register is to reset (hard or soft) the chip.

Note: When a new latency value is written, a latency error will be inevitably occur as the pipeline token separation will differ. The pipeline must be reset to reinitialise the pointers with the new separation. This must be done with a soft reset sequence (RESET101) which will also clear the error.

5.5 Mode Register Definition

Only six bits of the Mode register are used in the APV25-S1.

Bit number	Function	Value = 0	Value = 1
7	Not Used	-	-
6	Not Used	-	-
5	Preamp Polarity	Non-Inverting	Inverting
4	Read-out Frequency	20MHz	40MHz
3	Read-out Mode	Deconvolution	Peak
2	Calibration Inhibit	OFF	ON
1	Trigger Mode	3-sample	1-sample
0	Analogue Bias	OFF	ON

Table 7: Definition of Mode Register

5.5.1 Analogue Bias

The analogue bias control allows the bias to be disabled while the registers are programmed. Enabling analogue bias then lets the programmed values take effect. At power-up or hard reset it defaults to the off condition.

5.5.2 Trigger Mode

This determines the number of consecutive samples which are reserved in the pipeline each time the chip is triggered. In 1-sample mode only one sample is stored per trigger. In 3-sample mode three consecutive samples are stored.

5.5.3 Calibration Inhibit

The calibration logic contains a self-regulating "clocked" delay line which may cause noise in the system. For this reason it should be inhibited when not in use. At power-up it defaults to the inhibited condition.

5.5.4 Read-out Mode

This determines whether samples stored in the pipeline are read out and output individually (peak mode), or whether the APSP algorithm is used (deconvolution mode).

APV25-S1 Mode	Trigger Mode	Read-out Mode
Deconvolution	3-sample	Deconvolution
Peak	1-sample	Peak
Multi	3-sample	Peak

Table 8: Definition of Read-out Modes

Trigger Mode and Read-out Mode combine to give the three modes of operation of the APV-25S0

i) Deconvolution Mode

This is used in normal operation when data rates are sufficiently high such that the effects of pile-up are significant. It uses a three weight deconvolution-type algorithm.

ii) Peak Mode

This is used when pile-up is not significant and a larger signal to noise ratio is required. In this case the algorithm is not used, and single samples are triggered and read out directly.

iii) Multi-Mode

Due to the way the chip is triggered (see later section) it is not possible to trigger consecutive pipeline columns in *Peak* mode. To overcome this a new mode has been added called Multi-mode. In this mode three consecutive pipeline columns are reserved each time the chip is triggered, and these are then read out separately as with *Peak* mode. This can be useful when calibrating a pulse shape.

5.5.5 Read-out Frequency

The APSP FIR filter and the analogue multiplexer can operate at two read-out frequencies. The 20Mhz is the default mode of read-out and allows interleaving of data from two chips onto one 40Mhz bus. Interleaving is not possible using the 40Mhz mode.

5.5.6 Preamp Polarity

A unity gain inverter is included which can be switched onto the preamplifier output to invert the signal. This is included so that the shaper circuit always sees the same polarity of signal when silicon strip detectors of either polarity are used.

5.6 Latency Register Definition

This register contains an 8 bit binary number that defines the separation between the *Write* and *Trigger* pointers in the pipeline memory control. The register defaults at power-up to a value of 10000100 corresponding to 132 clock cycles. This value may be programmed to any value up to 191. However, values larger than 160 will reduce the pipeline efficiency especially at higher trigger rates). When the register is altered the pipeline must be reinitialised using RESET101.

5.7 MuxGain Register Definition

This register contains an 8 bit pattern which defines which size resistor to use in the input stage of the multiplexer. There are five possible values with the middle sized resistor giving a gain of 1 mA / mip. An adjustment of up +/- 20 % is possible by selection of the appropriate resistor. Selection is active high (i.e to select the mid-value resistor the register must be loaded with xxx00100).

5.8 Bias Generator Settings

The biases of the analogue stages of the APV25-S1 are controlled by an internal Bias Generator. There are three classes of bias: current, voltage and charge.

The Bias Generator initially produces a current in each case. Bias currents are then output directly, bias voltages are generated by internal resistors chosen to give appropriate levels of adjustment, and charges are generated by switching a current into a load resistor and converting the voltage step produced into a charge with a series capacitor.

The Bias Generator requires a reference current from which all of its levels are scaled. This can be generated from an internal or external source.

Name	Class	Range	Res.	Value	Description
IPRE	I	0 - 1020uA	4uA	n x 4uA	Preamplifier input fet bias current
IPCASC	I	0 - 255uA	1uA	n x 1uA	Preamplifier cascode current
IPSF	I	0 - 255uA	1uA	n x 1uA	Preamp source follower current
ISHA	I	0 - 255uA	1uA	n x 1uA	Shaper input fet bias current
ISSF	I	0 - 255uA	1uA	n x 1uA	Shaper source follower current
IPSP	I	0 - 255uA	1uA	n x 1uA	APSP current bias
IMUXIN	I	0 - 255uA	1uA	n x 1uA	Mux input current bias
ICAL	Q	0 - 255uA	625 elec.	n x 625 electrons	Calibrate edge generator current bias
VFP	V	-1.25 to + 0.65V	7.5mV	-1.25V + (7.5mV x n)	Preamplifier feedback voltage bias
VFS	V	-1.25 to + 0.65V	7.5mV	-1.25V + (7.5mV x n)	Shaper feedback volatage bias
VPSP	V	-0.65 to +1.25V	7.5mV	+1.25V - (7.5mV x n)	APSP voltage level adjust
CDRV	Dig.	Channel 0-7	-	-	Calibrate output mask
CSEL	Dig.	0 to 25ns	3.125ns	3.125ns / delay	Calibrate Delay Select

Table 9: Bias Generator Channel Definition

The nominal value of the *Bias Generator* reference current is 128uA. The resolution and ranges of each bias will scale accordingly if this is changed. The calibration charge injection levels also depend on the absolute values of on-chip capacitors and resistors.

5.9 Calibration Control Registers

The two registers CSEL and CDRV relate to the internal test pulse generator. They define the timing of the test pulses and the channels to which they are applied.

5.9.1 CDRV Register

The CDRV register controls the calibration sets masked when a calibration operation is performed. There are 8 calibrate sets each of which drive 16 channels of preamplifier. Calibrate set 0 drives preamplifer channels 0,8,16,24,32,40,48,56,64,72,80,88,96,104,112,120; calibrate set 1 drives preamplifier channels 1,9,17,25,33 etc.

To mask a calibrate set the relevant bit in the CDRV register must be set to 1. Therefore a value of 11111110 written in the register masks all channels except for channel 0. To mask all but channel 5, the register would require setting to 11011111.

5.9.2 CSEL Register

The CSEL register selects the number of delay elements connected in series following the output from the calibration edge generator. Setting this to 00000001 would mean one 3.125ns delay is switched in to the path, a setting of 00000010 would mean two 3.125ns delays are switched in, 00000100 would mean three delays, etc.

For more information concerning the calibration circuit, see separate document on the web.

5.10 Timing

The I2C standard is specified at 400 kbit/s. This is so that bus capacitances of 200 to 400pF may be used with reasonable values of pull-up resistors. The APV25-S1 internal logic is capable of running at speeds much higher than this, even up to 40MHz. The limiting factor is the external load capacitance and resistance.

5.11 Pad Specification

Since the APV25-S1 may only ever act as a slave device, it need never drive the clock line. For this reason the I2C clock is connected to one input pad *SCLK*, which is unidirectional. The data line is bi-directional, and for easy test this has been split into two pads that may be shorted external to the chip. The data input to the chip is called *SDAIN*, and the data output pad is called *SDOUT*.

6. BIASING THE APV25-S1

The current and voltage biases required by the APV25-S1 circuitry are generated by reference to either an internal or an external current source. The biases are then defined by programming registers through the I2C interface.

6.1 Defining the APV25-S1 reference current

There are two methods of supplying the APV25-S1 reference current. The first is to use the internal reference circuit. This has been designed to supply 128uA (nominally) to the bias generator. To use this method the input IREFBIAS must be connected to the middle supply (+1.25V if VSS=0V).

The second method is to connect an external current source between VDD and *IREF* (e.g. a 20k potentiometer). The nominal value for this current is +128uA. To use this method the input IREFBIAS must be connected to VDD.

6.2 Nominal settings for the APV25-S1

The nominal settings for running the APV25-S1 are different from those recommended for the s0 version of the chip. The values are designed to be a starting point; when configuring the chip some adjustment will be necessary to trim pulse shape and noise/power trade-off for ultimate system performance. The table below contains two columns of values, one for use if the bias current is provided externally (see section 6.1), the other if the internal reference is used. Values for use with the internal reference are based on tests from the first batch of s1 wafers, and may need adjustment for chips from subsequent runs. All values assume chip is powered at nominal supply voltages.

Bias Name	Description	Value (external 128uA ref.)	Value (internal ref)	Meaning
IPRE	Preamp Input FET Current Bias	85*	98*	460uA
IPCASC	Preamp Cascode Current Bias	45*	52*	60uA
IPSF	Preamp Source Follower Current Bias	30*	34*	50uA
ISHA	Shaper Input FET Current Bias	~30*	~34*	50uA
ISSF	Shaper Source Follower Current Bias	30*	34*	50uA
IPSP	APSP Current Bias	48*	55*	80uA
IMUXIN	Multiplexer Input Current Bias	30*	34*	50uA
ICAL	Calibrate Edge Generator Current Bias	25*	29*	+/- 25 000 electrons
VFP	Preamp Feedback Voltage Bias	~30*	~30*	
VFS	Shaper Feedback Voltage Bias	~60*	~60*	
VPSP	APSP Voltage Level Adjust	~40*	~40*	
CDRV	Calibrate Output Mask	11111110		Channel 0
CSEL	Calibrate Delay Select	00000001		1st of 8 delays
MODE	Mode of Operation of Chip	xx000100		See Mode Register
LATENCY	Write -> Trigger Pointer Delay	132		3.3us
MUXGAIN	Sets Gain of Multiplexer	xxx00100		100uA/mip

Table 10: Nominal Settings for the APV25-S1 Bias Registers

Note 1: Items marked * were revised at version 2.1
Note 2: Pulse shape tuning (rough guide): As detector capacitance increases ISHA needs to increase and VFS needs to be reduced. As a rough guide, for capacitances in the range 0 -> 20 pF, ISHA could be in range 20 -> 65, VFS in the range 65 -> 50.

7. RUNNING THE APV25-S1

Once set up the APV25-S1 control is achieved using only the *TRIG+ and TRIG-* inputs (complimentary). The positive input is normally held at logic 0 (and TRIG- at logic 1). Commands are sent by pulsing *TRIG+* to logic 1 (and TRIG- to logic 0) in three different ways.

7.1 Sending a RESET101

A RESET101 sequence clears any pipeline pointers and re-launches them with the programmed latency separation. This is done by sending two pulses on *TRIG* separated by a gap of one clock cycle

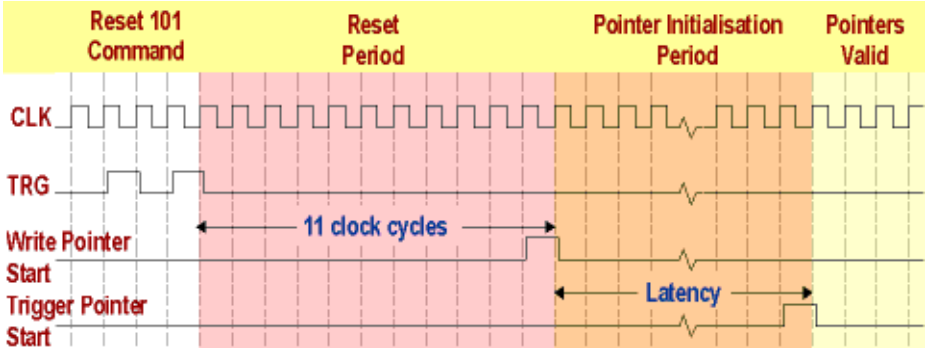


Figure 9: Sending a Reset 101

(i.e. 101). A chip reset period lasting 11 clock cycles then takes place before the write pointer is initialised. Following this, a latency period later, the trigger pointer is initialised. No triggers should be sent while the pointers are initialising (i.e 11 + latency clock cycles after a RESET101).

7.2 Sending a Trigger

This signal requests the APV25-S1 to reserve data in the pipeline for read-out. It is a single pulse on the *TRIG* line. There is a two clock cycle delay in processing the trigger request prior to it being applied to the pipeline. In *Peak* mode it will then reserve one pipeline column for read-out and in *Deconvolution* and *Multi* modes it will reserve three pipeline columns for read-out. Due to the delay in processing triggers, triggers must be separated by at least two clock cycles. This means that in peak mode it is not possible to trigger consecutive columns and for this reason the new mode of operation (Multi) has been introduced. It must be remembered that in the different modes of operation, different latency values will be required. This is because the signal will be sampled at different points on the shaping function.

7.3 Sending a Calibrate Request

This is a double pulse, *11*, on the *TRIG* line. When sensed, the APV25-S1 generates an internal step on a calibration line. This then injects charge into the input of the preamplifier. The resulting pipeline data may then be triggered a latency period later. The channels hit with the calibrate pulse, it's magnitude, polarity and timing are all programmable.

8. DATA OUTPUT FORMAT

The output from the APV25-S1 chip is in differential current form in the range +/- 4mA. When there is no data to read out, the output of the chip is at the logic 0 level, with synchronisation pulses every 70 clock cycles (in 20 MHz mode) or 35 clock cycles (in 40Mhz mode). When an event is triggered, the chip waits until the start of the next (70 or 35) clock cycle period before any data is output. A data set is then made up of four parts: a digital header, a digital address, an error bit, and an analogue data

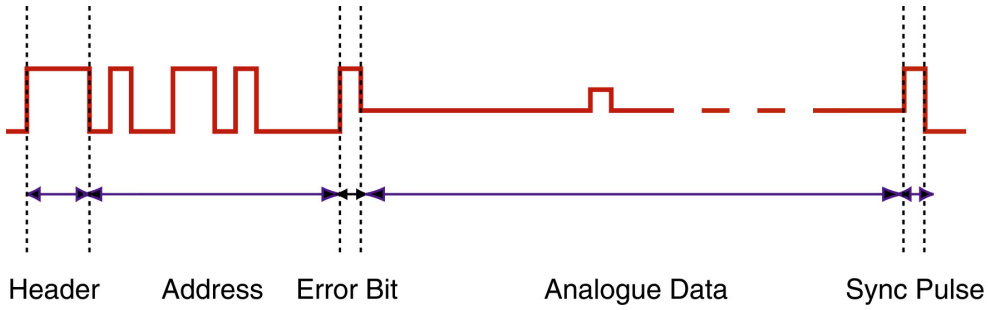


Figure 10: Analogue Data Format

set.

8.1 Header

This consists of three bits, all logic 1 (i.e. "111").

8.2 Address

This is an 8-bit number (MSB first) defining the column address that is used to store the signal when the chip is triggered. It can be used to monitor the synchronicity of many chips and as a tool to identify and remove data from bad memory locations. A table showing the column address sequence can be found on the med web.

8.3 Error Bit

This consists of one bit, normally logic 1. If an error is sensed by the APV25-S1's internal logic, the bit is switched to logic 0. This should be detected by the DAQ system. The error register can then be read out using the I2C.

8.4 Analogue Data

128 samples of analogue data, where a silicon MIP equivalent signal should be represented by a current of +/- 100uA . The baseline offset may be adjusted (using VADJ) to give optimal dynamic range in the signal polarity in which the chip is working.

8.5 Channel Order

Due to the tree structure of the analogue multiplexer, the order that channels are read out through the analogue output is non-consecutive. The multiplexer is constructed in three stages, if 'n' is the order in which the channels appear (starting at 0,1,2,3,4 etc), then the physical channel number is defined by:

Channel No. = 32 * (n MOD 4) + 8 * INT(n / 4) - 31 * INT(n / 16)

8.6 Synchronisation Pulse (or 'tick mark')

Since the chip may not output data for a considerable time it is necessary for the DAQ electronics to remain synchronised with the APV25-S1 when it eventually begins to read out data. To allow for this the chip outputs a synchronisation pulse called a 'tick mark' every 70 clocks cycles in 20 MHz mode or every 35 clock cycles in 40 Mhz mode when there is no data to read out.

8.7 Interleaving

In 20Mhz mode it is possible to interleave the outputs of two APV25-S1 chips onto one 40MHZ bus. This is achieved by delaying the output of one of the chips by one 25ns clock period. An external multiplexer can then multiplex the two signals together to form one 40MHz output. The chip addresses (define using the ADD0-ADD4 pads) determine which of the chips' data will be delayed by 25ns. Even addressed chips are not delayed, while odd addressed chips are delayed.

9. POWER CONSUMPTION

The currents flowing in the power supplies of the APV25-S1 are listed in the table below for a chip reference current of 128uA, and nominal settings in the bias generator. However, if the APV25-S1 bias generator is incorrectly programmed, then the currents can exceed these nominal values. The worst

Sub-Circuit	VDD to VSS / Channel [uA]	GND to VSS / Channel [uA]	Power / Channel [mW]
Preamplifier	60	400	0.65
Preamplifier Source Follower	50		0.125
Inverter		100	0.125
Shaper	50		0.125
Shaper Source Follower	50		0.125
APSP	80		0.2
MUX Input Stage	30		0.075
Output Stages	188		0.47
Digital	164		0.41
TOTAL / Channel	692	500	2.31

Table 11: APV25 Supply Currents

case current for each of the supplies is then listed in the subsequent table.

The worst case currents are listed in the table below.

Supply	Nominal [mA]	Worst Case [mA]
VDD (+1.25).....	+90	+243
GND (0)	+65	+165
VSS (-1.25)	-155	-374

Table 12: Total Current per Chip