# HIT SUM FPGA VERSION 1


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# HITSUM FPGA Functional Description

## Overview:

The Hit Sum FPGA receives two 8-bits Hit Bits and two 16-bits Sum Data from two ADC FPGA. The Hit Bits from are processed and the Sum Data are added.

The Hit Bits pulse width are programmable.

There are three Hit Bits processing modes that generates programable pulses. In Trigger Mode, the trigger pattern is downloaded through VME and stored in 65535x1 RAM. When the 16 Hit Bits (Hit Pattern) matched a selected pattern, Win/TO_Trig goes high. In Boolean Overlap mode, BO_Trig goes high for the duration that selected Hit Bits are all high. In Table Overlap mode, Hit Bits are switch in as address bits of the 65535x1 RAM The modes are selectable through VME.

The two 16-bits Sum Data are added. The result Board Sum (Bsum) is sent to the Switch Card through Xilinx MGT using Aurora Protocol. The sum also is also compare to a programmable threshold. When the sum is above this threshold, Sum_Triger ouput goes low for one clock (4 nS).

VME FPGA select which of four trigger to Live_Trig. Live_Trig and Latched Trigger are an LVDS and is accompanied by a CLOCK signal. Trig_Ready signal from VME FPGA needed to be accompanied by a clock so that the signal can be received properly.

The Hit Bits (programmable pulse width) and the Sum can be selected to be sent to VME P2 backplane. These signals are differential pairs and are accomodated by a clock.

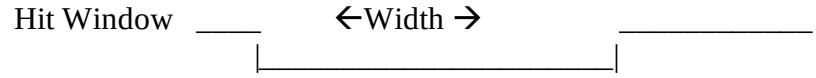
**Processing of 16-bits Hit Bits Word:**

1. The bits are active Hi. The rising edge triggers a pulse generator (one shot) of User Programmable width. This is to make all bits having same width.
2. Three modes of Operations: Trigger Mode, Boolean Overlapping Mode, and Table Overlapping Mode. The Active High output of each mode is selected by User.
3. Window Mode (Figure 1):
    a. Any bits can be selected (Trigger Selected Bits) by the User to trigger a Hit Window.
    b. The width of the Hit Window, programmable by the User, has a minimum of 4 ns and maximum of 262.14 uS (16-bits programmed word).
    c. When all the Triggered Selected Bits occurs while the Hit Window is active, a Triggered Mode Low pulse is generated. The Delay time from the rising edge (ending) of the Hit Window to the falling edge of the Triggered Mode Low is programmable from 8 ns to 262.14 us (16-bits programmed word). The width of the Trigger Mode Low is programmable from 4 ns to 262.14 us.
    d. The Triggered Selected Bits are selected by a 65535 x 1 table. An entry of one (in the address) selects that combination of bits. For Example: an entry of one at address 1, 125, 1000, 5235 select the following bit patterns:

| | Bits 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Select | | | | | | | | | | | | | | | | x | ADR 1 |
| Patterns | | | | | | | | | | x | x | x | x | x | x | x | ADR 125 |
| | | | | | | | x | x | x | x | x | | x | | | | ADR 1000 |
| | | | | x | | x | | | | x | x | x | | | x | x | ADR 5235 |

4. Boolean Overlapping Mode (Figure 2):
    a. Any bits can be selected (Overlaped Selected Bits) by the User for overlapping. The bits are selected with 16-bits word. A one entry selects the respective Hit Bit.
    b. An Overlapped Mode Low pulse is generated when there is an overlap of Overlaped Selected Bits. The pulse width is the same as the duration of the overlap.
5. Table Mode
    a. In this mode, the bits are the address of the 65535x1 table. The table is described in section 3.d above.
6. When a hit occurs in any mode, Live Trigger pulse high. If Trig_Ready is high, the 32-bits Hits word is stored in a external FIFO to be read by VME FPGA Figure 3 illustrates FIFO data storage using example in 3 above. It takes two read cycle from VME FPGA to read the 32-bits Hit Word. The first read reads the Hit Number and the second read reads the Hit Pattern.

Figure 1: Trigger Mode



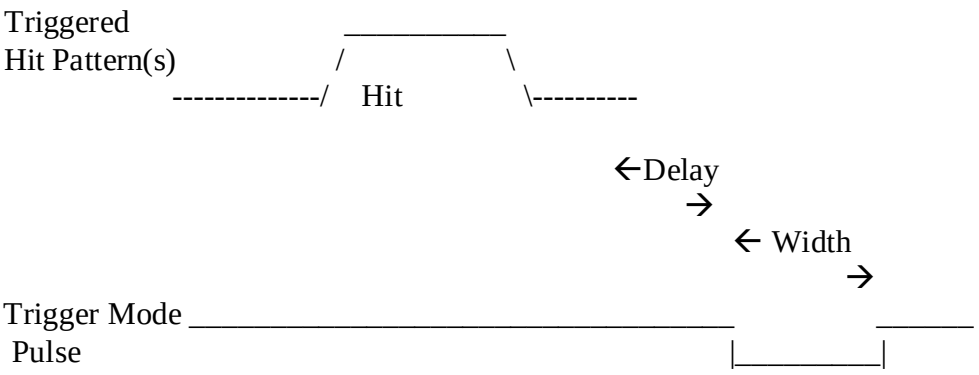



Figure 2: Overlapped Mode

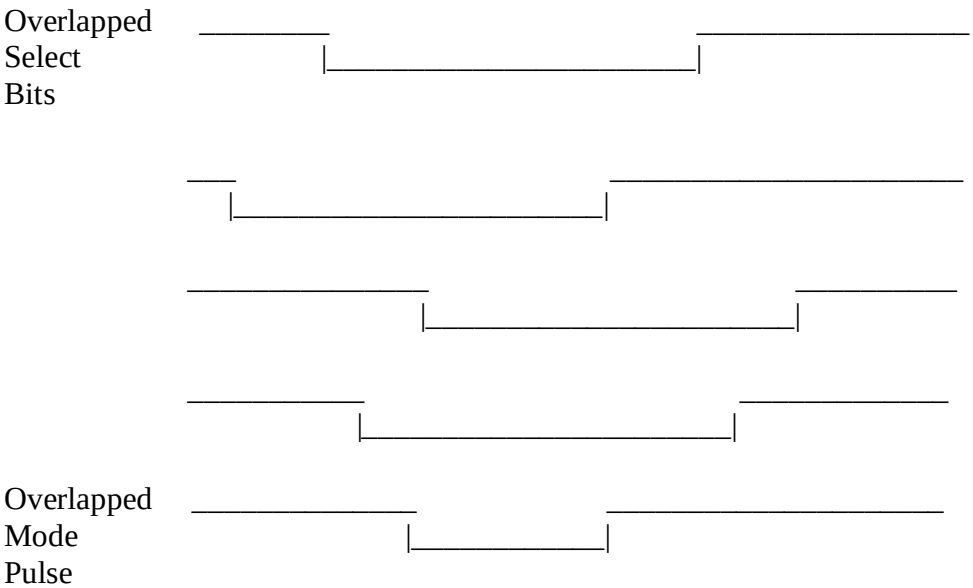


Figure 3: FIFO Storage for Hits on Patterns (1, 1000, 125, 1, 5235.

| FIFO Address | Event Number (upper 16 bits) | Hit Patterns (lower 16 bits) |
|---|---|---|
| 0 | 1 | 1 |
| 1 | 2 | 1000 |
| 2 | 3 | 125 |
| 3 | 4 | 1 |
| 4 | 5 | 5235 |
| | | |

**SUM Processing:**

The two 16-bits SUM from the two ADC FPGA are added together. Since the sixteen ADC on the FADC board are 12 bits, the (total) sum is 16-bits wide. The sum is input to Xilinx MGT circuit to be sent to the Switch Card using Aurora protocol. When the sum is above a programmable threshold, Sum_trig goes high.

**Processing of Live Trigger:**

VME FPGA selects via register which trigger: Sum_Trig, Win/TO_Trig, BO_Trig to drive the Live Trigger output. If Trig_Ready is high, the 32-bits Hit Word is written to external FIFO. Latched_Trigger goes high to indicate that the 32-bits Hit Word is written to FIFO. The Trig_Ready need to go low to acknowledge Latched_Trigger. Latched_Triigger goes back low. Figure 4 shows the connections between VME FPGA, HIT SUM FPGA, and FIFO. Figure 5 shows the timing relationship. VHDL "Extern FIFO Write" code handles the timing relationship and generates the FIFO clock.

Figure 4: Connections for Trigger.

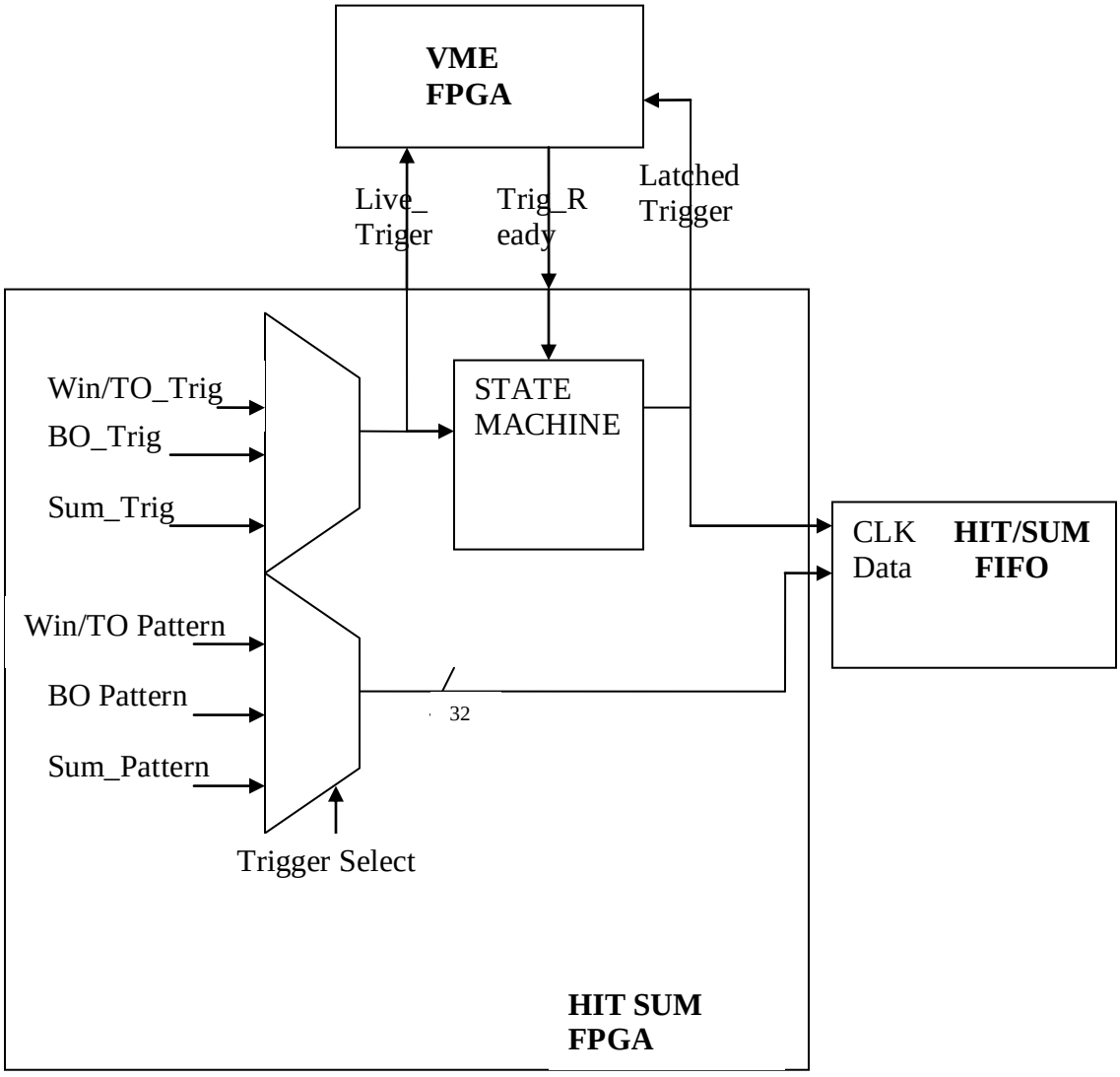
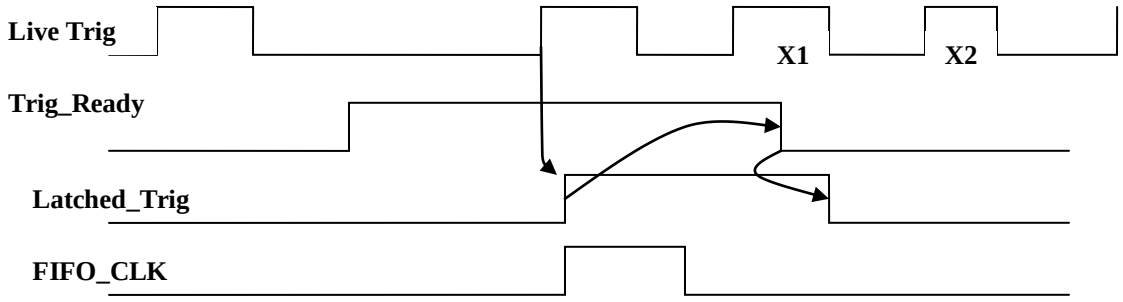


Figure 5: Live TriggerTiming diagram




**Trigger X1 is ignored because present trigger process is not done.**
**Trigger X2 is ignored because Trig Ready is low**

**Reset:**

There is only Hard Reset in this FPGA. When Hard Reset is low, everything is reset. It is power on reset. Soft Reset is not implemented. When Soft Reset is active (low) on board, ADC (LX25) FPGA held HITBITS and SUM inactive (low). HitSum FPGA is inactive if HITBITS and SUM are inactive. There is no Sync Reset since there is no 48 bits time-stamp counter.

# VHDL Block Diagram

Figure 6: VHDL Top Level

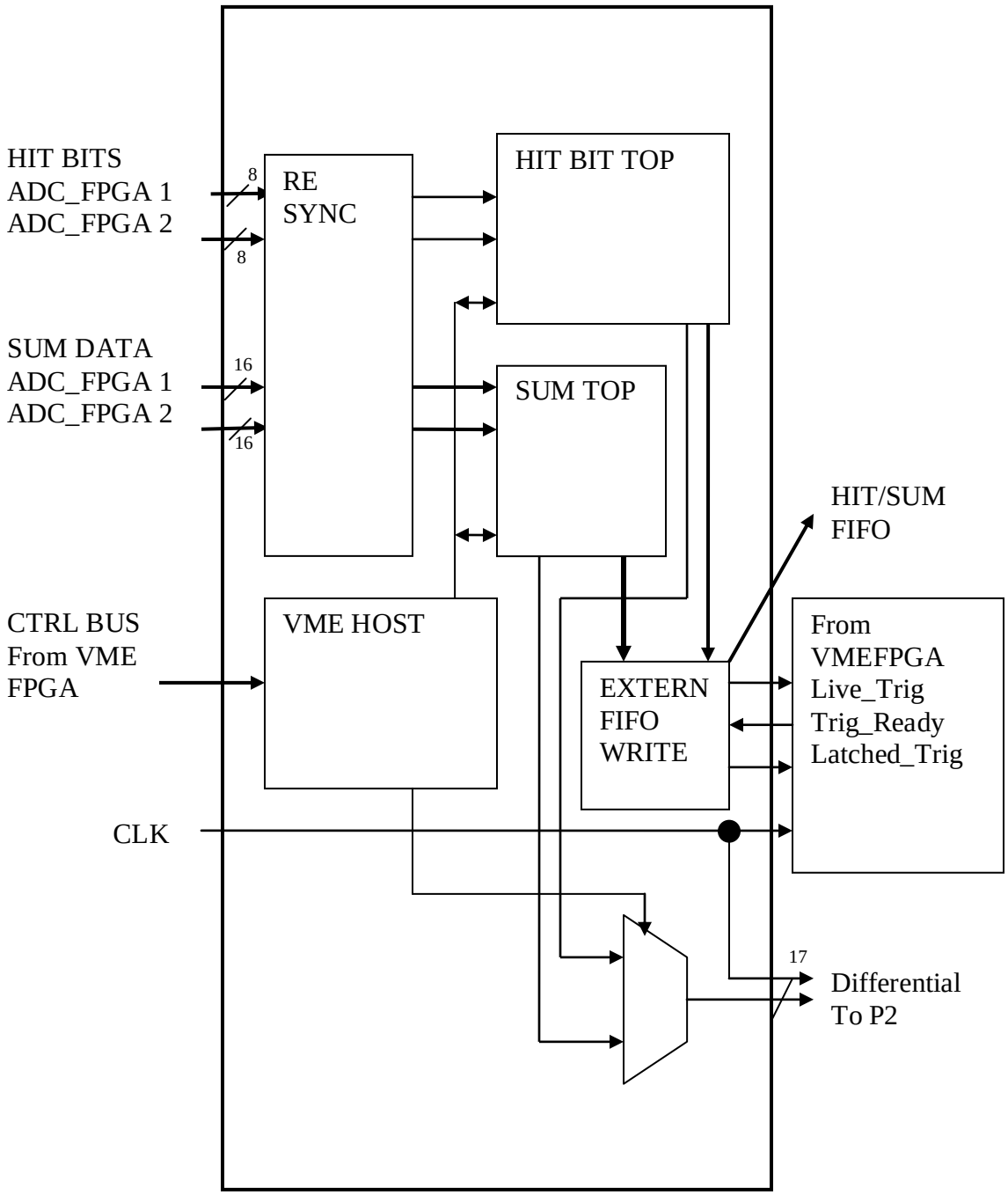
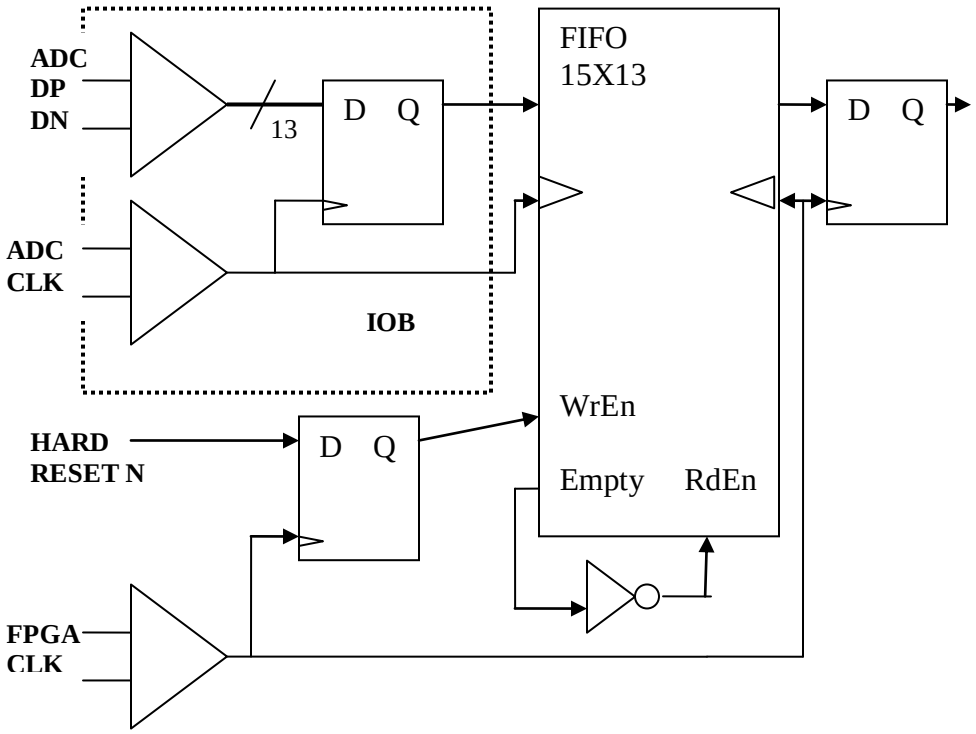
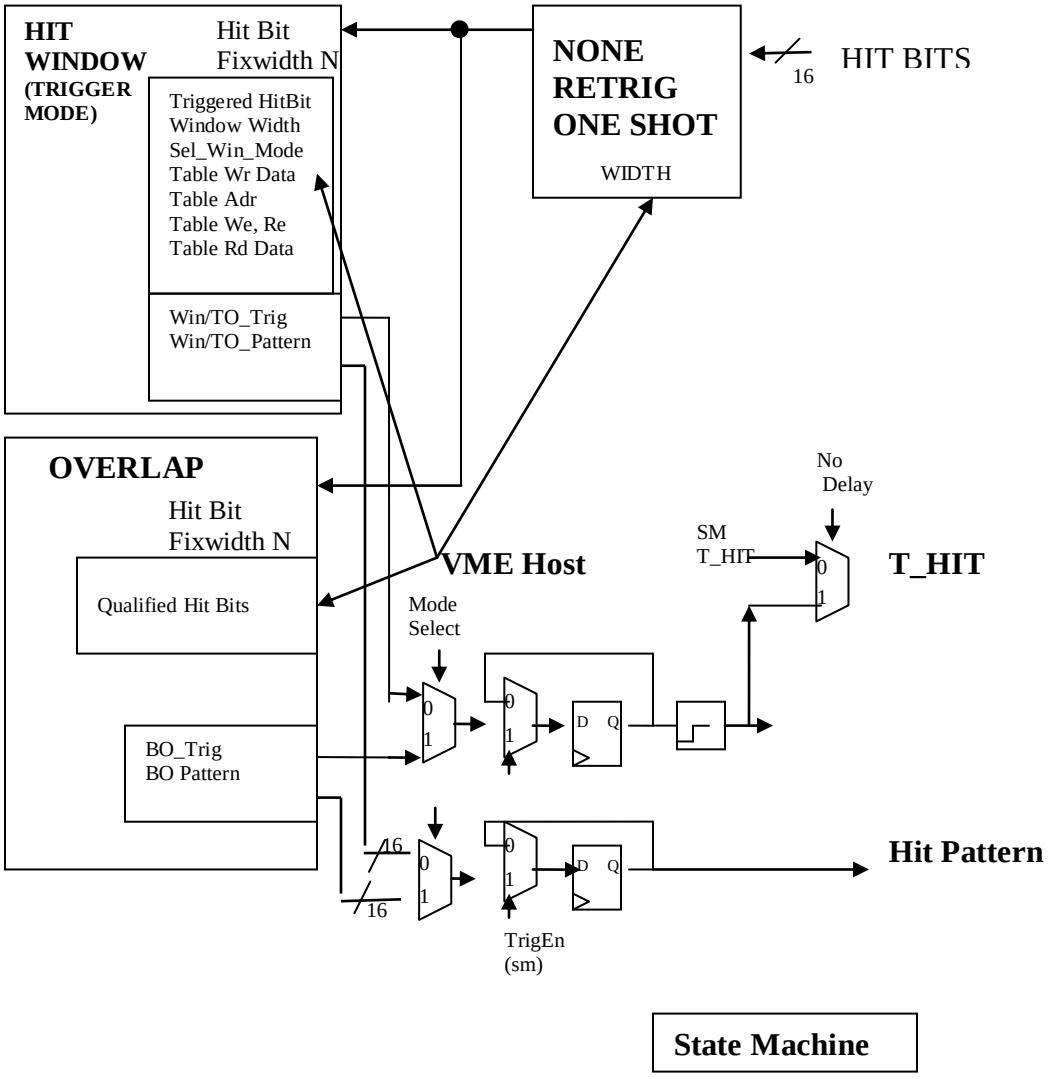


**Figure 7: Resync**




The Resync Circuit receives the data from the ADC FPGA and synchronize the captured data to the Hit SUM's CLK. The clock of the ADC FPGA and the Hit Sum FPGA are asynchronous even if the two FPGA are clocked from the same clock source because the clock to out time of the ADC FPGA plus the setup and hold time of the Hit Sum FPGA is longer than the CLK period (4 nS). To properly transfer the data between the ADC FPGA also sending a ClockOut to accompany the data. The FIFO allows the data to be synchronized to Hit Sum's CLK by the fact FIFO read clock is independent from FIFO write clock.

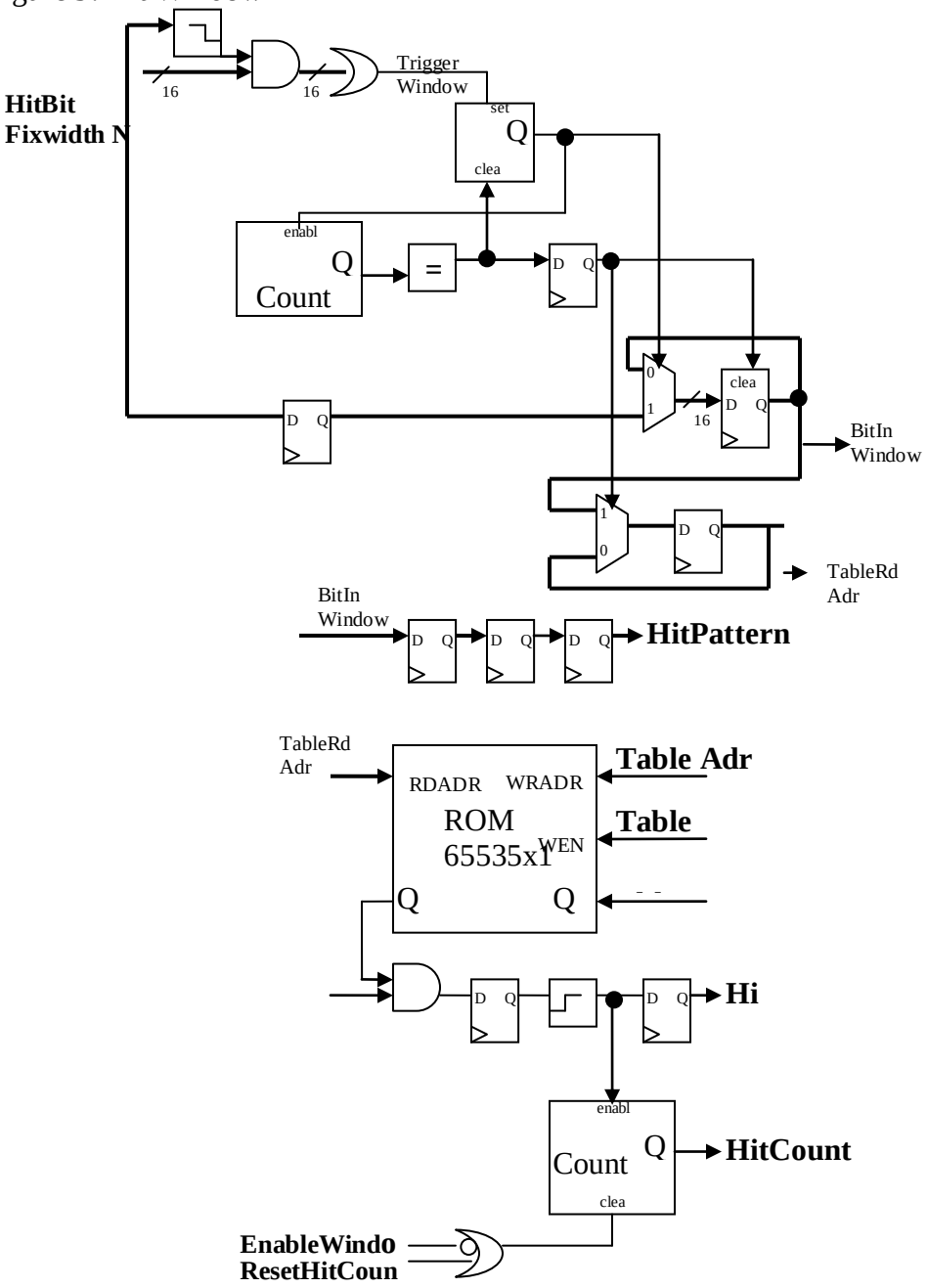
Figure 8: HIT BIT Top




Hit Bit Top switch the output of
Window or Overlap to Extern_FIFO_WRITE.
Mode from VME select one or the others.

It also delay the output of Hit or Overlap and Stretch the width to HitDly and HitWidth. Both parameters are set by VME host. State Machine handles HitDly and Hit Width

Figure 9: Hit Window

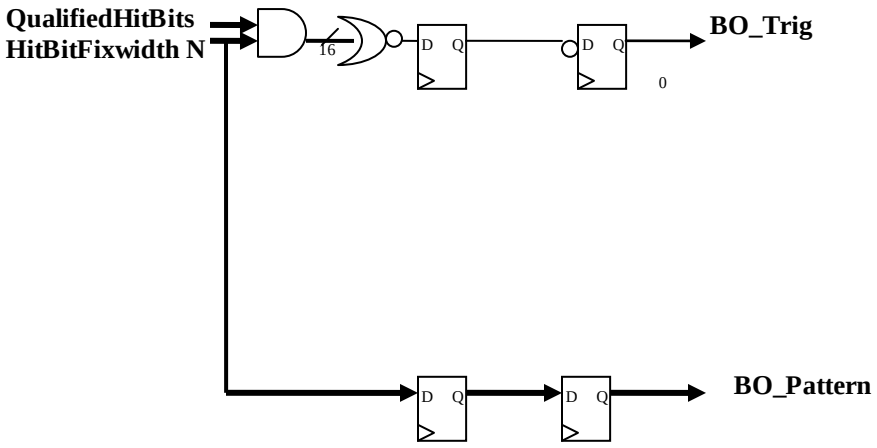



Hit Window does the following

On falling edge of any HitBit(s) that select to participate in Window mode, a programmable pulse width (Window) is generated. During this Window , any rising edge HitBits is registered as HitPattern. At end of Window, the HitPattern is latch to ROM address. The output of that ROM address is output on Hit port.

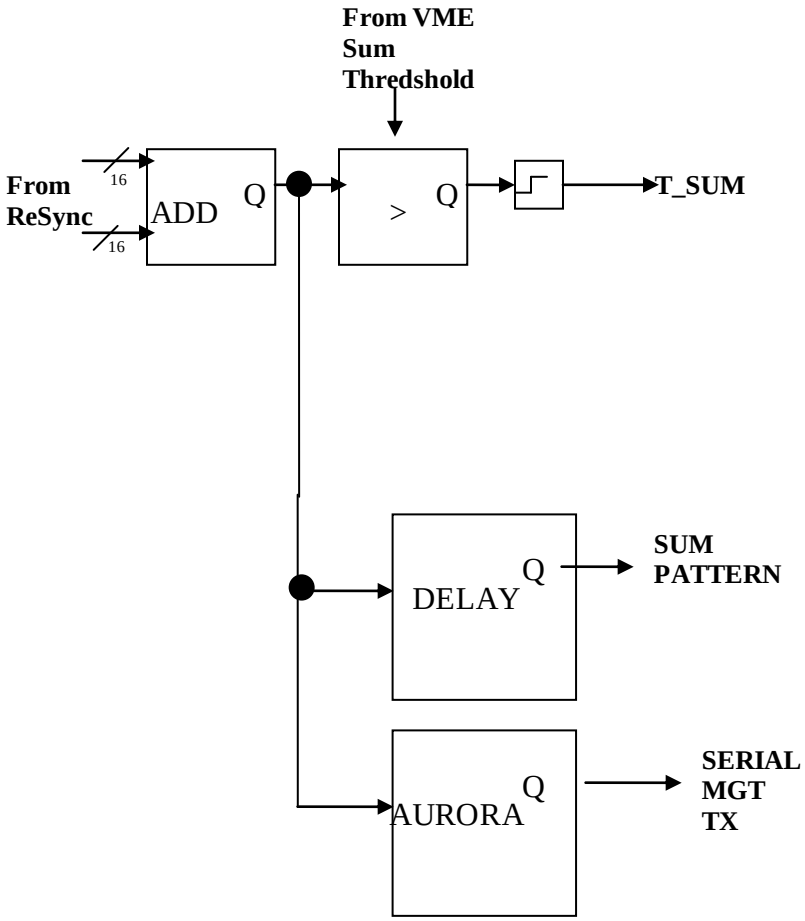
TableRdAdr can come from VME Address, HitBits, or HitPattern (window).

Figure 10: Overlap

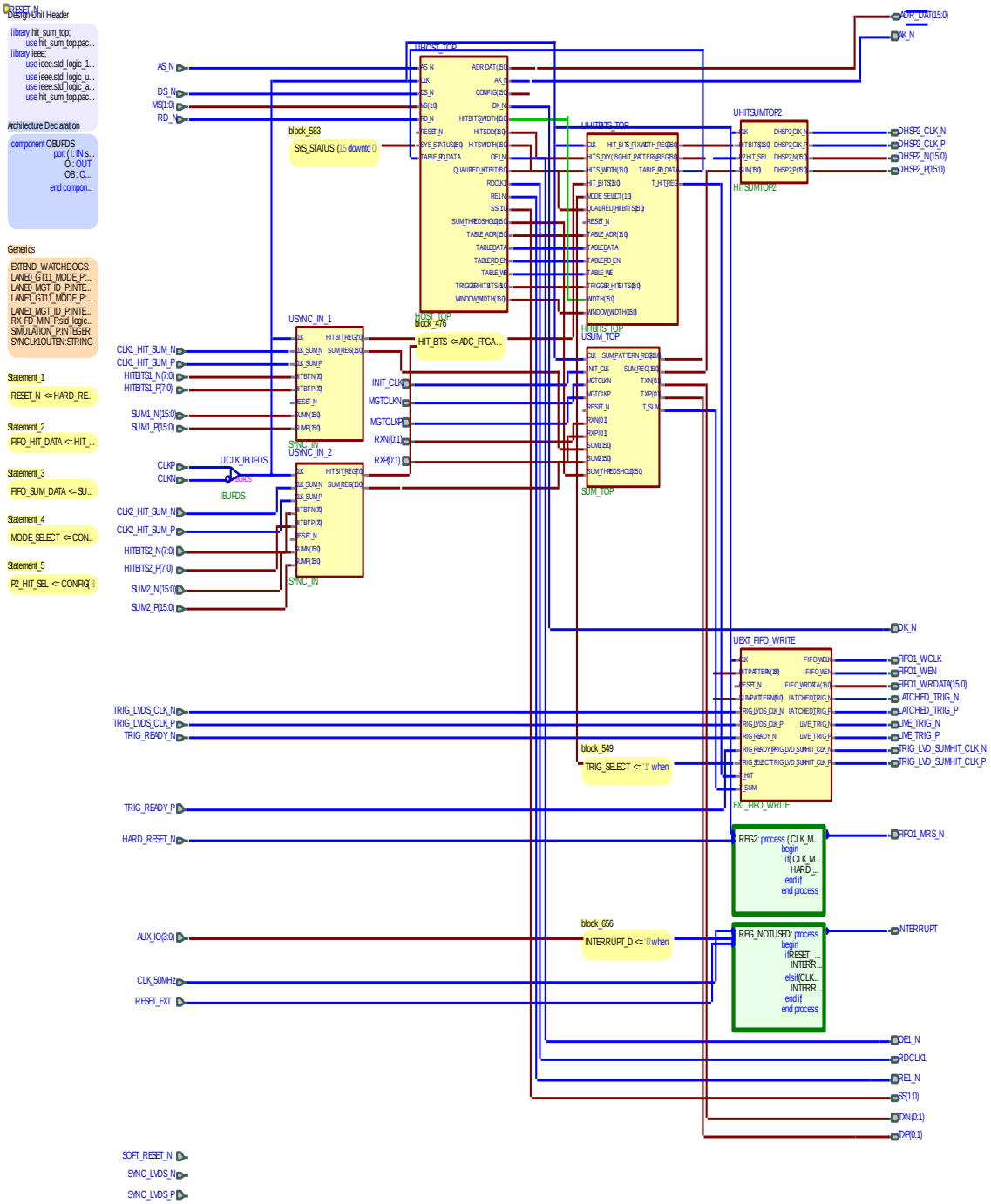



When there is an overlap of low of Qualified Hit Bits, Overlap goes low for the duration of overlap.

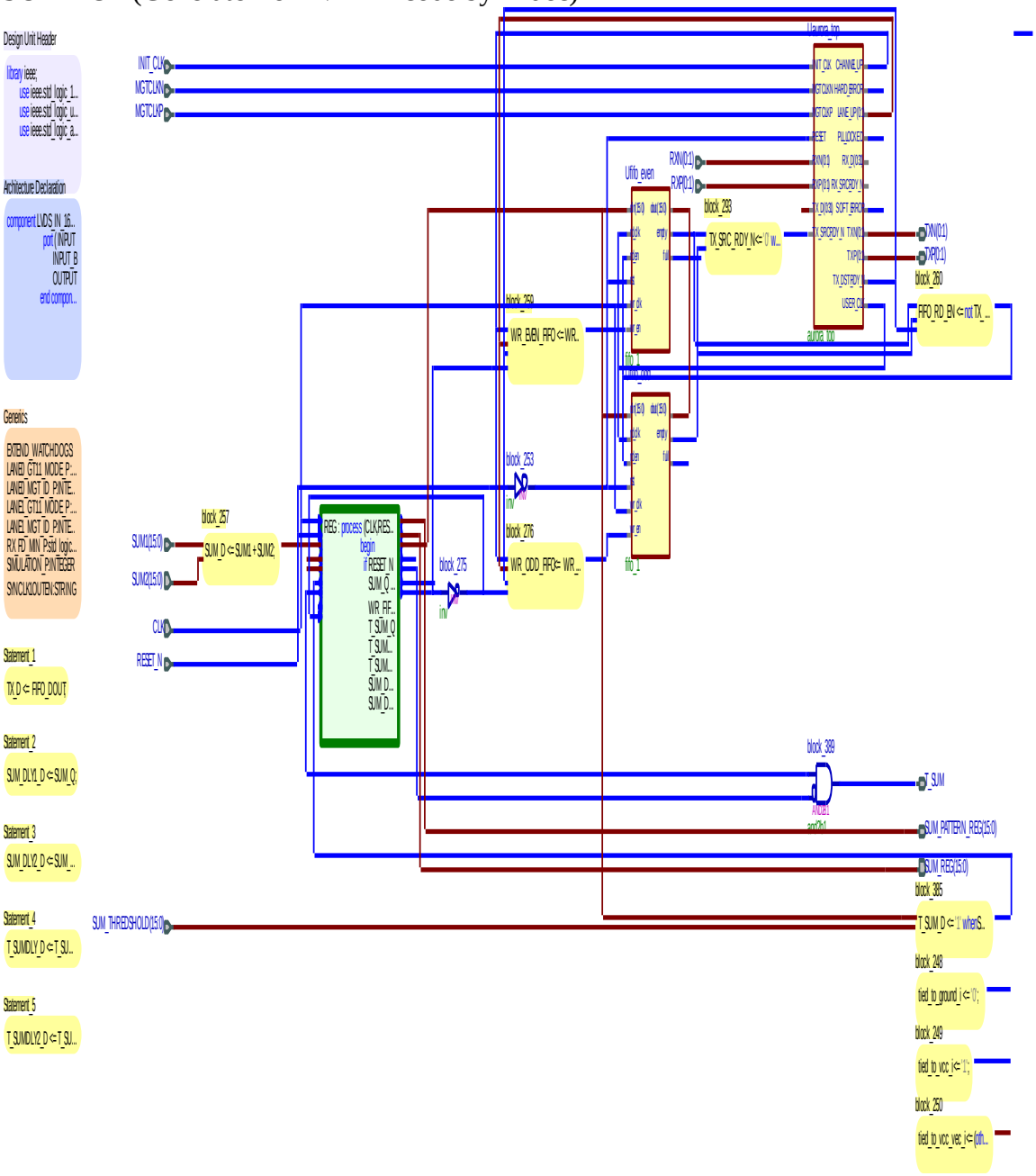
Figure 11: SUM



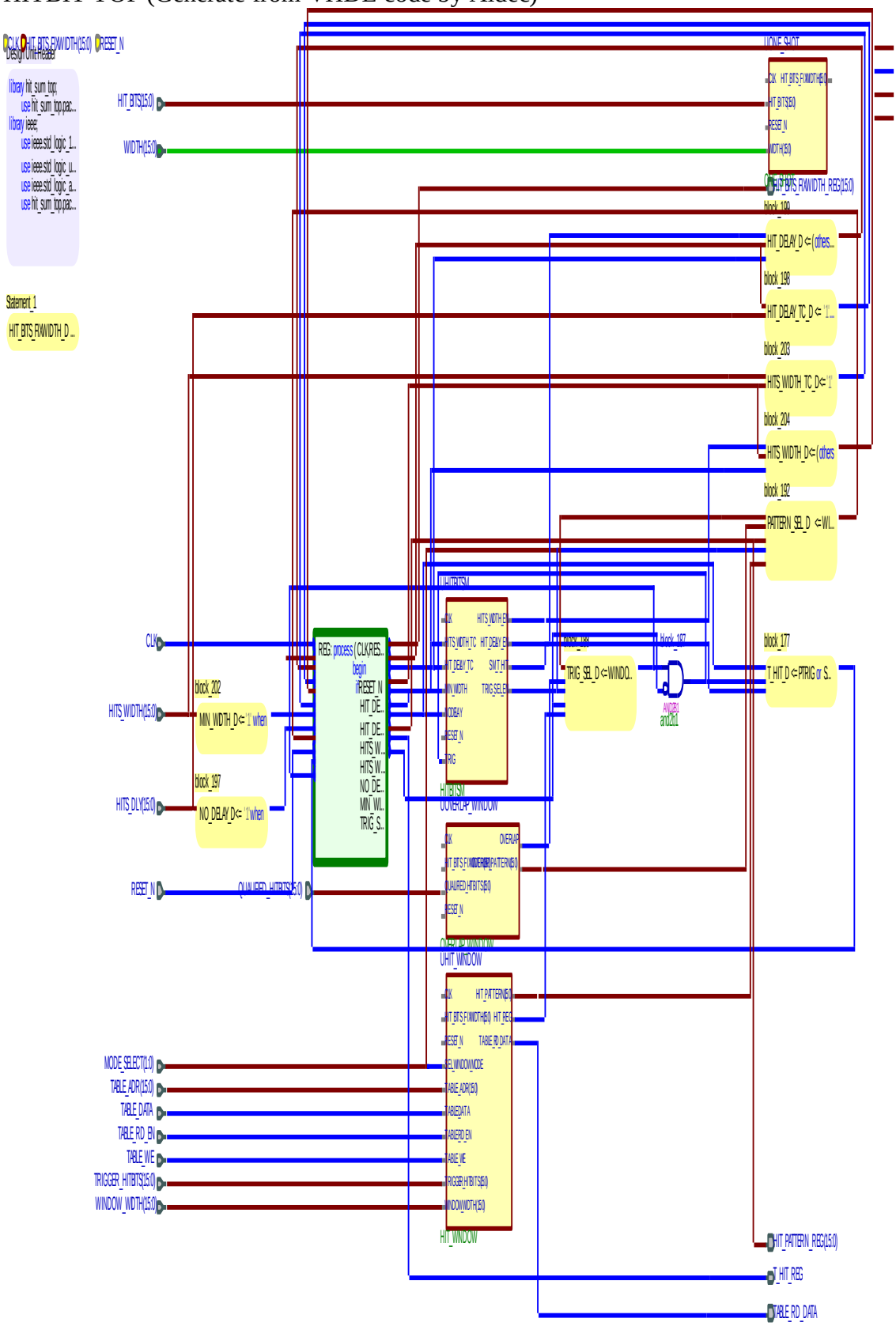
# HITSUM TOP (Generate from VHDL code by Aldec)



SUM TOP (Generate from VHDL code by Aldec)



HITBIT TOP (Generate from VHDL code by Aldec)



Aurora TOP (Generate from VHDL by ALDEC)

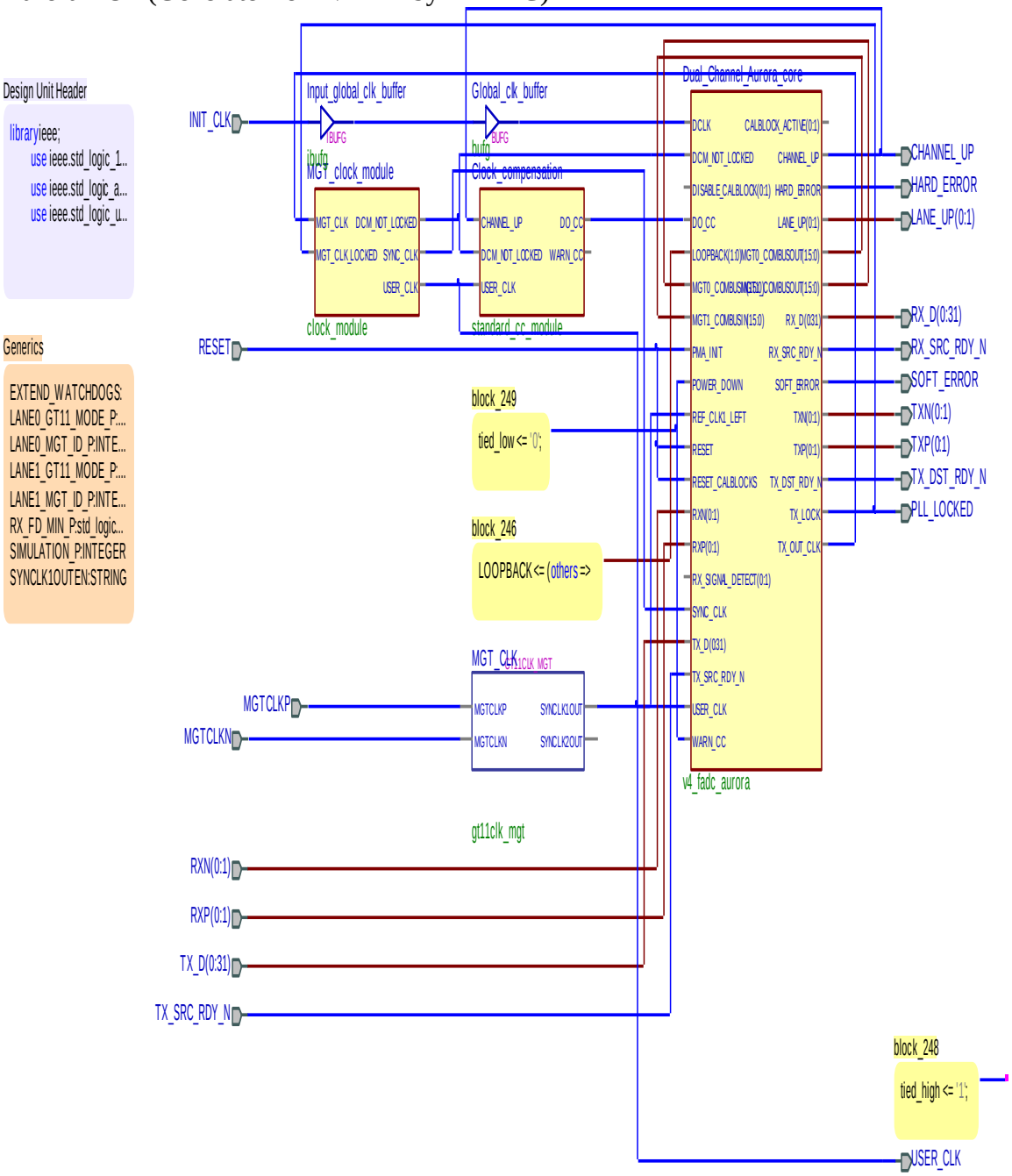


Figure 12: Control Bus Address Map

**Do not use burst mode.**

| Name | Width (Bits) | Quantity | Access | Primary Address (Secondary Address) | Function |
|---|---|---|---|---|---|
| STATUS | 16 | 1 | R | 0x0400 (---) | Active HI |
| CONFIGURATION | 16 | 1 | R/W | 0x0401 (---) | 00→ Table mode<br>10→ Window mode<br>01→ Boolean Overlap<br>11→ undefined<br><br>Bit 2: 0→ T_HIT to Ctrl FPGA, Hitpattern to FIFO<br>1→ T_SUM to Ctrl FPGA, Sumpattern to FIFO<br><br>Bitt3: 1→ select Hit Bit with programmable positive pulse width to P2.<br>0→ select Sum to P2<br><br>Bit4 0→ unable Table overlap and Trigger mode<br>1→ read back hit pattern selection table. Disable Table overlap and Trigger mode. |
| HITBITS_WIDTH | 16 | 16 | R/W | 0x0402 (0 – 0x000F) | Hit Bits One Shot Pulse Width. Actual width is one clk longer. |
| HITS_DLY | 16 | 1 | R/W | 0x0403 | Actual delay is 14 clock longer for all values. Exmple: 0→ 14, 1→ 15, 2→ 16 etc. Delay is from input of FX20. |
| Live Trig Out WIDTH | 16 | 1 | R/W | 0x0404 | Pulse width of LiveTrig Output. Actual width is 2 clock longer. A value |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | of 0 produces no pulse. |
| TRIGGER HITBITS | 16 | 1 | R/W | 0x0405 | In Window Mode. Select Hit Bit(s) that can activate(s) window. The Bit(s) that activate the Window is include in the Trigger Hit Pattern. |
| WINDOW WIDTH | 16 | 1 | R/W | 0x0406 | In Window Mode. Select the duration of window. Width is 2 clock longer. |
| BOOLEAN OVERLAP QUALIFIED BITS | 16 | 1 | R/W | 0x0407 | In Boolean Overlap Mode. Select Hit Bits to be active in this mode |
| HIT PATTERN SELECTION TABLE DATA | 16 | 65536 | R/W | 0x0408 | Write to 65536x1 Hit Pattern Selection Table. Each word contains data for 1 location. The address are auto-increment. |
| SUM/HITBIT External FIFO | 16 | | R | 0x0409 | Read HITBITS |
| SUM Threshold | 16 | 1 | R/W | 0x40A | Write SUM Threshold Register. T_SUM goes high when BSUM > register value |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

NOTE #1: For Trigger Mode (Configuration bit 1,0 = 10), delay time from end of window to beginning of Live Trigger high.