Front Panel Signal Distribution Module for the F1TDC

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5/12/09

Summary

The signal distribution module supports a set of up to five F1TDC modules through their front panel interfaces. Common CLOCK, START, TRIGGER, and SYNC_RESET signals are distributed with low skew to each of the F1TDC boards. BUSY signals from the F1TDC modules are collected and ORed together.

The signal distribution module can serve as the source of the common 40 MHz system CLOCK, or an external CLOCK signal can be accepted. The module can also generate a local SYNC_RESET pulse instead of using the external SYNC_RESET input. The programmer has access to the current BUSY status of the set of connected F1TDC modules.

The module requires a VME64x backplane.

Input/Output Signals

Figure 1 identifies the front panel connectors. **Tables 1 - 4** describes the signals carried and their pin assignments.

Table 1. Connector **A** signal definition. (Pin 1 is *lower-right*.)

Signal name	Direction	Level	Pin # (Q(+), /Q(-))
EXT CLOCK	input	LVPECL	14, 13
---	---	---	12, 11
CLOCK	output	LVPECL	10, 9
CLOCK	output	LVPECL	8, 7
CLOCK	output	LVPECL	6, 5
CLOCK	output	LVPECL	4, 3
CLOCK	output	LVPECL	2, 1

Table 2. Connector **B** signal definition. (Pin 1 is *lower-right*.)

Signal name	Direction	Level	Pin # (Q(+), /Q(-))
EXT START	input	NECL	10, 9
EXT SYNC_RESET	input	NECL	8, 7
EXT TRIGGER	input	NECL	6, 5
(Ground)	------	(0 V)	4, 3
OR BUSY	output	NECL	2, 1

Table 3. Connector **C-F** signal definition. (**C-F**: *top-to-bottom* Lemo connectors.)

Signal name	Direction	Level	Connector
EXT START	input	NIM	**C**
EXT SYNC_RESET	input	NIM	**D**
EXT TRIGGER	input	NIM	**E**
OR BUSY	output	NIM	**F**

Table 4. Connector **1-5** signal definition. (Pin 1 is *lower-right*.)

Signal name	Direction	Level	Pin # (Q(+), /Q(-))
START	output	NECL	10, 9
SYNC_RESET	output	NECL	8, 7
TRIGGER	output	NECL	6, 5
--------	--------	--------	4, 3
BUSY	input	NECL	2, 1

Note: Inputs with the same name on connectors **B** & **C-E** are ORed together.

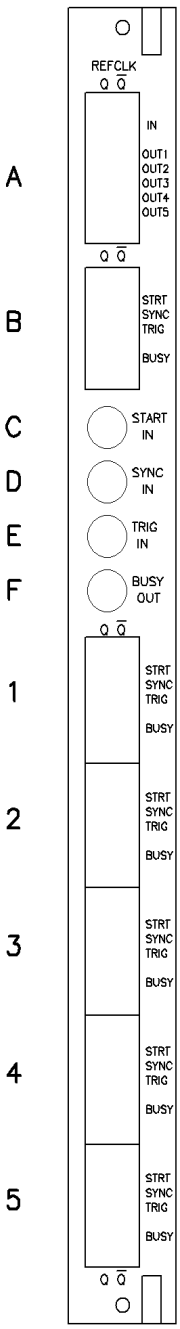

Figure 1. Front panel layout

Module Registers

The module is programmed by the user through VMEbus protocols (ANSI/IEEE STD1014-1987). The device meets all VMEbus standards. The module is categorized as an A16-D16 VME64x slave. All storage locations can be accessed as both Short Supervisory and Short Non-privileged data.

The base address (A15 – A4) is selected by DIP switches on the board. An open switch element represents a '1'. The module occupies 16 bytes of VME address space organized in eight 2-byte registers. Two registers are currently defined. The remaining space is reserved for testing and future use.

1. CONTROL/STATUS REGISTER (CSR) [addr = 0]

   (0) CLOCK SELECT (R/W) – '0' = external, '1' = internal.

   (1) SYNC_RESET SELECT (R/W) – '0' = external, '1' = internal.

   (2) – (6) – not used (read as '0')

   (7) BUSY STATUS (R) – state of the BUSY output of the module ('1' = BUSY asserted = 'OR' of all connected F1TDC modules).

   (8) – (15) – not used (read as '1').

2. CONTRL (CTRL) (Write only) [addr = 2]

   (0) INITIALIZE (W) – writing a '1' to this bit resets the board to the power-up state.

   (1) PULSE SYNC_RESET (W) – writing a '1' to this bit generates a pulse on the SYNC_RESET outputs if CSR(1) = 1.

   (2) – (15) – not used.

Notes: (1) Power-up / initialize state: CSR = 0.
(CSR = 0 => use external CLOCK and external SYNC_RESET inputs.)