Front Panel Signal Distribution Module for the FADC250

SD-FP

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Summary

The signal distribution module (SD-FP) supports a set of up to seven FADC250 modules through their front panel interfaces. Common CLOCK, TRIGGER, and SYNC_RESET signals are distributed with low skew to each of the FADC boards. BUSY signals from the FADC modules are collected and ORed together. MOD_TRIGGER signals from the FADC modules are collected and driven out for use by external logic.

The SD-FP can be used in stand-alone mode, or together with the Trigger Interface module (TI). In stand-alone mode, the SD-FP can serve as the source of the 250 MHz CLOCK, or an external CLOCK signal can be accepted. External TRIGGER and SYNC_RESET signals are then synchronized to the chosen clock (as required by the FADC module). When in TI mode, the SD-FP simply fans out the CLOCK, TRIGGER, and SYNC_RESET signals provided by the TI.

The SD-FP module can generate TRIGGER and SYNC_RESET pulses by writing to a module register. These signals are always synchronized to the selected clock (internal or external). The programmer has access to the current BUSY status of each connected FADC module, and can set a mask identifying the FADC modules that can contribute to the ORed BUSY output.

The SD-FP module also interfaces CLOCK, TRIGGER, SYNC_RESET, MOD_TRIGGER, and BUSY signals onto user pins of the VME P2 connector. This allows expansion of the system to more than seven FADC modules if a P2 distribution scheme is introduced.

Input/Output Signals

Figure 1 identifies the SD-FP front panel connectors. **Tables 1 - 4** identify the signals carried and their pin assignments.

Table 1. Connector **1-7** signal definition (FADC ⇔ SD-FP). (Pin 1 is *lower-left*.)

Signal name	Direction	Level	Pin # (Q, /Q)
--------	--------	--------	1, 7
BUSY	input	LVDS	2, 8
MOD TRIGGER	input	LVDS	3, 9
TRIGGER	output	LVPECL	4, 10
SYNC_RESET	output	LVPECL	5, 11
CLOCK	output	LVPECL	6, 12

Table 2. Connector **A** signal definition (TI ⇔ SD-FP). (Pin 1 is *lower-right*.)

Signal name	Direction	Level	Pin # (Q, /Q)
OR BUSY	output	NECL	1, 2
EXT TRIGGER	input	NECL	3, 4
EXT SYNC_RESET	input	NECL	5, 6
(Ground)	------	(0 V)	7, 8
EXT CLOCK	input	NECL	9, 10

Table 3. Connector **B-E** signal definition. (**B-E**: *top-to-bottom* Lemo connectors.)

Signal name	Direction	Level	Connector
EXT CLOCK	input	NIM	**B**
EXT SYNC_RESET	input	NIM	**C**
EXT TRIGGER	input	NIM	**D**
OR BUSY	output	NIM	**E**

Table 4. Connector **F** signal definition (SD-FP => EXT_LOGIC). (Pin 1 is *lower-right*.)

Signal name	Direction	Level	Pin # (Q, /Q)
MOD 1 TRIGGER	output	NECL	1, 2
MOD 2 TRIGGER	output	NECL	3, 4
MOD 3 TRIGGER	output	NECL	5, 6
MOD 4 TRIGGER	output	NECL	7, 8
MOD 5 TRIGGER	output	NECL	9, 10
MOD 6 TRIGGER	output	NECL	11, 12
MOD 7 TRIGGER	output	NECL	13, 14
MOD P2 TRIGGER	output	NECL	15, 16

Notes: (1) MOD TRIGGER (connector ‘**n**’) => MOD ’n’ TRIGGER (connector **F**); (n = **1…7**).

(2) Inputs with the same name on connectors **A** & **B-E** are ORed together.

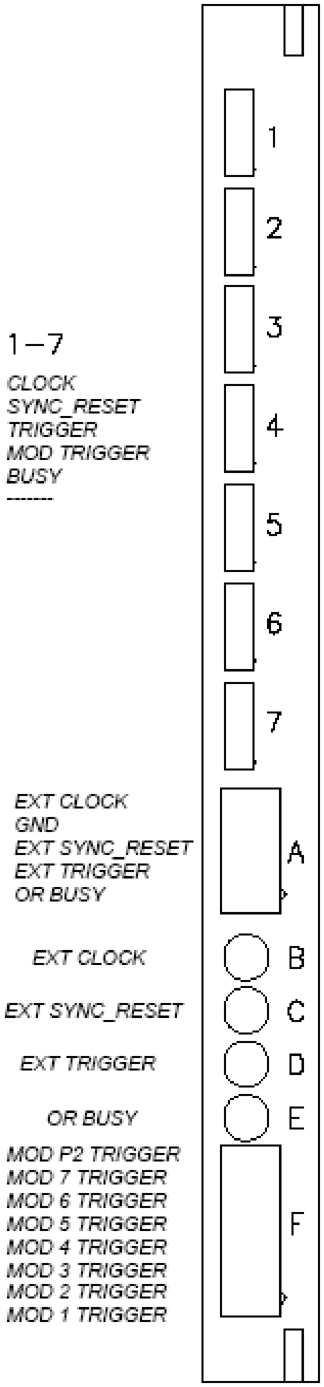

Figure 1. SD-FP front panel

SD-FP Registers

The SD-FP is programmed by the user through VMEbus protocols (ANSI/IEEE STD1014-1987). The device meets all VMEbus standards. The VME Trigger Interface is categorized as an A16 - D16 VMEbus slave. All storage locations can be accessed as both Short Supervisory and Short Non-privileged data.

The base address (A15 – A6) is selected by DIP switches on the board. An open switch element represents a '1'. The module occupies 64 bytes of VME address space organized in 32 2-byte registers. Four registers are currently defined. The remaining space is reserved for testing and future use.

1. <u>CONTROL/STATUS REGISTER (CSR)</u> [addr = 0]

(0) BUSY STATUS (R) – state of the BUSY output of the module ('1' = BUSY asserted). Includes the OR of all enabled FADC busy signals (BUSY ENABLE register) and the module soft busy assert bit (CTRL(15)).

(1) – (4) – not used (read as '0')

(5) PULSE TRIGGER (W) – writing a '1' to this bit generates a pulse on the TRIGGER outputs if software triggers are enabled (CTRL(5) = 1).

(6) PULSE SYNC_RESET (W) – writing a '1' to this bit generates a pulse on the SYNC_RESET outputs if software sync_resets are enabled (CTRL(9) = 1).

(7) INITIALIZE (W) – writing a '1' to this bit resets the board to the power-up state.

(15) – (8) – firmware version.

2. <u>CONTRL (CTRL)</u> [addr = 2]

(0) CLOCK SELECT (R/W) – '0' = internal, '1' = external.

(1) – (3) – not used (read as '0')

(4) TRIGGER SELECT (R/W) – '0' = synchronize TRIGGER input to selected CLOCK, '1' = DO NOT synchronize TRIGGER to CLOCK.

(5) SOFT TRIGGER ENABLE (R/W) – '1' = enable, '0' = disable.

(6) – (7) – unused (read as '0')

(8) SYNC_RESET SELECT (R/W) – '0' = synchronize SYNC_RESET input to selected CLOCK, '1' = DO NOT synchronize SYNC_RESET to CLOCK.

(9) SOFT SYNC_RESET ENABLE (R/W) – '1' = enable, '0' = disable.

(10) – (14) – unused (read as ‘0’)

(15) SOFT BUSY ASSERT (R/W) – ‘1’ = assert

3. BUSY ENABLE [addr = 4]

(0) ENABLE FADC 1 BUSY (R/W) – ‘1’ = use in OR busy

(1) ENABLE FADC 2 BUSY (R/W) – ‘1’ = use in OR busy

(2) ENABLE FADC 3 BUSY (R/W) – ‘1’ = use in OR busy

(3) ENABLE FADC 4 BUSY (R/W) – ‘1’ = use in OR busy

(4) ENABLE FADC 5 BUSY (R/W) – ‘1’ = use in OR busy

(5) ENABLE FADC 6 BUSY (R/W) – ‘1’ = use in OR busy

(6) ENABLE FADC 7 BUSY (R/W) – ‘1’ = use in OR busy

(7) ENABLE P2 BUSY (R/W) – ‘1’ = use in OR busy

(8) - (15) - not used (read as ‘1’)

4. BUSY STATUS [addr = 6]

(0) FADC 1 BUSY STATUS (R) – ‘1’ = busy asserted and FADC 1 busy enabled

(1) FADC 2 BUSY STATUS (R) – ‘1’ = busy asserted and FADC 2 busy enabled

(2) FADC 3 BUSY STATUS (R) – ‘1’ = busy asserted and FADC 3 busy enabled

(3) FADC 4 BUSY STATUS (R) – ‘1’ = busy asserted and FADC 4 busy enabled

(4) FADC 5 BUSY STATUS (R) – ‘1’ = busy asserted and FADC 5 busy enabled

(5) FADC 6 BUSY STATUS (R) – ‘1’ = busy asserted and FADC 6 busy enabled

(6) FADC 7 BUSY STATUS (R) – ‘1’ = busy asserted and FADC 7 busy enabled

(7) P2 BUSY STATUS (R) – ‘1’ = busy asserted and P2 busy enabled

(8) FADC 1 BUSY STATUS (unmasked) (R) – ‘1’ = busy asserted

(9) FADC 2 BUSY STATUS (unmasked) (R) – ‘1’ = busy asserted

(10) FADC 3 BUSY STATUS (unmasked) (R) – ‘1’ = busy asserted

(11) FADC 4 BUSY STATUS (unmasked) (R) – ‘1’ = busy asserted

(12) FADC 5 BUSY STATUS (unmasked) (R) – ‘1’ = busy asserted

(13) FADC 6 BUSY STATUS (unmasked) (R) – ‘1’ = busy asserted

(14) FADC 7 BUSY STATUS (unmasked) (R) – ‘1’ = busy asserted

(15) P2 BUSY STATUS (unmasked) (R) – ‘1’ = busy asserted

Notes: (1) Power-up state: CTRL = 0, BUSY ENABLE = 0.
(CTRL = 0 => internal CLOCK, synchronize TRIGGER & SYNC_RESET to CLOCK, soft TRIGGER & SYNC_RESET generation disabled.)

(2) Disconnected BUSY inputs (connectors **1-7**) default to a high (asserted) state. Use the BUSY ENABLE register to enable only those inputs that are connected to functioning FADC modules.