VME Trigger Interface

Version 2

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The VME Trigger Interface

Introduction

As part of a data acquisition system a VME read out controller (ROC) must be told when to extract data from the front end modules under its control. The experimenter's trigger system is the origin of this signal, and it may be capable of supplying information about the character of the event as well. The VME trigger interface enables a VME read out controller to have access to this trigger information. This data may be used by the ROC to selectively read the subset of modules most relevant to that event.

The VME Trigger Interface module can accept triggers from one of two possible sources: the Trigger Supervisor (TS) or external triggers.

The TS mode is useful for multiple ROC systems. In this mode the trigger data (8 bits) enters the interface module through a special parallel trigger cable driven by the Trigger Supervisor. This cable links all ROCs in the system. The TS itself maintains system busy and asserts signals that are used for gating front end modules. Every ROC in the system must acknowledge to the TS that it has finished handling the front end data relevant to the current trigger before new trigger data can be sent by the TS. When in TS mode the VME Trigger Interface allows the VME ROC to execute this protocol. (For more information see the Trigger Supervisor User Manual.)

The external trigger mode is useful for single ROC systems or test setups. In this mode up to 4 independent free running user triggers and 8 data levels can be accepted. When the OR of the 4 triggers is asserted all 12 input lines are latched, forming 12 bits of trigger data. Subsequent triggers are held off and a prompt signal is issued that can be used in the gating of front end modules. The busy state is maintained until cleared by the ROC. This is done when the ROC has processed all data associated with the current trigger.

The presence of trigger data at the interface module can be communicated to the ROC by means of interrupts or polling.

When in interrupt mode the condition of valid trigger data causes the interface module to generate a VMEbus interrupt. As part of the interrupt service routine the ROC reads the trigger
data register in the interface. The ROC then reads the appropriate front end modules. When this is finished the ROC writes to the trigger data register, enabling new triggers.

When in polling mode the condition of valid trigger data causes the interface module to set a bit in its status register. The ROC is programmed to regularly read this register. When the bit is detected as set the ROC reads the trigger data register in the interface. The ROC then reads the appropriate front end modules. When this is finished the ROC writes to the trigger data register, enabling new triggers.

In addition to the functions described above the interface has some general purpose I/O capability. The module has an 8-bit output port that is always available for use. When the interface is set up in the TS mode of triggering, the 4 external trigger inputs and 8 data level inputs function as a 12-bit input port. The state of these 12 inputs is latched upon a read of the input port register.

Input/Output Signals

Figure 1 identifies the VME Trigger Interface front panel connectors. Connectors A - E mate with 100 ohm impedance twisted pair cable. Tables 1 - 4 identify the signals carried and their pin assignments.

The A,B connector pair is associated with the TS trigger data cable. This cable is designed to link multiple ROCs with the TS in a linear fashion. The A connector (labeled IN) accepts the cable from the TS. The B connector (labeled OUT) is cabled to the next ROC's A connector. This pattern is repeated for the additional ROCs in the chain.

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(TS)       (ROC 0)       (ROC 1)       (ROC 2)       (ROC 3)
|======= A B ======= A B ======= A B ======= A B  ...
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Up to 8 ROCs can be supported on such a link. The last ROC in the chain must properly terminate the signals of the link (see "Configuring The Interface"). The TS drives 4 independent
links for a maximum of 32 ROCs in a system.

The C, D, & E connectors are associated with external triggers and general interface I/O.
Out_0,...,Out_7 are general output signals. *Trigger 0 - 3* are independent external trigger inputs, while *Data_4,...,Data_11* are auxiliary trigger data inputs that are latched on the occurrence of an external trigger. *Level 1 Accept (1) & (2)* are prompt output signals indicating that an external trigger has been accepted. They occur about 10 ns after the leading trigger input signal. These signals remain asserted until the trigger has been acknowledged by the ROC. *Level 1 Accept Pulse (1) & (2)* are pulsed versions of *Level 1 Accept (1) & (2)*, with a common adjustable width (20 - 300 ns). The *Busy* output is asserted while the Interface/ROC is processing a trigger and cannot accept another.

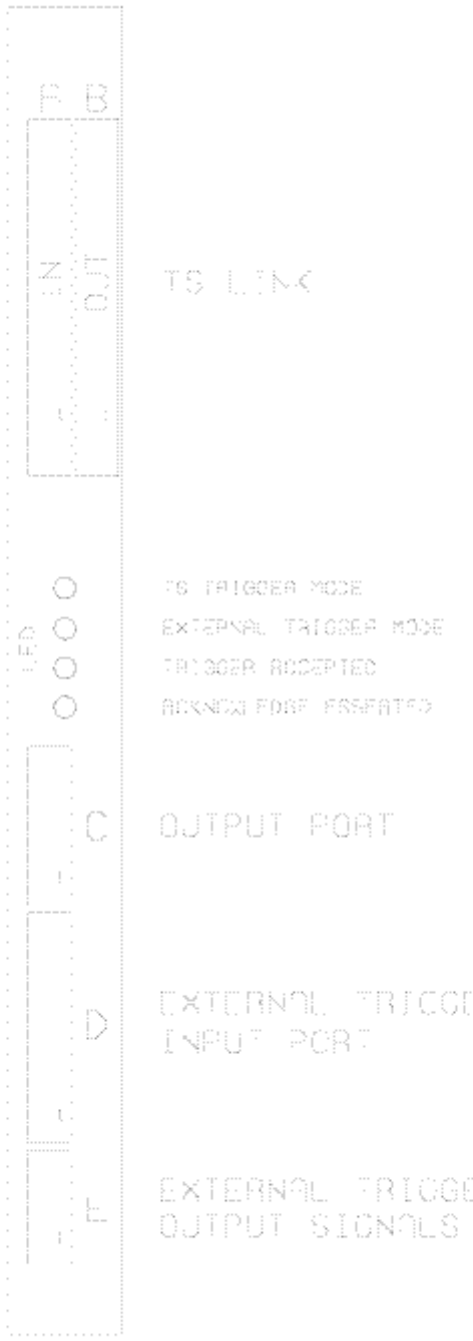

FIGURE 1. VME Trigger Interface front panel.

Table 1. Connectors A & B signal definition

- All signals are differential RS-485

Signal name (Q)	Pin # (Q,/Q)
Strobe	1,2
Sync	3,4
Late Fail	5,6
ROC Code Bit 0	7,8
ROC Code Bit 1	9,10
ROC Code Bit 2	11,12
ROC Code Bit 3	13,14
ROC Code Bit 4 *	15,16
ROC Code Bit 5 *	17,18
ROC 0 Acknowledge	19,20
ROC 1 Acknowledge	21,22
ROC 2 Acknowledge	23,24
ROC 3 Acknowledge	25,26
ROC 4 Acknowledge	27,28
ROC 5 Acknowledge	29,30
ROC 6 Acknowledge	31,32
ROC 7 Acknowledge	33,34

* These lines are not implemented in the current TS - they are included in this module for future expansion.

Table 2. Connector C signal definition - All signals are differential ECL

Signal name (Q)	Direction	Pin # (Q,/Q)
Out 0	Output	1,2
Out 1	Output	3,4
Out 2	Output	5,6
Out 3	Output	7,8
Out 4	Output	9,10
Out 5	Output	11,12
Out 6	Output	13,14
Out 7	Output	15,16

Table 3. Connector D signal definition - All signals are differential ECL

Signal name (Q)	Direction	Pin # (Q,/Q)
Trigger 0	Input	1,2
Trigger 1	Input	3,4
Trigger 2	Input	5,6
Trigger 3	Input	7,8
Data_4	Input	9,10
Data_5	Input	11,12
Data_6	Input	13,14
Data_7	Input	15,16
Data_8	Input	17,18
Data_9	Input	19,20
Data_10	Input	21,22
Data_11	Input	23,24
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Table 4. Connector E signal definition - All signals are differential ECL

Signal name (Q)	Direction	Pin # (Q,/Q)
Level 1 Accept (1)	Output	1,2
Level 1 Accept (2)	Output	3,4
Level 1 Accept Pulse (1)	Output	5,6
Level 1 Accept Pulse (2)	Output	7,8
Busy	Output	9,10

VME Trigger Interface Registers

The VME Trigger Interface is programmed by the user through VMEbus protocols (ANSI/IEEE STD1014-1987). The device meets all VMEbus standards. The VME Trigger Interface is categorized as an A16 - D16 VMEbus slave. All storage locations can be accessed as
both Short Supervisory and Short Non-privileged data. In terms of its interrupt capability the interface is classified as an I(1-7), D08(O), ROAK VMEbus interrupter.

We now describe in detail the registers of the VME Trigger Interface. The local address of each register is given. The base address (A15 - A4) is selected by DIP switches on the board (see
"Configuring The Interface").

1. CONTROL/STATUS REGISTER (CSR) [addr = 0]

The CSR is used to configure the operating conditions of the VME Trigger Interface, as well as provide the current status of the device.

Bits are read/write unless otherwise indicated.

(0) EXTERNAL TRIGGER - setting this bit selects the external trigger mode of operation. In this mode the 4 independent free running user triggers and 8 data levels are recognized by the interface. Clearing this bit selects the TS mode of operation. In this mode trigger data originating from the Trigger Supervisor is recognized by the interface.

(1) ENABLE TRIGGER - setting this bit enables triggers from the selected source to enter the interface and influence its behavior.

(2) ENABLE INTERRUPT - setting this bit allows a trigger accepted by the interface to initiate a VMEbus interrupt.

(3) TEST - setting this bit enables the test interrupt feature of the interface (see Trigger Data Register).

(4) AUTO SAMPLE - setting this bit causes the Input Port Register to be sampled when a TS trigger occurs. This bit has an effect only when the interface is in the TS mode of operation (CSR(0) = 0).

(5) - (6) RESERVED

(7) RESET - (Write only) asserting this bit generates a pulse that clears CSR bits (0)-(4), (15), clears the Interrupt Register, clears the Output Port Register, and clears any latched external trigger.

The following are Read only STATUS bits.

(8) - (10) INTERRUPT LEVEL - binary encoded value of the VMEbus interrupt level LEVEL (0) - (3) that has been selected for the interface by the DIP switches on the module.

(11) - (13) UNUSED - (read as 0)

(14) INTERRUPT PENDING - when set it indicates that the interface has initiated a VMEbus interrupt request and is awaiting acknowledgment from the interrupt handler.

(15) TRIGGER STATUS - when set it indicates that the interface has valid trigger information available in its Trigger Data Register.

2. INTERRUPT REGISTER [addr = 2]

The Interrupt Register is programmed with the 8-bit interrupt ID. During the interrupt acknowledge cycle the reading of this register allows the interrupt handler to identify the VME Trigger Interface as the source of the interrupt request.

All bits are Read/Write.

(0) - (7) INTERRUPT ID

(8) - (15) UNUSED - (read as 1)

3. TRIGGER DATA REGISTER [addr = 4]

The Trigger Data Register contains the trigger information for the event. The contents of the register depends on which trigger mode of the interface has been selected.

Bits of the register are Read only, except where indicated.

(0) - (11) TRIGGER DATA - when in TS mode (CSR(0) = 0) this represents the encoded trigger information generated by the TS (see Trigger Supervisor User Manual for more detailed information).

(0) synchronization flag
(1) late fail flag
(2) - (7) ROC code
(8) - (11) UNUSED (read as 1)

When in external trigger mode (CSR(0) = 1) this represents the latched status of the 4 external trigger inputs and 8 data levels.

(0) - (3) Trigger 0 - Trigger 3 input status
(4) - (11) Data 4 - Data 11 input status

(12) TRIGGER MODE ID - this bit is asserted when in external trigger mode, and cleared when in TS mode.

(13) UNUSED - (read as 1)

(14) TEST INTERRUPT - (Write only) asserting this bit while in TEST mode and with interrupts enabled initiates a VMEbus interrupt.

(15) ACKNOWLEDGE TRIGGER - (Write only) asserting this bit while in TS mode allows the interface to instruct the TS that this ROC has completed the handling of front end data associated with the current trigger.

Asserting this bit while in external trigger mode clears the busy state of the interface, allowing new triggers to be processed by the interface.

4. OUTPUT PORT REGISTER [addr = 6]

The OUTPUT PORT REGISTER allows the user to control the state of the 8 general purpose outputs of the interface.

All bits of the register are Read/Write.

(0) - (7) OUTPUT 0 - OUTPUT 7 levels.

(8) - (15) UNUSED (read as 1)

5. INPUT PORT REGISTER [addr = 8]

The INPUT PORT REGISTER allows the user to sample the state of the 12 external trigger inputs while the interface is configured in the TS mode. If the interface is in external trigger mode, no sampling of inputs occurs (all bits read as 1).

All bits of the register are Read only.

(0) - (3) Trigger 0 - Trigger 3 input status.

(4) - (11) Data 4 - Data 11 input status.

(12) - (15) UNUSED (read as 1)

Configuring The Interface

(a) VMEbus Base Address - this is set using the 12 element DIP switch identified in Figure 2. Switch element 1 is A4, ..., Switch element 12 is A15. An open switch defines a '1'.

(b) VMEbus Interrupt Level - this is set using the 3 element DIP switch identified in Figure 2. The level is binary encoded - Switch element 1 is bit 0, ..., Switch element 3 is bit 2. An open switch defines a '1'. (Note: Default CODA configuration is for interrupt level 5.)

(c) ROC Number - The ROC number is the Acknowledge line (ACK 0 - 7) that the ROC is assigned to on the TS trigger data cable. This assignment must be unique on a cable. The physical location of the ROC along the TS trigger data cable is independent of this logical ROC number.

The ROC number is set using the 8-row x 6-column PIN HEADER array illustrated in Figure 2. The rows are labeled 0 - 7 on the board and correspond to Acknowledge lines 0 - 7. We refer to the columns from left to right as columns 1 - 6. To set ROC number 'N', go to row 'N' and place a jumper that bridges columns 2 - 3, and a jumper that bridges columns 4 - 5. All other rows must have jumpers that bridge columns 1 - 2 and columns 5 - 6.

(d) Trigger Data Cable Termination - the last ROC in the chain must properly electrically terminate the signals of the cable. This is accomplished by inserting the following SIP resistor packs in the last ROC interface module (see Figure 2):

Location	Package	Resistor	Comment
R5	SIP8	100 ohm, isolated	
R6	SIP8	100 ohm, isolated	
R7	SIP8	100 ohm, isolated	
R3	SIP10	180 ohm, bussed	NOTE PIN 1
R4	SIP10	180 ohm, bussed	NOTE PIN 1

(e) External Trigger Inputs - Trigger 0, ..., Trigger 3 can be individually enabled to contribute to the OR of trigger inputs by installing jumpers at locations J0, ..., J3 (see Figure 2). The absence of a jumper means that the input cannot itself trigger the interface. However, the state of such an input will be sampled when this OR signal is asserted. Of course, at least one of the trigger inputs must be enabled to generate the OR signal.

Visual Indicators

4 LEDs visible through the front panel indicate the operating condition and trigger status of the interface (see Figure 1). From top (1) to bottom (4) the LEDs, when lit, convey the following information:

(1) TS trigger mode selected AND triggers enabled.

(2) External trigger mode selected AND triggers enabled.

(3) Trigger accepted by the interface.

(4) Acknowledge asserted by the interface.

2 LEDs on the board indicate the powered status of the interface (see Figure 2). The LED at the top of the board indicates that +5V is present when it is lit. The LED at the bottom of the board indicates that -5.2V (derived from -12V) is present when it is lit. A blown fuse on the board is the most likely cause of either of these LEDs not to be lit. Both fuses have a rating of 3 amps, and their locations are shown in Figure 2.

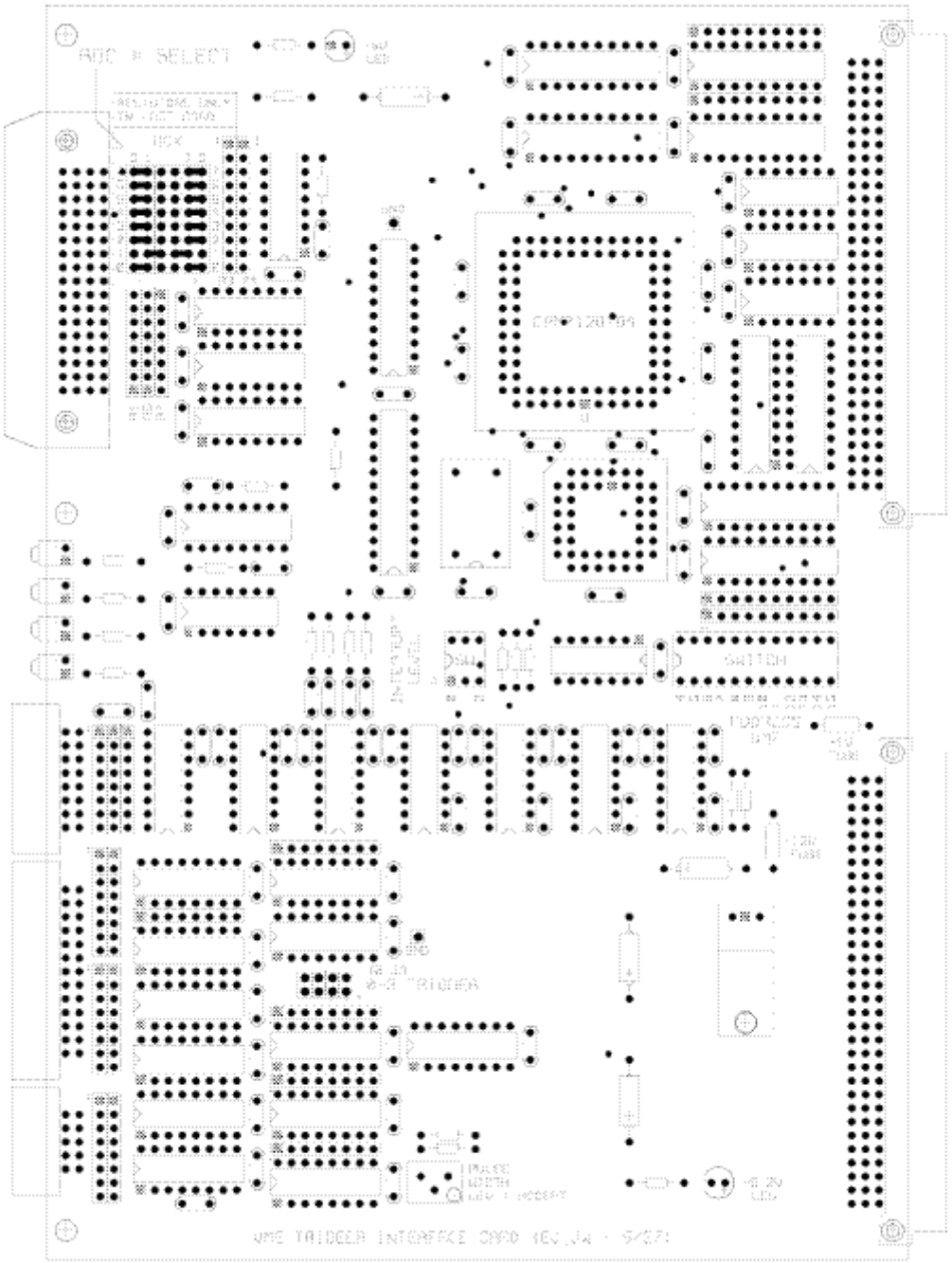

FIGURE 2. Board layout. Shown is jumper setup for ROC #1.