DAQ requirements on the Helicity Decoder

- The module must be a VMEbus module.

- In order that the readout of the Helicity Decoder does not slow down the DAQ the module's data transfer rate over the VME bus must be consistent with standard DAQ modules (200 Mbyte/sec).

- The module must be able to accept consecutive triggers that are separated by 50 ns. The module must therefore have an on-board memory to store event data.

- Rather than reading a single event fragment from all modules when a trigger is received, the DAQ can be configured to wait for a large number (< 255) of event fragments to accumulate in the module memory before readout is initiated. Reading out data in event blocks (e.g. 1 block = 255 event fragments) enhances readout efficiency. To make sure that the on-board memory will not overflow, the module should be able to store 10 maximum size blocks (2550 event fragments). The Decoder reports 20 words (32-bits each) for each trigger, so 51 K words is required. (256 KB = 64 K words is available in the FPGA.)

- The time of arrival of the trigger must be recorded and included in the data for the event. This is done so that the ROC (read out controller) can check that the event fragments it collects from the modules are actually from the same event (i.e. same electron interaction with nucleus). This means that the global system clock (250 MHz) and Sync reset signals must be accepted by the module. We accept the 250 MHz clock and divide it down to 125 MHz using a PLL in the FPGA. The FPGA design is completely synchronous and uses this 125 MHz clock, except for the VME readout that uses a 50 MHz on-board clock. Data generated by the logic is written at 125 MHz into a dual clocked FIFO. Data is read from this FIFO and onto the VMEbus at 50 MHz. The FIFO is the main storage on the module and is instantiated within the FPGA.

- The module must be able to delay the helicity input signals by the trigger latency (T). The trigger comes later in time (by T) than the electron interaction in the target. We want to use and record the states of the helicity signals at the time of the interaction, not at the time of the trigger's arrival to the module.

Clock, *sync_reset*, and *trigger* signals for the Helicity Decoder

The current data acquisition system at JLab is a synchronous design. *Clock*, *sync_reset*, and *trigger* signals are sourced by the Trigger Supervisor (TS) and are distributed to Trigger Interface (TI) modules located in the VME or VXS front end readout crates (one TI per crate). For a VXS readout crate the 3 signals are distributed from the TI to the readout modules through the VXS fabric that is appended to the VME backplane. A P0 connector on each module connects to the VXS fabric.

Connector PO is located between the standard VME P1 and P2 connectors. For a standard VME readout crate the signals are instead distributed from the TI to the modules through front panel connectors. This is facilitated with an auxiliary front panel distribution module when multiple readout modules are present. A single readout module may be directly connected to the TI by front panel.

Time in clock periods is kept locally in each readout module. Time across the system is synchronized (set to 0) by the *sync_reset* signal sent at the beginning of a run. For each *trigger* received a module time stamps its associated data. In this way the event fragments from the distributed readout system can be reliably combined into a complete event.

A 250 MHz *clock* is distributed from the TS to TI in the JLab system. The TI can distribute this 250 MHz clock or a divided one (125 MHz, 62.5 MHz, 31.25 MHz) to the modules in its crate. Hall D uses modules clocked at 250 MHz (Flash ADC250), 125 MHz (Flash ADC125), and 31.25 MHz (F1 TDC). The Flash ADC250 is used in every hall, so it is natural to design the Helicity Decoder to accept the 250 MHz clock.

For maximum flexibility we design the Helicity Decoder to accept *clock*, *sync_reset*, and *trigger* signals by both P0 and front panel connections. The front panel connector type and signal levels will match that of the Flash ADC250 so that that same auxiliary front panel distribution module can support Flash ADC250s and the Helicity Decoder in the same VME crate. In case the Helicity Decoder is in a VME crate with no Flash ADC250 modules, there will be a 2nd front panel connector with type and signal levels that allow a direct connect to the TI. For true stand-alone operation, the Helicity Decoder will have an internal 250 MHz clock that can be selected.

An associated document (*Clock Sync Trig for Helicity Decoder.pdf*) shows the functional circuitry necessary to support the options described above. Note that single lines in the drawings represent differential signal pairs with the labelled levels (NECL, LVPECL, LVDS). Proper termination and biasing for these high-speed signals is required and will be discussed later. Appropriate ICs to implement the circuitry are identified. IC packages with leads (not pads) should be selected when possible to ease in assembly and repair.