Nuclear Physics Division

Fast Electronics Group

Description and Technical Information for the VME LED Driver (VLD) Module

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Table of Contents

1 Introduction

The VME LED Driver (VLD) module is being designed for the scintillator calibration and bleaching of the NPS experiment in Jefferson Lab HallC [1]. The VLD boards are located in the VME crate in the radiation-shielded hut in the experimental hall. The VLD drives blue LEDs on the HV-LED board mounted on the back of the scintillator detector through ribbon cables totaling about 50 (max) meters in length. Figure1 shows the crate level diagram of VLD boards in the experiment.

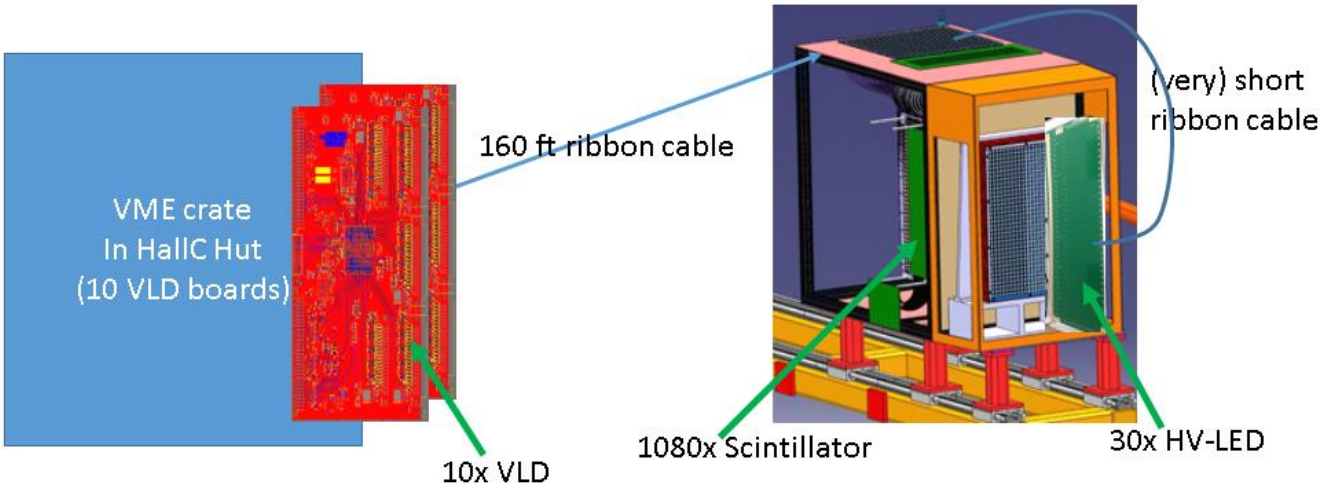


Figure 1 The VLD boards location and cables to 'power' the LEDs

The VLD design will be based on the TI/TD [2] design for the VME interface with the ability of updating the firmware remotely, and uses the same FPGA (Xilinx Artix-7) as the VETROC [3] board for inexpensive and flexible control.

The blue LEDs (NSPB500AS by NICHIA) [4] are mounted on the HV-LED board on the back of the crystals (scintillators), and coupled with a quartz optic fiber to the back of each of the 1080 crystals of NPS detector. The Cathode of the LED is tied to the common ground, which simplifies the VLD design greatly (comparing with the initial assumption that the Anodes were tied to the common ground. The LED Anode is connected to the VLD output through several sections of the ribbon cables (and the PCB traces), totaling about 50 meters.

There are two working modes for the LED driver: the calibration mode, and the bleaching mode. In calibration mode, the LED can be powered up individually with an adjustable current of up to 110mA and pulse rising time of several ns, and the pulse width adjustable (~10ns to ~us) to simulate a real scintillator signal.

In the bleaching mode, (to bleach off the scintillator radiation damage), all the channels can be powered up for up to several days (continuously) with the bleaching current of up to 35 mA per channel. The bleaching can be powered up in groups of 36-channels (36-channels share one LDO regulator).

Here are the requirements documented by Carlos Munoz Camacho [4]:

> *The calibration and optical bleaching of the NPS crystal imply the following requirements to the LED control system:*
>
> *_ Operate each LED both in continuous and pulsed mode.*
>
> *_ Be able to light up one single LED individually (in addition to 'all at once'), for both the continuous and pulsed modes.*
>
> *_ Be able to cycle all the channels, lighting up one LED at a time (in pulsed mode).*

_ Be able to trigger the DAQ on the pulsed mode operation.

_ The system should have 'trigger/clock' NIM input in order to set the flash rate for enabled LEDs.

In continuous mode (for optical bleaching of the crystals) LEDs will need to be on for several hours (up to 48{72 hours).

Here are the additional (clarifying) requirements documented by Brad Sawatzky [5]:

1. Bleaching Mode: The LEDs will need to operate in two modes at 35 mA continuously for 48–72 hours during bleaching mode.

2. Pulse Mode: The LED pulses should be comparable in amplitude and timing to real pulses produced in the NPS crystal. Rise times on the order of a few nanoseconds, a pulse width on the order of 10–40 ns. Pulse amplitude is unclear (will depend strongly on the optical coupling of the LED → Fiber → crystal.

◦ It is not clear what level of granular control is desired over individual amplitude and pulse widths.

◦ It is not clear whether remote/programmable control of these pulse parameters is a "like" or a "must".

3. Clarification for circuit drawing on p. 25:

◦ J1-1 and P1-1 are tied together and supply power to LED_0

◦ J1-2 and P1-2 are the nominal common return for LED_0 ie. are tied to the common ground plane)

◦ J1-3 and P1-3 are tied together and supply power to LED_1

◦ J1-4 and P1-4 are the nominal common return for LED_1 (ie. are tied to the common ground plane)

4. ~~It is the anode (positive) pins on the LED that are tied to the common ground.~~

** (4): it is confirmed by the HV distribution PCB design that the LED cathodes are tied to common ground.*

5. The ground of the LED boards are presently tied to the frame through screws (chassis ground). I have some concerns this will produce ground-bounce noise in adjacent PMTs that may be hard

In summary, there are totally 1080 channels (1080 LEDs distributed on 30 HV-LED boards with 36 per board). The total bleaching current is about 40 A continuous. There will be 10 VLD boards, with 108 channels each to cover all the 1080 LEDs (crystals).

The actual cost is about $33K (added up all the related PRs). Twelve production boards were produced. One prototype was produced (can be salvaged for spare parts).

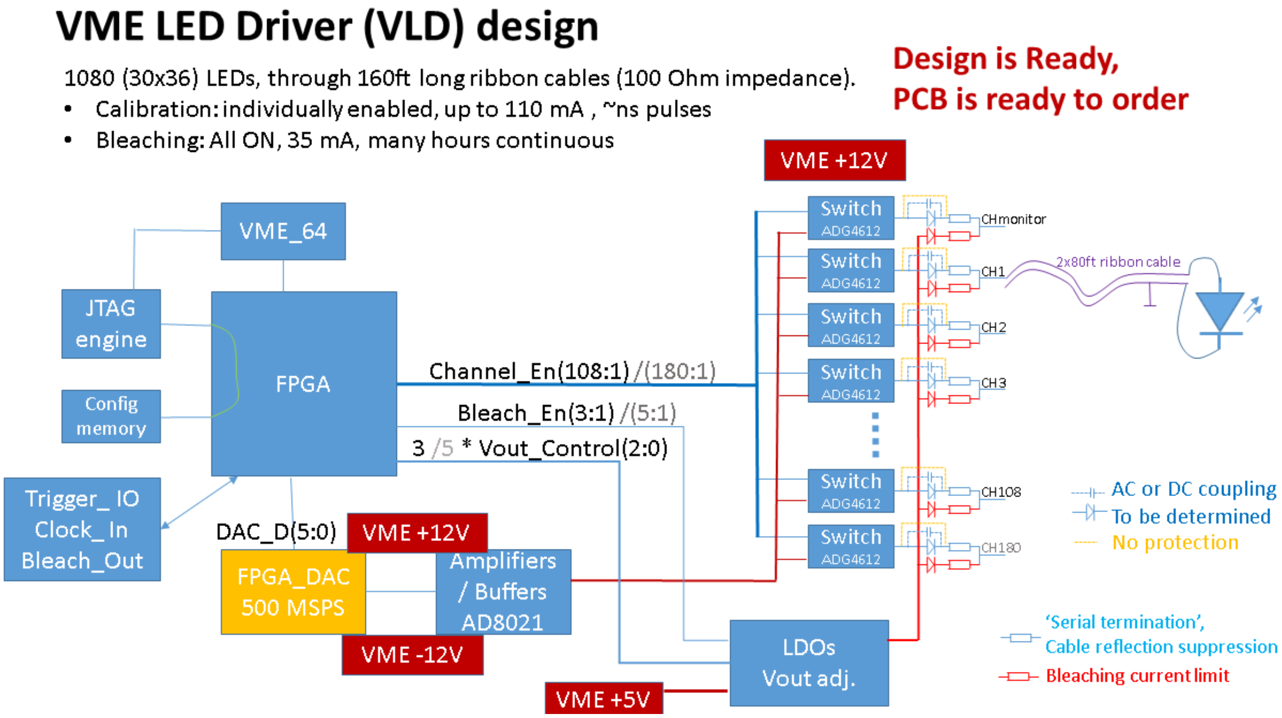
The additional components for the LED driver system include a VME crate, a CPU/VME_controller, and many ribbon cables. These additional components are not included in this document.

2 Purpose of the VLD module

The VLD board is loaded in the VME crate in the radiation-shielded hut in hall C as a VME slave board. Each VLD board drives 108 LEDs through the front panel connectors, and the attached long ribbon cables. The VLD can also accept external trigger signals, and initiate calibration pulses, or preprogrammed calibration sequences. The VLD can also generate DAQ readout trigger initiated by the LED calibration pulses.

The VLD can pulse any of the 108 channels with a programmable pulse (height and width). The VLD can also supply up to 35 mA continuous current to each LED, totaling about 4 A per VLD.

The VLD can work on its onboard oscillator clock, or the NIM input clock (to synchronize to a common clock). It can generate triggers when pulsing the LEDs, and it can also pulse the LEDs on the external trigger inputs. Figure 2 is a functional diagram of the VLD board.



VME LED Driver (VLD) design

1080 (30x36) LEDs, through 160ft long ribbon cables (100 Ohm impedance).

- Calibration: individually enabled, up to 110 mA , ~ns pulses
- Bleaching: All ON, 35 mA, many hours continuous

Design is Ready,
PCB is ready to order

Figure 2 Functional diagram of VME LED Driver (VLD) board

To use the FPGA (xc7a200t-ffg1156) resources and the VLD PCB physical resources fully, two on-board connectors for additional 72 channels LED drivers are implemented. This expands the 108 channels to 180 channels. To connect these 72 channels, the same cable can be used, but the cable has to go through the front panel opening. These two connectors are not expected to be used.

3 Functional Descriptions

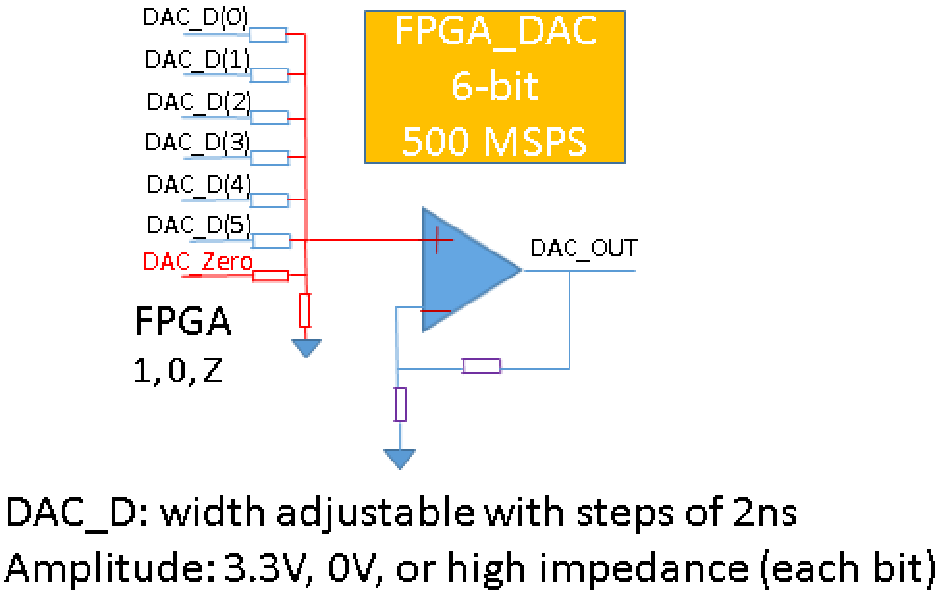
3.1 General description

Figure 2 shows the block diagram of the VLD board, indicating the major components used in the design. The Xilinx XC7A200T is chosen for the controlling logic and VME interface, which has abundant resources, is less expensive, is LVTTL33 I/O compatible, and has been proven in the VETROC project.

3.2 Pulse shape generation (current/amplitude, and pulse width control):

The calibration pulse is generated by a FPGA digitally controlled "DAC" working at 500 MSPS, followed by op-amps. The user can load the pulse shape into a memory in the FPGA.

Figure 3 shows the FPGA controlled DAC with an amplifier. The DAC (op-amp) output is further amplified/buffered per cables (36 LED channels). The buffered signals drive the LEDs through analog switches, which are used to disable/enable individual LEDs.



DAC_D: width adjustable with steps of 2ns
Amplitude: 3.3V, 0V, or high impedance (each bit)

Figure 3: FPGA DAC design

As shown in Figure 3, the DAC_Zero is used to set the base level for the LED positive conduction voltage, typically 3V for the blue LED. The DAC_D[5:0] is used to set the pulse shape, hence the current through the resistor and the LED. The correlation between the LED light output and the DAC_D[5:0] setting is to be determined by the actual detector implementation. A sequence (hundreds/thousands) of DAC_D[5:0] is clocked out from the FPGA at the speed of 500 MS/s to get the proper calibration pulses.

3.3 Pulse (pulse mode) coupling to the ribbon cable:

Each channel is controlled by an analog switch, so that the calibration can be turned ON/OFF individually. Every 36 channels (one connector) share one pair of op-amps, which are connected in parallel to supply the needed current and maintain a faster rising time.

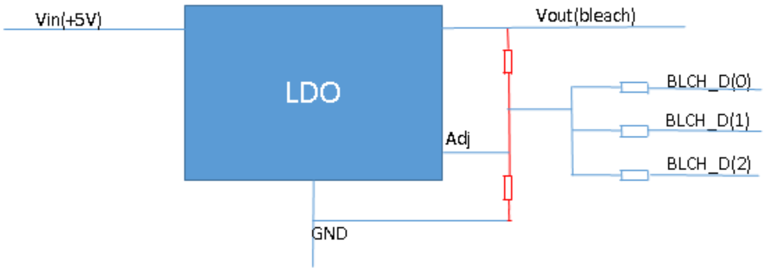
Two methods of coupling are being considered: AC and DC. In AC coupling, the pulse is coupled through a (0.1 uF) capacitor (for a <1 us pulse) to the current limiting resistor and the cable. In AC coupling mode, the voltage shift can be applied at the cable side of the capacitor. The disadvantage of the AC coupling is that the AC coupling would not work for crystal bleaching (almost DC current).

In DC coupling, a high speed diode may be used to isolate from the bleaching mode driving circuit. A direct connection should be OK, if the bleaching circuit is diode isolated. If the diode is used for DC coupling, there will be an extra (~ 1V) dropout on the diode, and the voltage shift (for LED forward voltage) has to come from the amplifier too. This requires the op-amp output to have a larger swing, hence the diode coupling is not favorable.

The DC coupling is chosen. A 20 Ohm serial resistor is used to ‘back terminate’ the calibration pulse. The bleaching is driven through an isolation diode and a 30 Ohm current limiting resistor.

3.4: Bleaching mode:

The bleaching current is supplied by an adjustable LDO powered by +5V from the VME connector. The LDO output can be fine tuned by the FPGA digitally as shown in figure 3 by driving the ADJ pin of the voltage regulator. The Vout drives all the 36 channels (per connector) with an isolation diode and a current limiting resistor (30 Ohm) per channel. Each LDO can be disabled independently by setting the regulator’s ENABLE pin.



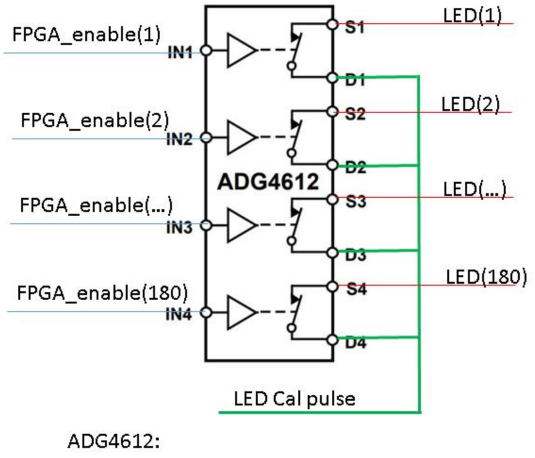
BLCH_D: Add current to R2 (hence requires less current from R1, and lower Vout) when high (+3.3V)
Drain current from R1 (hence requires more current from R1, and higher Vout)

Figure 4 Bleaching voltage/current control

Each connector has its own bleaching current control. By setting the BLCH_D(2:0), the voltage regulator out Vout can be adjusted, hence the bleaching current over the current limiting resistors and LEDs. The BLCH_D(2:0) is set by the VME registers. The correlation between the BLCH_D(2:0) setting and the bleaching current has been measured by the first VLD board. Refer to the VLD test document[6] for details.

3.5: Channel enables:

For pulse mode: each channel can be enabled/disabled independently, and the channel enable/disable can be programmed to cycle through a certain sequence. When more than one channel are enabled, the enabled channels will have the same (amplitude and shape) pulse (calibration signals). The enabling/disabling is controlled by the analog switch, conduct or isolate.



Power-off protection

Switch guaranteed off with no power supplies present

Inputs are high impedance with no power

Switch turns off when input > V_{DD} + V_T

Overvoltage protection up to 16 V

PSS robust

Negative signal capability passes signals down to −5.5 V

6.1 Ω maximum on resistance

1.4 Ω on-resistance flatness

±3 V to ±5.5 V dual supply

3 V to 12 V single supply

3 V logic compatible inputs

Rail-to-rail operation

16-lead TSSOP and 16-lead 3 mm × 3 mm LFCSP

Figure 5: ADG4612, analog switch functional diagram

For bleaching mode, each connector (36 channels) can be enabled/disabled independently by enabling/disabling the LDO regulator directly.

The analog switch ENABLE can also be used to generate the calibration pulse with a faster rising edge.

3.6: LEMO Input and Output

The LEMO inputs (of the trigger and clock) are received by a TI SN65LVDS348 any-level-differential receiver powered by +3.3V, and the output (LVTTL) is connected to the FPGA directly. The clock input is connected to an FPGA clock capable pin. The differential receiver Vref can be adjusted to -1.2V, -0.4V, +1.2V by a three position switch for ECL, NIM, and (LV)TTL respectively. The LEMO inputs (single ended signal) are terminated (50 Ohm to ground) on the VLD board. Here is the diagram of the receiver (the 10K resistor is actually 50 Ohm):

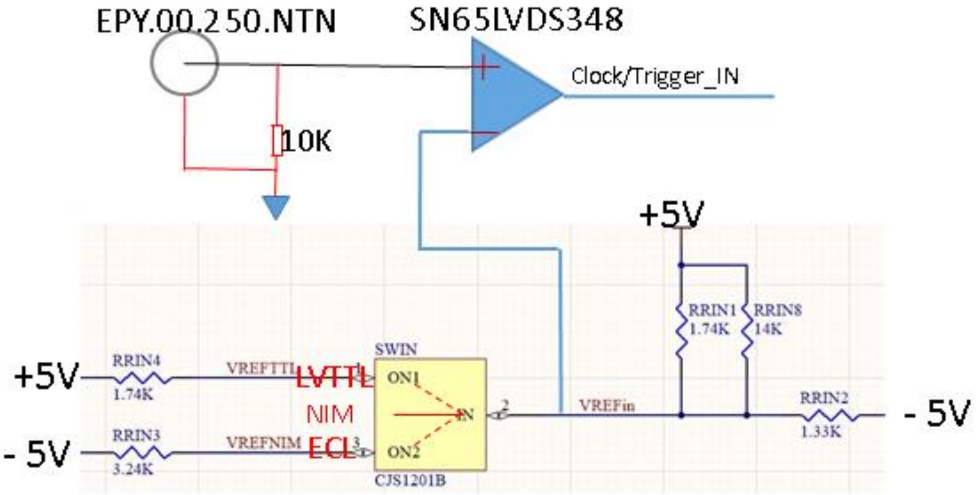


Figure 6 LEMO input diagram

The TRIGGER output from the FPGA is driven to the LEMO connector (NIM level). The active BLEACHING signal from the FPGA is also driven to the LEMO connector (NIM level), and can be used to safety lock the HV supply. The RF04 (14K) resistor in the schematic is actually populated as a 0.22uF capacitor to improve the NIM output rising edge and falling edge.

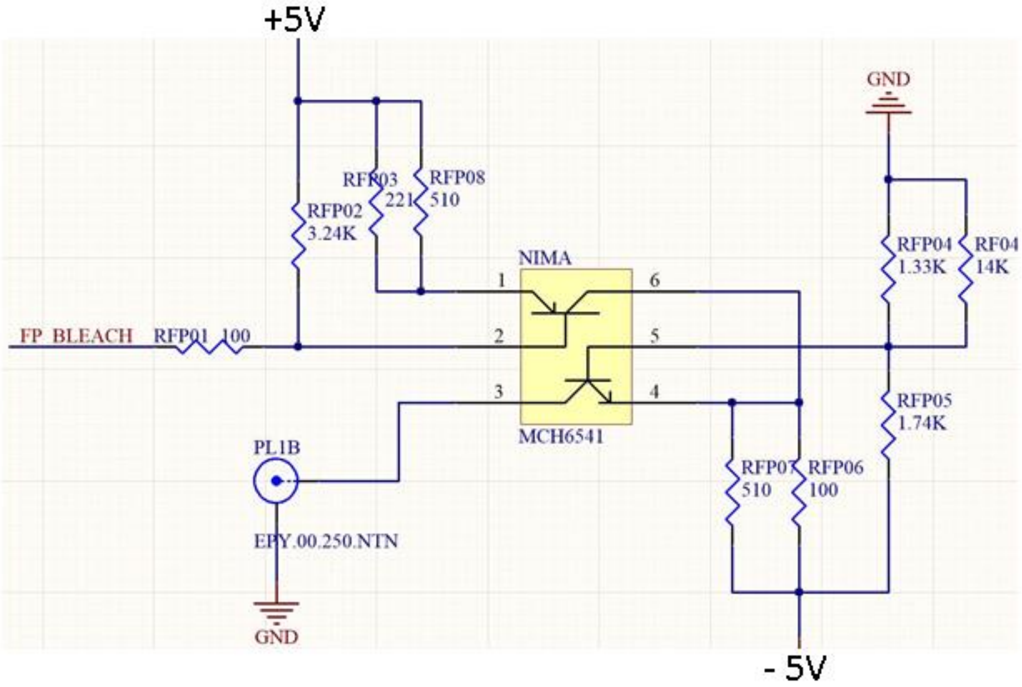
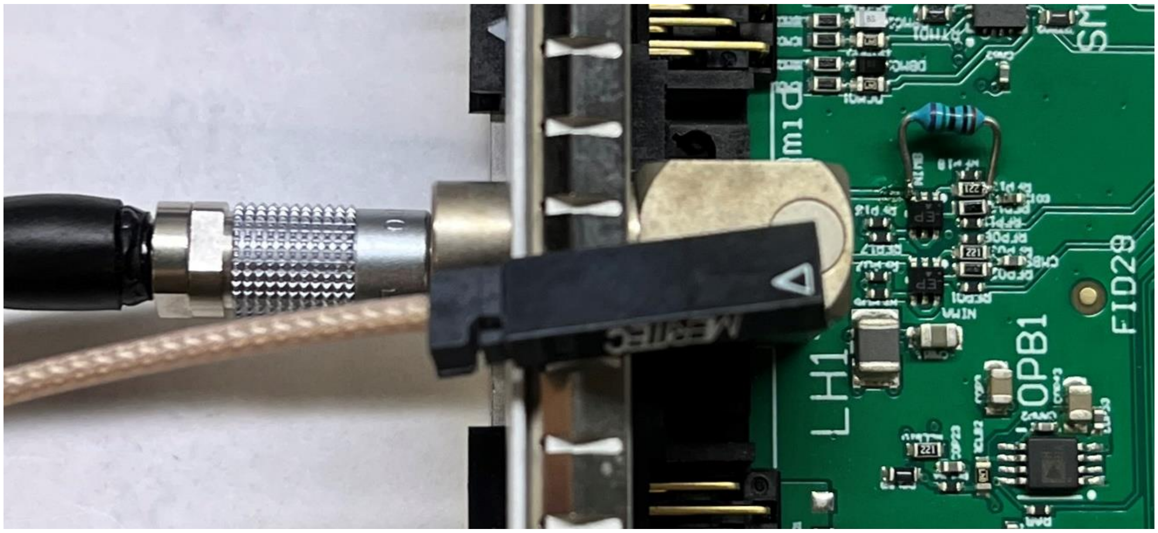


Figure 7 LEMO driver circuit

On VLD board#02, the FP_TrgOut driving circuit was modified to a psudo_differential signal, which is acceptable by a newer TI modules (with QSFP optic transceivers) as trigger inputs.



The FP_TrgOut modifications: A 750 Ω resistor is added between NIMB pin#3 and V+5. The LEMO output should be connected to the TI front panel input's Negative leg, and the LEMO ground should be connected to the TI front panel input's Positive leg (the white triangle mark in this cable). A 100 Ω differential cable (not the coax cable in the picture) is preferred.

From firmware V3.4, the VLD can "OR" the front panel TRIGGER input (Top_Left, NIM) with its on-board trigger, and outputs to the front panel trigger output (Bottom_Left). The LVD can also "OR" the front panel BLEACH input (Top_Right, NIM) with its on-board BLEACH, and outputs to the front panel Bleach output (Bottom_Right). The "OR" logic can be disabled by the software (section 6.2 of this manual reg 0x20, bit#15:14).

3.7 VME interface

The VLD board is a VME slave board. It is compatible with VME64x backplane, and the payload slots in the VXS crate. Normally, it is a VME slave board, with interrupt capability.

For simplicity, two kinds of VME address modifier codes are implemented. (1), User defined address modifier (0x19, 0x1A, 0x1C and 0x1D). This is similar to the A24 address modifier. It is used to load the FPGA programming memory by the 'emergency VME to JTAG engine' logic. (2), Standard A24 address modifier. This is used to set or readout the registers on the FPGA, slow controls of the VLD peripherals. This is implemented the same way as VETROC, except that there is no need to generate DAQ data for the VLD board.

3.8: FPGA programming/PROM loading

The FPGA XC7A200T needs about 80Mbit flash memory to configure. This configure data is saved in the Micron MT25QL256A (N25Q256 for VETROC, but this flash memory is discontinued), which is 256 Mbit.

The FPGA is programmed in Master SPI mode with external clock of 50 MHz and 4-bit wide data loading (SPIx4). The expected FPGA program time is less than one second. The Micron flash memory can be loaded by the Xilinx iMPACT software through the on-board JTAG connector. The iMPACT software will load a special firmware to the FPGA through the JTAG connector and program the memory through the special firmware, which Xilinx calls it the indirect flash memory programming.

The FPGA and the Flash memory can be remotely loaded (through VME). To make it more robust for remote programming, a hardware (discrete logic) VME to JTAG engine is implemented on the board (copied from TS/TI/TD design) using the custom defined address modifier code (AM = 19), which will not get confused with the standard (VME specified) A24 address modifier codes. This engine can load the FPGA firmware even if the memory is corrupted (or simply, the memory is empty) or the FPGA failed to be loaded by the flash memory. The JTAG engine has been tested successfully on the VETROC. It takes about 30 seconds to load the FPGA through VME. It takes about ten minutes to load (program) the Flash memory (Micron N25Q256). In this JTAG engine, the VME data bit[1] is used for TDI, bit[0] is used for TMS, and all the other bits are unused. The higher 5 bits of A24 address (A[23:19]) should match with the geographic address, and the lower A24 address (A[18:0]) is set to be 0x0FFFC. When the VLD is plugged into a standard VME64 crate, (no geographic address for slots), the on-board switch is used to set the 'geographic address'.

For more flexibility, two Micron flash memories are loaded on the board, and the flash memory is selected by a hardware switch just like that of the VETROC board. Two independent firmware designs can be loaded for the same piece of hardware (PCB).

3.9 Other functions

The VLD has several on board LEDs to indicate the VLD status.

4. Specification Sheet

4.1 Mechanical

- Single width, 6Ux160mm VME64x slave module. It is compatible with the VXS payload slots, and standard VME64 crate slots (except slot#1).

4.2 Front panel inputs and outputs:

- LEMO: Upto 250MHz CLOCK Input, with hardware switch settable Vref for ECL, NIM, and TTL levels;

- LEMO: TRIGGER Input with hardware switch settable Vref for ECL, NIM, and TTL levels;
- LEMO: TRIGGER with adjustable width NIM level output;
- LEMO: BLEACH active NIM level output;
- 3M P50E-080: 108 channels (on three connectors) LED driver Outputs

4.3 LED Indicators:

On-board, needs light-guide to show on the Front Panel:

- Bit 1 (top): FPGA programmed and the clock (DCM locked) is ready;
- Bit 2: VME DTACK, VME activity;
- Bit 3: Trigger is active (either external input, or FPGA generated);
- Bit 4: flashing: Calibration pulse active, ON: bleaching active.

On board:

- Power OK near each regulator or DC-DC converter (LED is OFF when the power is OK);
- FPGA program DONE (LED is OFF when the FPGA is programmed);

4.4 Programming:

- VME to JTAG A24D32 with user defined AM (Address Modifier) for remote loading with redundant On board JTAG connector;
- Two flash memories can save two independent firmware simultaneously.

4.5 Power requirements:

- +5v @ 6 Amps; -12V @ 1 Amps; +12V @ 1 Amps (from VME P1 Backplane connector), all are fused.
- DC-DC converters for +3.3V (from +5V), +2.5V/3.3V, +1.2V, +1.0V, and LDO for +1.8V FPGA BRAM and +1.0V FPGA MGT power.
- LDO regulators for LED bleaching.

4.6 Environment:

- Forced air cooling: VME 6U crate standard
- Commercial grade (minimum) components (0-75 Celsius)

Figure 6 shows a typical populated VLD board:

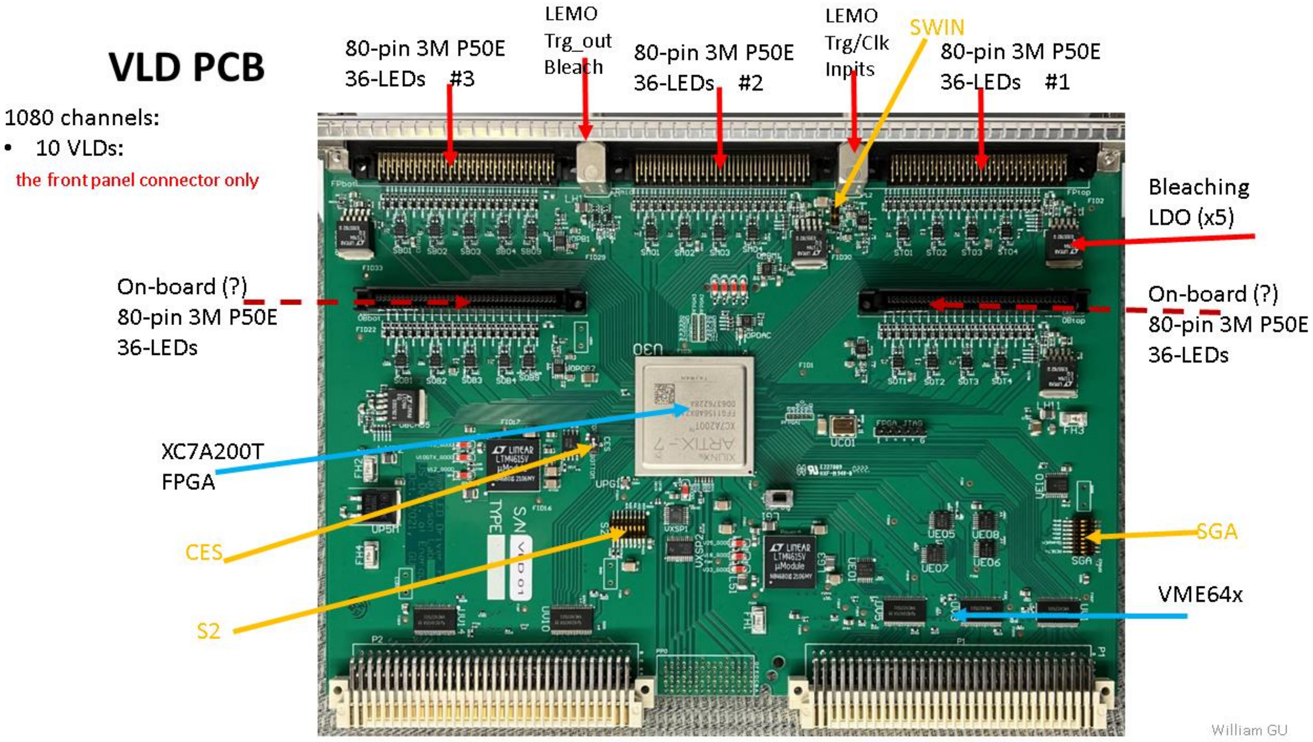


Figure 8: The VLD board (using the PCB layout as a placeholder)

5 VLD operation procedures:

The VLD needs to be properly set, and to be plugged into the proper crate and slot. Damage may happen to the VLD, the crate, or other PCBs in the crate if the right procedure is not followed.

5.1 VLD Power supply:

The VLD uses +5V, +12V, and -12V from the VME P1 connector, generates +3.3V, +2.5V, +1.8V, +1.2V and +1.0V by the onboard DC-DC regulators or LDO regulators, and generates adjustable bleaching current (voltage) outputs by five LDO regulators.

5.2 Hardware setting (Switch etc., the orange colored marking):

CES: Reserved for VLD firmware developer

This is a one-bit, three-position switch used to select the flash memory to load the FPGA. The VLD FPGA can be loaded by two independent flash memories with SPIx4 interface. The switch CES needs be set to the right flash memory. When the three position switch is set in the middle, no flash memory is selected, hence the FPGA will not be programmed. This is switch is reserved for VLD firmware developer.

SGA: Reserved for VLD board installer

This is an 8-bit ON/OFF switch with pull up resistors (to +3.3V, so OFF = High, ON = Low).

- Bit[1:5]= GA_N(4:0) if the VLD is plugged into a standard VME/VME64 crate (without Geographic address). These five bits should be set to high (OFF) if the VLD is plugged into a VME64x (or VXS) crate. This address is used in VME emergency JTAG engine (flash memory loading). It is suggested to be set as the same as the slot number of the VME64 crate.

Example: for slot#5, Bit[1:5] should be set to OFF, OFF, ON, OFF, ON. (Geographic address is polarity inverted per VME64x standard, 11010 for slot#5).

- Bit[6:7]: not used;
- Bit[8]: FPGA re-loading, connected to FPGA's PROGRAM# pin. Keep it OFF normally.

S2: Reserved for VLD installer

This is an 8-bit ON/OFF switch with pull up resistors (to +3.3V, so OFF = High, ON = Low).

- Bit[1:5]=A[23:19], VME address space in A24 mode. When the VLD is in a VME64x compatible crate, these bit settings do not matter, and the geographic address is used to match with A[23:19]. When the VLD is in a standard VME crate, the Bit[1:5] is usually set to its location in the VME crate (less confusing when addressing the VLD) to match with A[23:19] for VME address space. Like the Bit[1:5] of switch SGA, it suggested to be set as the slot number of the VME crate.
  Example: for slot#5, Bit[1:5] should be set to ON, ON, OFF, ON, OFF, or 00101.
- Bit[6:7]: to be determined
- Bit[8]: Clock source selection: 0: to select the on-board oscillator, 1: to select the external NIM input, this setting can be over-written by the software (register 0x2C).

SWIN: Reserved for system installer

This is a 1-bit three-position switch used to set the Vref for the LEMO signal receiver.

- Set to Middle, the Vref is ~ -0.4V, for NIM level input;
- Set to left, the Vref is ~ +1.5V, for TTL level input;
- Set to right, the Vref is ~ -1.2V, for ECL level input.

5.3 Software setting:

The VLD is powered up to a default low-power (inactive) state. All the calibration pulses are disabled, and the bleaching is disabled too. No user interference is required if the user does not want to power up the LEDs on the detector. The software should implement an register reset after the calibration/bleaching has been finished.

Here are some example procedures to power up the LEDs.

5.3.1 Scintillator calibration initiated by the internal command:

- Load the pulse shape (to the FPGA memory) if the default pulse shape is not the right one, by write to VME address 0x6C repeatedly;
- Load the channel enable pattern (bits(18:0) of VME_registers 0x40, 0x44, 0x48, 0x4C, 0x50, 0x54, 0x58, 0x5C, 0x60, and 0x64); (bit0 should be the OR of the 18 channels bit(18:1))
- Load the 'trigger' source enable register (0x20) to use internal pulsing;
- Load the number of pulses and period (address 0x8C), or load the random pulsing period (0x88)

5.3.2 Scintillator calibration initiated by the external trigger:

- Load the pulse shape (to the FPGA memory) if the default pulse shape is not the right one, by write to VME address 0x6C repeatedly;
- Load the channel enable pattern (bits(18:0) of VME_registers 0x40, 0x44, 0x48, 0x4C, 0x50, 0x54, 0x58, 0x5C, 0x60, and 0x64);
- Load the 'trigger' source enable register (0x20) to use external pulsing;
- Enable the external pulsing (this operation is NOT on the VLD)

5.3.3 Scintillator calibration initiated by the internal sequence (*to request more inputs from user*):

To speed up the calibration, the channels can be cycled through automatically by enabling the internal calibration sequence. This process can easily be implemented in the software, by looping over channel enable registers.

- Load the pulse shape (to the FPGA memory) if the default pulse shape is not the right one, by write to VME address 0x6C repeatedly;
- Load the ‘trigger’ source enable register (0x20) to use automatic cycling through;
- Load the number of pulses per channel and period (address 0x8C).

5.3.4 Scintillator bleaching (all channels):

- Load the bleaching time (register address 0x68);
- Load the bleaching LDO regulator enable and the bleaching current setting (by adjusting the LDO output voltage) of vme_registers (addresses) 0x40, 0x48, 0x50, 0x58, and 0x60) for blocks of 36 channels. The bit0 of these registers need to be 0 to disable the firmware lock of bleaching (by disabling the calibration pulses and disabling the analog switch, which has higher priority).

5.3.5 Scintillator bleaching (single channels):

The scintillators can also be bleached by the calibration pulsing when a specific scintillator bleaching is required, though this procedure may never be required. To do this,

- Load the Calibration pulse to the memory with the desired value for the bleaching current required (register address 0x6C);
- Enable the proper channel(s), by writing to bits(18:0) of registers 0x40, 0x44, …, 0x64.
- The op-amp can supply up to 200 mA bleaching current.
- The readout may need to be masked off to reduce the ‘noise’, but this is not by VLD.
- To disable the bleaching, simply disable the channels by writing to bits(18:0) of registers 0x40, 0x44, …, 0x64.

5.3.6 Faster calibration signal generation:

The calibration pulse from the op-amp has a slope of about 1V/6ns, which could be too slow for some applications. There are two tricks to get a faster light output:

Trick#1: Set the calibration pulse base voltage to ~3V, which is just below the blue LED threshold. Any pulse above this voltage will light up the LED. The voltage swing on the cable is small, which means smaller noise.

Trick#2: Set the analog switch enable/disable. This ENABLE timing (the delay from the trigger, and the width) can be set by the register 0x74. The analog switch ENABLE can generate a rising edge of ~5ns, even for >8V calibration pulse. The cable will be pretty noisy.

- Do the same procedure as 5.3.1 for LED calibration.
- Set the analog switch enable timing register 0x74.

6. VME Programming Requirements (This part will be updated as the firmware develops)

There are two categories of Address Modifier codes supported on the VLD: the user-defined codes (A24) for emergency firmware loading; and the standard A24 for FPGA register read/write. (The slow controls, JTAG engine and I2C engine, can be implemented if needed).

6.1 VME to JTAG (flash memory) emergency loading engine:

The AM[5:0] user defined codes are used for this logic. This works even before the FPGA is programmed and working. It is almost the same as A24D32 mode. The valid AM codes are: 0x19, 0x1A, 0x1D and 0x1E. These AM codes are user defined, and similar to the AM codes 0x39, 0x3A, 0x3D and 0x3E.

The valid address bits are A[31:24] do not care; A[23:19]=GA[4:0] for VME64x crates, or A[23:19]= Bit[1:5] of SGA switch for non-VME64x crates; A[18:2]=b’00011111111111111.

Data bit[1] is TDI; data bit[0] is TMS.

For example, if the board is in slot#5 (that is ~GA(4:0)= 11010), you need write to A(23:0)=0x28fffc. If data(1:0)=00, both TMS and TDI will be low; if data(1:0)=01, TMS is high, TDI is low; if data(1:0)=10, TMS is low, TDI is high; if data(1:0)=11, both TDI and TMS are high. The normal A24 address should try to avoid this address (0x0fffc). The TCK is one cycle (low→ High → low) on every VME write cycle.

A more advanced example: Instruction register shift (8-bit, shift in 0x5a) starting from/end up at the 'reset idle' JTAG state: 14 consecutive writes to the address 0x28fffc with AM=0x19, 1a, 1d or 1e, the data are 1, 1, 0, 0, 0, 2, 0, 2, 2, 0, 2, 1, 1, 0 respectively.

Data	1	1	0	0	0	2	0	2	2	0	2	1	1	0
TMS	H	H	L	L	L	L	L	L	L	L	L	H	H	L
TDI	0x	0x	0x	0x	0	1	0	1	1	0	1	0	0x	0x

- "TMS H" means logic High, "TMS L" means logic Low, "TDI 0" means 0 or Low, "TDI 1" means 1 or High, and "TDI 0x" means DO NOT CARE by the JTAG, but the set value is 0.

6.2 Configuration Registers:

A24D32 are used for register read/write. Similar to the emergency loading logic, the base address is determined by the Geographic Address in VME64x/VXS crate, and external switch for non-VME64x crate. That is, A[23:19]=GA[4:0], or S2[1:5].

➢ Address offset: 0x00000: Board ID:

Bit 7-0 (R/W): Crate ID; Reset default 0x00;
Bit 12-8 (R): A24 address, higher 5 bits; Reset default 000
Bit 13 (R): VME Crate info, 1: VME64x compatible, 0: standard VME;
Bit 15-14 (R): reserved;
Bit 23-16 (R): PCB related setting, 0x01: production board, 0x00; prototype board;
Bit 31-24 (R): Board type: 0x1D: vme Led Driver (VLD) board.

➢ Address offset: 0x0000C: Trigger delay and Pulse width:

Bit 7-0 (R/W): Trigger delay, 1024*Bit7 + (Bit(6:0)+1) * 4 * (4**Bit7) ns; Reset default 0x00; That is when bit#7 = 0, the delay is "bit(6:0)+1" in steps of 4ns; when bit#7 =1, the delay is "bit(6:0) + 64" in steps of 16ns. The minimum delay for bit7=1 is about 1 us, the maximum delay is about 3 us.
Bit 12-8 (R/W): Trigger Pulse width (n+1)*4 ns; Reset default 0x07;

➢ Address offset: 0x0020 (R/W): Trigger source selection, default: 0, no trigger is enabled

Bit 0: Enable internal trigger, periodic (0x8C);
Bit 1: Enable internal trigger, random (0x88);
Bit 2: Enable internal trigger sequence (to be implemented);
Bit 3: not used;
Bit 4: Enable external trigger input;
Bit 14: BLEACH daisy chain ('OR' function) control. '1' to disable, '0' to enable (default);
Bit 15: Trigger daisy chain control ('OR' function). '1' to disable, '0' to enable (default);
Bit (31:16, 13:5): not used.

➢ Address offset: 0x002C (R/W): Clock source selection, default: 0, oscillator clock

Bit 0: Clock source selection, default: 0
0: on-board oscillator;
1: External LEMO connector input.
Bit(31:1): not used

- Address offset: 0x0040 (R/W): LED calibration channel enable, default: 0x00000000, all disabled

  Bit(0): Calibration enable setting check, OR of bits(18:1); If this bit is '1', the bleaching will not be enabled.
  Bit (18:1): Connector#1 (front panel, top), Channels#18-#1 enable, 1: enable, 0: disable;
  Bit (23:19): not used
  Bit (26:24): Bleach current setting/control of connector#1;
  Bit (27): Bleaching LDO regulator enable
  Bit (31:28): "1011": These 36 channel bleaching enable, otherwise bleaching disabled

- Address offset: 0x0044 (R/W): LED calibration channel enable, default: 0x00000000, all disabled

  Bit(0): Calibration enable setting check, OR of bits(18:1);
  Bit (18:1): Connector#1(front panel, top), Channels#36-#19; 1: enable, 0: disable
  Bit (31:19): not used

- Address offset: 0x0048 (R/W): LED calibration channel enable, default: 0x00000000, all disabled

  Bit(0): Calibration enable setting check, OR of bits(18:1); If this bit is '1', the bleaching will not be enabled.
  Bit (18:1): Connector#2 (front panel, Middle), Channels#18-#1 enable, 1: enable, 0: disable;
  Bit (23:19): not used
  Bit (26:24): Bleach current setting/control of connector#2;
  Bit (27): Bleaching LDO regulator enable
  Bit (31:28): "1011": These 36 channel bleaching enable, otherwise bleaching disabled

- Address offset: 0x004C (R/W): LED calibration channel enable, default: 0x00000000, all disabled

  Bit(0): Calibration enable setting check, OR of bits(18:1);
  Bit (18:1): Connector#2(front panel, Middle), Channels#36-#19; 1: enable, 0: disable
  Bit (31:19): not used

- Address offset: 0x0050 (R/W): LED calibration channel enable, default: 0x00000000, all disabled

  Bit(0): Calibration enable setting check, OR of bits(18:1); If this bit is '1', the bleaching will not be enabled.
  Bit (18:1): Connector#3 (front panel, Bottom), Channels#18-#1 enable, 1: enable, 0: disable;
  Bit (23:19): not used
  Bit (26:24): Bleach current setting/control of connector#3;
  Bit (27): Bleaching LDO regulator enable
  Bit (31:28): "1011": These 36 channel bleaching enable, otherwise bleaching disabled

- Address offset: 0x0054 (R/W): LED calibration channel enable, default: 0x00000000, all disabled

  Bit(0): Calibration enable setting check, OR of bits(18:1);
  Bit (18:1): Connector#3(front panel, Bottom), Channels#36-#19; 1: enable, 0: disable
  Bit (31:19): not used

- Address offset: 0x0058 (R/W): LED calibration channel enable, default: 0x00000000, all disabled

Bit(0): Calibration enable setting check, OR of bits(18:1); If this bit is ‘1’, the bleaching will not be enabled.
Bit (18:1): Connector#4 (On-board, top), Channels#18-#1 enable, 1: enable, 0: disable;
Bit (23:19): not used
Bit (26:24): Bleach current setting/control of connector#4;
Bit (27): Bleaching LDO regulator enable
Bit (31:28): “1011”: These 36 channel bleaching enable, otherwise bleaching disabled

- Address offset: 0x005C (R/W): LED calibration channel enable, default: 0x00000000, all disabled

Bit(0): Calibration enable setting check, OR of bits(18:1);
Bit (18:1): Connector#4(On-board, top), Channels#36-#19; 1: enable, 0: disable
Bit (31:19): not used

- Address offset: 0x0060 (R/W): LED calibration channel enable, default: 0x00000000, all disabled

Bit(0): Calibration enable setting check, OR of bits(18:1); If this bit is ‘1’, the bleaching will not be enabled.
Bit (18:1): Connector#5 (On-board, Bottom), Channels#18-#1 enable, 1: enable, 0: disable;
Bit (23:19): not used
Bit (26:24): Bleach current setting/control of connector#5;
Bit (27): Bleaching LDO regulator enable
Bit (31:28): “1011”: These 36 channel bleaching enable, otherwise bleaching disabled

- Address offset: 0x0064 (R/W): LED calibration channel enable, default: 0x00000000, all disabled

Bit(0): Calibration enable setting check, OR of bits(18:1);
Bit (18:1): Connector#5(On-board, bottom), Channels#36-#19; 1: enable, 0: disable
Bit (31:19): not used

- Address offset: 0x0068 (R/W): Bleaching time setting, default:

Bit [31:28]: 0xB, or “1011” for bleaching timer enable
Bit [27:0]: bleaching timer in the units of 20ns*1024*1024, which is about 21ms. The maximum is about two months.

- Address offset: 0x006C (R/W): Pulse shape loading, default: 4ns rising, 25ns falling edge pulses

Bit [5:0]: DAC_D[5:0], pulse shape loading, the sample# automatically counts up. 2048 (or smaller) samples at 2ns per sample ➔ total pulse width: ~4us;
Bit [6]: DAC_D_ZERO, a base line setting for the DAC;
Bit [7]: to generate trigger?
Bit [15:8]: similar to Bit[7:0], but it is for the next 2ns;
Bit [31:16]: similar to Bit [15:0]. Width matched from 32-bit to 16-bit for efficient pulse shape loading.
512 deep/32-bit wide in loading,
1024 deep/16-bit wide in reading at 4ns,
2048 deep/8-bit wide after DDR at DAC at 2ns.

- Address offset: 0x0070 (R/W): Calibration pulse width, default “01,0100,0000”

Bit [9:0]: Calibration pulse width, in ClkCal periods (4ns steps), max ~ 4us.

- Address offset: 0x0074 (R/W): Analog switch control enable (default 0)

Bit [7:0]: Switch control enable delay setting (delay after trigger), in ClkCal periods (4ns steps).
Bit [15:9]: switch control enable width, in ClkCal period (4 ns steps). When set to 0x00, the enable is always true (infinitely wide). Bit[8] is reserved for ½ ClkCal period width setting (to be implemented).

- Address offset: 0x0078 (R): Bleaching timer reading:

  Bit [31:28]: Reg0x68 bit(31:28) read back,
  Bit [27:0]: bleaching timer in the units of 20ns*1024*1024, which is about 21ms.

- Address offset: 0x007C (R): Bleaching timer read back:

  Bit [31:20]: 0xF1E, (Fine),
  Bit [19:0]: bleaching timer in the units of 20ns. This part is not used for Bleach Timer comparison.

- Address offset: 0x0088 (R/W): Random Pulsing, default 0,

  Bit [7:0]: Random pulsing speed setting (average period). Bit[7] random trigger enable. Bit[6:4]=Bit[2:0], Bit[3:0] random trigger rate: ~{700 KHz / (2**Bit[3:0])}. For example, Bit[3:0]=0101 (5 in decimal), the average random trigger rate is about 700KHz/32, or ~20 KHz;
  Bit [31:8]: not used

- Address offset: 0x008C (R/W): Periodic pulsing, default 0,

  Bit [15:0]: number of repeat for periodic triggers/pulsing, if set to 0xFFFF, the trigger will not stop
  Bit [31:16]: Pulsing period. (2048**Bit#31) * (Bit(30:16) + 1) * 20ns, for example: 0x003F ➔ 1.3us; 0x803F ➔ 2.6 ms.

- Address offset: 0x00DC (R): Total number of triggers (not implemented yet),

  Bit [31:0]: number of trigger.

- Address offset: 0x00100 (W): Reset and one-shot registers. The signal will be one VME clock cycle. If the VME clock is 50 MHz, the one-shot will be 20ns wide. Positive logic. (to be implemented).

  Bit 1: if ‘1’, RESET signal to reset the VME_to_I2C engine;
  Bit 2: if ‘1’, RESET signal to reset the VME_to_JTAG engine;
  Bit 4: if ‘1’, RESET signal to reset the VME registers (VLD settings) to their default values;
  Bit 5: if ‘1’, RESET signal to reset the Pulse_shape memory load address to 0.
  Bit 8: if ‘1’, Reset the Clock DCM.
  Bit 10: if ‘1’, Reset the MGT (MultiGigabit Transceiver,) inside the FPGA (for JESD204).
  Bit 21: if ‘1’, clock reset for the ClkVme, and all other clocks (similar to Sync_code 0x11), Generic RESET of the VLD. Be cautious to use this.

6.3 VME to Serial engines (to be implemented as needed):

A24D32 are used for VME to serial engines. The two engines are “VME to JTAG engine for the FPGA”, and “VME to I2C engine for the P2 connector (could be used for anything)”. In the I2C engines design, only the lower one-byte or 2-byte of the 32-bit data word is used. The higher bytes are not used. The A(1:0) are required to be “00”.

Address offset A(18:0): 0x2XXXX: JTAG for FPGA;
Address offset A(18:0): 0x4XXXX: I2C for the P2 connector;

7 Front panel IO Connectors' Pinout tables:

7.1 Front panel FPtop, FPmid, and FPbot Pinout Table (3M P50E-080P1-SR1), all are outputs. On-board connector OBtop, and OBbot

Pin name	Signal Description	Signal Level	Direction
#1	Ch#1 LED driver	#2	GND
#3	Ch#2 LED driver	#4	GND
#5	Ch#3 LED driver	#6	GND
#7	Ch#4 LED driver	#8	GND
#9	Ch#5 LED driver	#10	GND
#11	Ch#6 LED driver	#12	GND
#13	Ch#7 LED driver	#14	GND
#15	Ch#8 LED driver	#16	GND
#17	Ch#9 LED driver	#18	GND
#19	Ch#10 LED driver	#20	GND
#21	Ch#11 LED driver	#22	GND
#23	Ch#12 LED driver	#24	GND
#25	Ch#13 LED driver	#26	GND
#27	Ch#14 LED driver	#28	GND
#29	Ch#15 LED driver	#30	GND
#31	Ch#16 LED driver	#32	GND
#33	Ch#17 LED driver	#34	GND
#35	Ch#18 LED driver	#36	GND
#37, #39	Floating GND	#38,#40	Floating GND
#41	Ch#19 LED driver	#42	GND
#43	Ch#20 LED driver	#44	GND
#45	Ch#21 LED driver	#46	GND
#47	Ch#22 LED driver	#48	GND
#49	Ch#23 LED driver	#50	GND
#51	Ch#24 LED driver	#52	GND
#53	Ch#25 LED driver	#54	GND
#55	Ch#26 LED driver	#56	GND
#57	Ch#27 LED driver	#58	GND
#59	Ch#28 LED driver	#60	GND
#61	Ch#29 LED driver	#62	GND
#63	Ch#30 LED driver	#64	GND
#65	Ch#31 LED driver	#66	GND
#67	Ch#32 LED driver	#68	GND
#69	Ch#33 LED driver	#70	GND
#71	Ch#34 LED driver	#72	GND
#73	Ch#35 LED driver	#74	GND
#75	Ch#36 LED driver	#76	GND
#77#79	Floating GND	#78#80	Floating GND

7.2 LEMO connector:

LEMO#11	Clock_input	LEMO#12	Trigger_input
LEMO#21	Bleach_output	LEMO#22	Trigger_output

8 VLD Operation examples (to be updated):

The following is some operating procedures at VxWorks interactive mode. This is just a memo for the quick test of the VLD board. They may change as the VLD debug proceeds. First, one needs to login the VME controller. Here is the sequence:

> From any xterm on daq network computers, telnet to DAVW5 (neither username, nor password is needed). Only one telnet process is supported for the MVME6100 module). The address mapping for A24 is 0x90xxxxxx.
>
> DAVW5: ld < usrTempeDma_AM.o; //load the custom vme Address Modifier library to the CPU.
>
> DAVW5: ld < trigger.o; // If necessary, load the user software code.

The following commands are assuming that the VLD is in slot#13 VME64x compatible crate (Geographic address available). 0x68 = 01101xxx, that is the Geographic Address GA=13 or 01101.

8.1 A24 register echoing (write and read):

DAVW5: *(0x90680000)=0x64; the same register should be read out, with Bit(31:24) == 0x1D, and Bit(7:0) == 0x64, and non-zero Bit(23:8).

8.2 A24 register reset (to be implemented)

The VME registers are reset to their default by setting register 0x100, bit#4:

DAVW5: *(0x90680100)=0x10: VME_to_JTAG engine logic reset

8.3 VLD test code

The VLD production test code can be found at /daqfs/home/jgu/Trigger_software/trigger.c.

VLDtest2: VLD firmware update (loading the flash memory);

VLDtest5: VLD calibration pulse shape loading.

VLDtest6: VLD test, channel by channel calibration, and connector by connector Bleaching test;

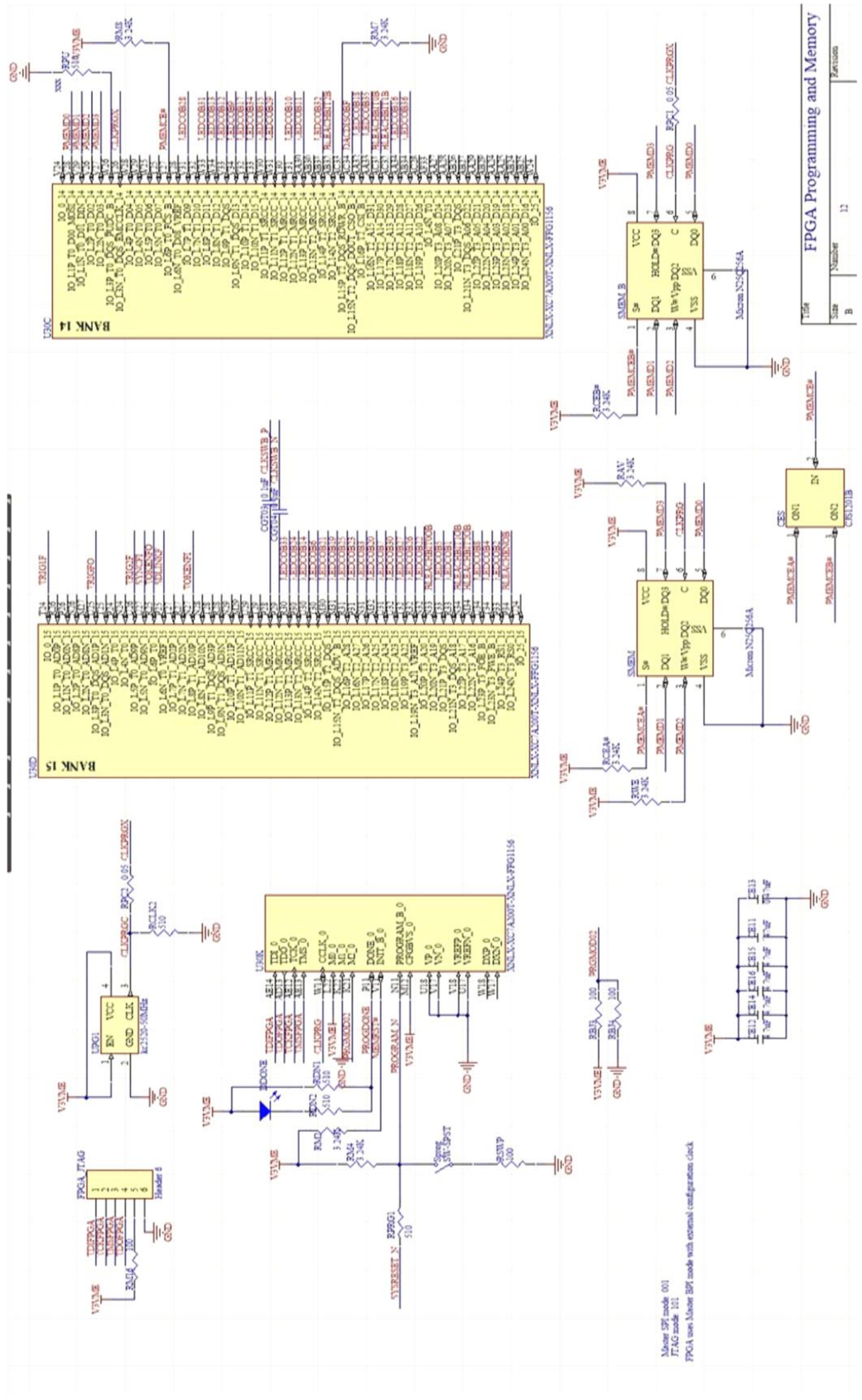
VLDtest7: VLD clock source switching and trigger source switching.

9. Citations:

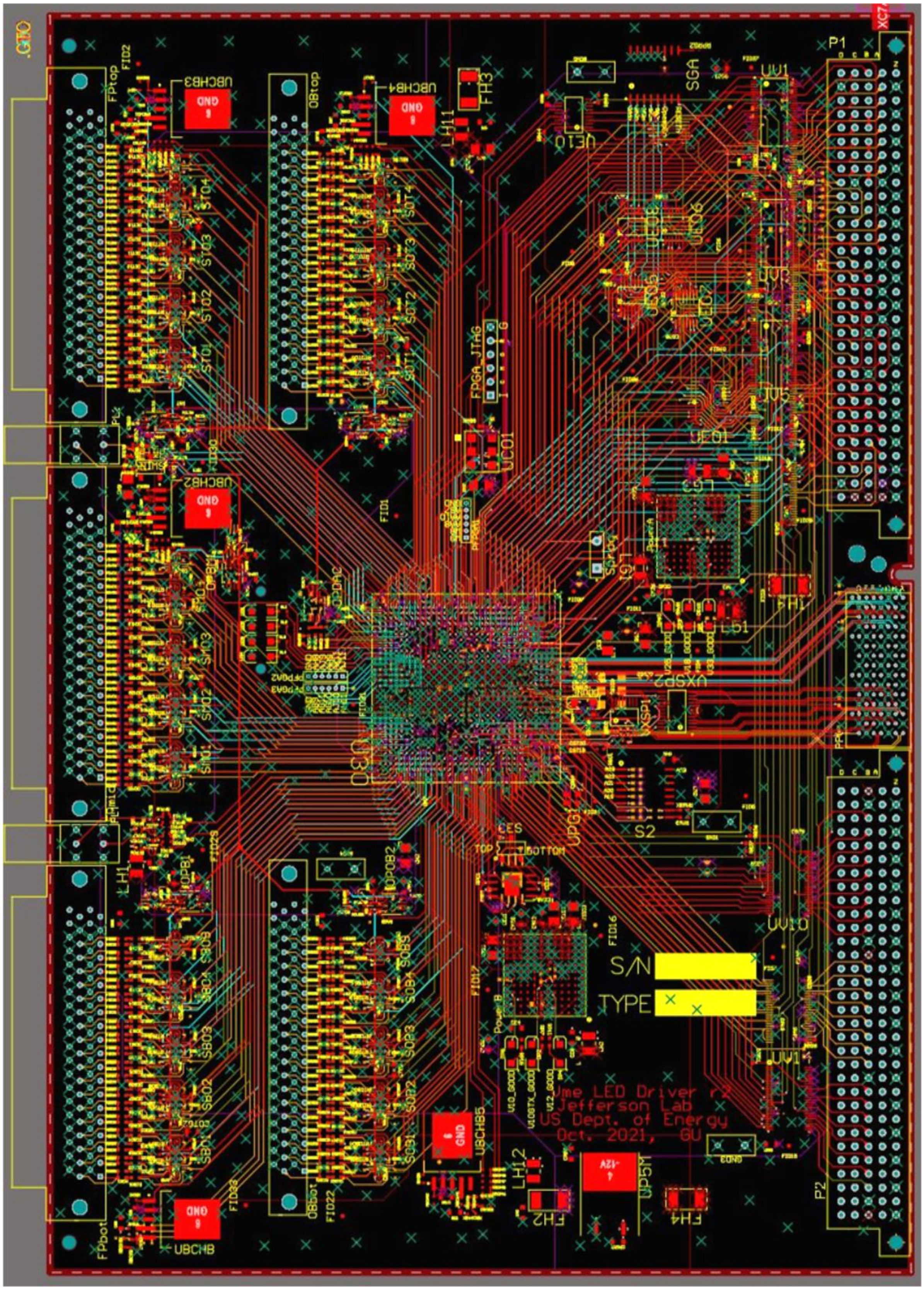
Works Cited

1. NPS experiment
2. GU, TI/TD design document
3. GU, VETROC design document
4. Carlos, LED driver requirement
5. Brad, Further explanation of LED driver requirement
6. GU, VLD tests

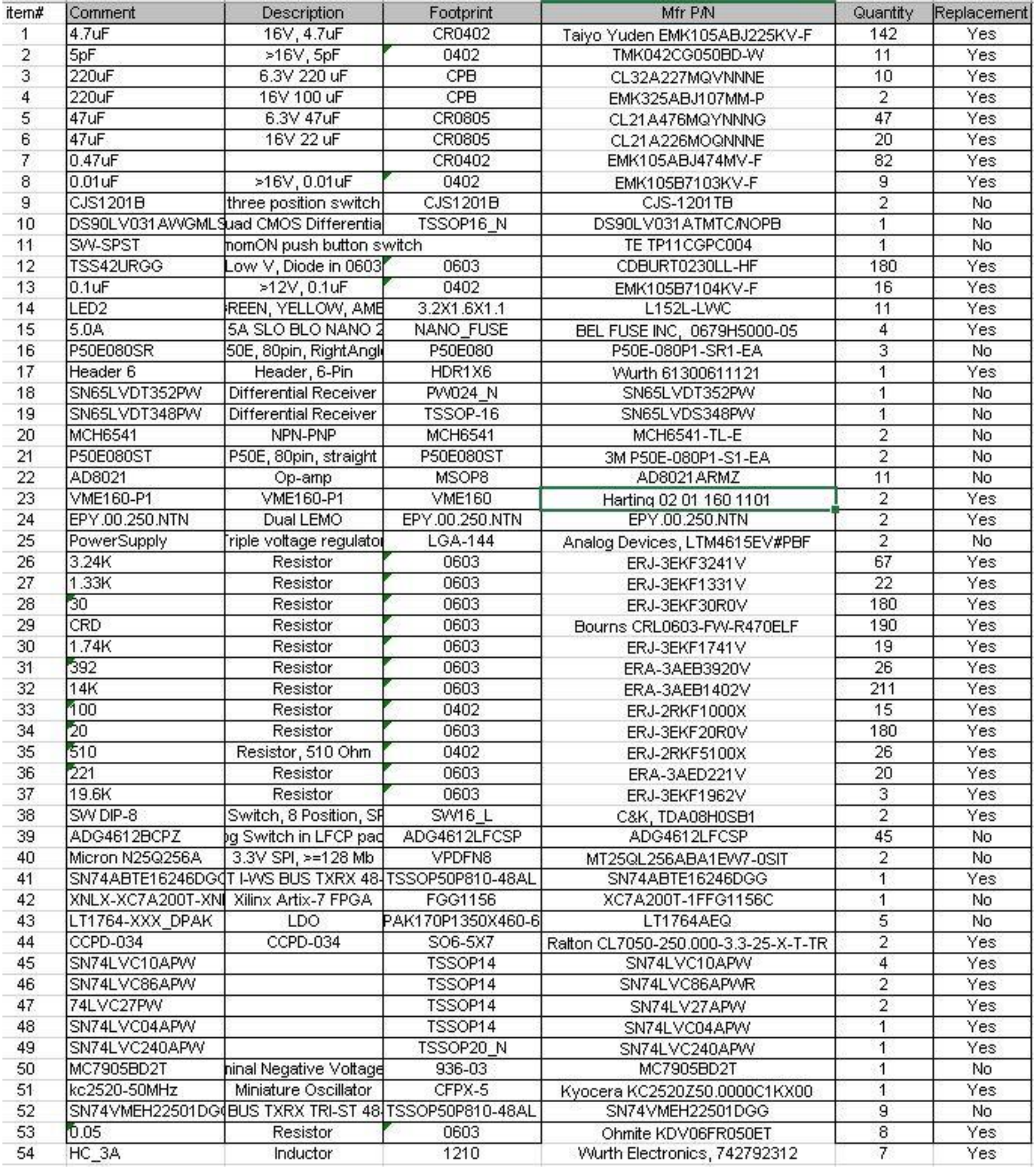
Appendix A: VLD Schematics:


FPGA Programming and Memory
BANK 14
BANK 15
Micron N25Q256A
Micron N25Q256A
FPGA_JTAG
Master SPI mode 001
JTAG mode 101
FPGA uses Master BPI mode with external configuration clock

Appendix B: VLD fabrication drawing:



Appendix C: VLD Bill of materials:



item#	Comment	Description	Footprint	Mfr P/N	Quantity	Replacement
1	4.7uF	16V, 4.7uF	CR0402	Taiyo Yuden EMK105ABJ225KV-F	142	Yes
2	5pF	>16V, 5pF	0402	TMK042CG050BD-W	11	Yes
3	220uF	6.3V 220 uF	CPB	CL32A227MQVNNNE	10	Yes
4	220uF	16V 100 uF	CPB	EMK325ABJ107MM-P	2	Yes
5	47uF	6.3V 47uF	CR0805	CL21A476MQYNNNG	47	Yes
6	47uF	16V 22 uF	CR0805	CL21A226MOQNNNE	20	Yes
7	0.47uF		CR0402	EMK105ABJ474MV-F	82	Yes
8	0.01uF	>16V, 0.01uF	0402	EMK105B7103KV-F	9	Yes
9	CJS1201B	three position switch	CJS1201B	CJS-1201TB	2	No
10	DS90LV031AWGMLS	uad CMOS Differentia	TSSOP16_N	DS90LV031ATMTC/NOPB	1	No
11	SW-SPST	nomON push button switch		TE TP11CGPC004	1	No
12	TSS42URGG	Low V, Diode in 0603	0603	CDBURT0230LL-HF	180	Yes
13	0.1uF	>12V, 0.1uF	0402	EMK105B7104KV-F	16	Yes
14	LED2	REEN, YELLOW, AME	3.2X1.6X1.1	L152L-LWC	11	Yes
15	5.0A	5A SLO BLO NANO 2	NANO_FUSE	BEL FUSE INC, 0679H5000-05	4	Yes
16	P50E080SR	50E, 80pin, RightAngl	P50E080	P50E-080P1-SR1-EA	3	No
17	Header 6	Header, 6-Pin	HDR1X6	Wurth 61300611121	1	Yes
18	SN65LVDT352PW	Differential Receiver	PW024_N	SN65LVDT352PW	1	No
19	SN65LVDT348PW	Differential Receiver	TSSOP-16	SN65LVDS348PW	1	No
20	MCH6541	NPN-PNP	MCH6541	MCH6541-TL-E	2	No
21	P50E080ST	P50E, 80pin, straight	P50E080ST	3M P50E-080P1-S1-EA	2	No
22	AD8021	Op-amp	MSOP8	AD8021ARMZ	11	No
23	VME160-P1	VME160-P1	VME160	Harting 02 01 160 1101	2	Yes
24	EPY.00.250.NTN	Dual LEMO	EPY.00.250.NTN	EPY.00.250.NTN	2	Yes
25	PowerSupply	Triple voltage regulato	LGA-144	Analog Devices, LTM4615EV#PBF	2	No
26	3.24K	Resistor	0603	ERJ-3EKF3241V	67	Yes
27	1.33K	Resistor	0603	ERJ-3EKF1331V	22	Yes
28	30	Resistor	0603	ERJ-3EKF30R0V	180	Yes
29	CRD	Resistor	0603	Bourns CRL0603-FW-R470ELF	190	Yes
30	1.74K	Resistor	0603	ERJ-3EKF1741V	19	Yes
31	392	Resistor	0603	ERA-3AEB3920V	26	Yes
32	14K	Resistor	0603	ERA-3AEB1402V	211	Yes
33	100	Resistor	0402	ERJ-2RKF1000X	15	Yes
34	20	Resistor	0603	ERJ-3EKF20R0V	180	Yes
35	510	Resistor, 510 Ohm	0402	ERJ-2RKF5100X	26	Yes
36	221	Resistor	0603	ERA-3AED221V	20	Yes
37	19.6K	Resistor	0603	ERJ-3EKF1962V	3	Yes
38	SW DIP-8	Switch, 8 Position, SF	SW16_L	C&K, TDA08H0SB1	2	Yes
39	ADG4612BCPZ	g Switch in LFCP pac	ADG4612LFCSP	ADG4612LFCSP	45	No
40	Micron N25Q256A	3.3V SPI, >=128 Mb	VPDFN8	MT25QL256ABA1EW7-0SIT	2	No
41	SN74ABTE16246DGC	T I-WS BUS TXRX 48-	TSSOP50P810-48AL	SN74ABTE16246DGG	1	Yes
42	XNLX-XC7A200T-XNI	Xilinx Artix-7 FPGA	FGG1156	XC7A200T-1FFG1156C	1	No
43	LT1764-XXX_DPAK	LDO	PAK170P1350X460-6	LT1764AEQ	5	No
44	CCPD-034	CCPD-034	SO6-5X7	Ralton CL7050-250.000-3.3-25-X-T-TR	2	Yes
45	SN74LVC10APW		TSSOP14	SN74LVC10APW	4	Yes
46	SN74LVC86APW		TSSOP14	SN74LVC86APWR	2	Yes
47	74LVC27PW		TSSOP14	SN74LV27APW	2	Yes
48	SN74LVC04APW		TSSOP14	SN74LVC04APW	1	Yes
49	SN74LVC240APW		TSSOP20_N	SN74LVC240APW	1	Yes
50	MC7905BD2T	ninal Negative Voltage	936-03	MC7905BD2T	1	No
51	kc2520-50MHz	Miniature Oscillator	CFPX-5	Kyocera KC2520Z50.0000C1KX00	1	Yes
52	SN74VMEH22501DG(	BUS TXRX TRI-ST 48-	TSSOP50P810-48AL	SN74VMEH22501DGG	9	No
53	0.05	Resistor	0603	Ohmite KDV06FR050ET	8	Yes
54	HC_3A	Inductor	1210	Wurth Electronics, 742792312	7	Yes

Appendix D: Document revision history:

Document started on Sept. 4th, 2020: Using the TI documentation format;

First release on Sept. 14th, 2020: to circulate to the NPS group for design feedback

Jan. 4, 2021: Added the FPGA DAC and Bleach regulator controls. Confirmed that the LED's Cathodes are tied to common ground.

Jan. 11, 2021: updated with Chris and Brad.

Mar. 31, 2021: Further update after the VLD PCB design.

Mar. 25, 2022: Added some test results, and matched with the production boards.

Apr. 1-8, 2022: overall review after the production tests.

Dec. 14, 2022: Added the register 0x78, 0x7C for bleaching timer read out.

Feb. 15, 2023: Use VmeRst(5) to reset the Pulse_shape memory loading address (to 0); Fix the mistake in Reg 0x6C description, updated reg 0x8C description

May 15, 2023: Add the Trigger, Bleach LEMO daisy chain ("OR"), and reg 0x20 bit(15:14) control.