

SFI Trigger Interface

Version 2

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Introduction

As part of a data acquisition system a Read Out Controller (ROC) must be told when to extract data from the front-end modules under its control. The experimenter's trigger system is the origin of this signal, and it may be capable of supplying information about the character of the event as well. The SFI Trigger Interface enables the SFI read out controller to have access to this information. This data may be used by the ROC to selectively read the subset of modules most relevant to that event.

The SFI Trigger Interface module can accept triggers from one of two possible sources: Trigger Supervisor (TS) or External triggers.

The TS mode is useful for multiple ROC systems. In this mode the trigger data (8 bits) enters the interface module through a special parallel trigger cable driven by the Trigger Supervisor. This cable links all ROCs in the system. The TS itself maintains system busy and asserts signals that are used for gating front-end modules. Every ROC in the system must acknowledge to the TS that it has finished handling the front-end data relevant to the current trigger before new trigger data can be sent by the TS. When in TS mode the SFI Trigger Interface allows the SFI ROC to execute this protocol. (For more information see the Trigger Supervisor User Manual.)

The External trigger mode is useful for single ROC systems or test setups. In this mode up to 4 independent free running user triggers and 2 data levels can be accepted. When the OR of the 4 triggers is asserted all 6 input lines are latched, forming 6 bits of trigger data. Subsequent triggers are held off and a prompt signal is issued that can be used in the gating of front-end modules. The busy state is maintained until cleared by the ROC. This is done when the ROC has processed all data associated with the current trigger.

The STR340 Struck Fastbus Interface (SFI) is a Fastbus Read Out Controller that is managed through VME protocols by a VME Single Board Computer (SBC). The presence of trigger data at the trigger interface module is communicated to the VME SBC by means of interrupts or polling (see the SFI manual for details).

In addition to the functions described above the trigger interface has some general purpose I/O capability. The module has an 8-bit output port that is available for use. When the interface is set up in the TS mode of triggering, the 4 external trigger inputs and 2 data level inputs function as a 6-bit input port. The state of these 6 inputs is latched upon a read of the SFI Trigger Interface Register.

The SFI Trigger Interface is implemented as a standard Fastbus Auxiliary card, and communicates with the SFI through its Auxiliary Port.

SFI Trigger Interface Register

Bits are Read/Write unless otherwise indicated. Bits function as follows:

(0)-(7) TRIGGER DATA (Read only) - when in TS mode this represents the encoded trigger information generated by the TS (see Trigger Supervisor User Manual for detailed information).

- (0) synchronization flag
- (1) late fail flag
- (2)-(7) ROC code

When in external trigger mode this represents the latched status of the 4 external trigger inputs and 2 data levels.

- (0) Trigger 0 input status
- (1) Trigger 1 input status
- (2) Trigger 2 input status
- (3) Trigger 3 input status
- (4) Data A input status
- (5) Data B input status
- (6)-(7) Unused (read as 0)

(8) TRIGGER MODE - setting this bit selects the external trigger mode of operation. In this mode the 4 independent free running user triggers and 2 data levels are recognized by the interface. Clearing this bit selects the TS mode of operation. In this mode trigger data originating from the TS is recognized by the interface.

(9) ENABLE EXTERNAL TRIGGERS - if the external trigger mode has been selected, setting this bit enables these inputs for use. If cleared, any external triggers are ignored. When in TS mode, this bit has no effect.

(10) SAMPLE MODE - if the TS mode has been selected, setting this bit allows the 4 external trigger inputs and 2 data level inputs to function as a 6-bit input port. A read of this register will latch the state of these 6 inputs, with the data appearing in bits (16)-(21).

(11)-(12) RESERVED

(13)-(14) VERSION ID (Read only) - Version 1: bit 13 = 1, bit 14 = 1
Version 2: bit 13 = 0, bit 14 = 1.

(15) RESET (Write only) - asserting this bit resets the interface. Bits (8)-(10), (23)-(31) of this register are cleared.

(16)-(21) EXTERNAL DATA (Read only) - external data is latched upon read of this register (see SAMPLE MODE).

(22) UNUSED - (Read as 1)

(23) ENABLE OUTPUT PORT WRITE - setting this bit is required when a write to the OUTPUT PORT (bits 24-31) is desired. Not asserting this bit during a register write allows the contents of the Output Port to remain unchanged while other register bits are modified.

(24)-(31) OUTPUT PORT - this data pattern appears at the 8 general-purpose outputs of the interface.

Using the Trigger Interface with the SFI

For complete information about controlling the SFI see the SFI manual. In the following outlines the address 'E0EXXXXX' implies a VME address offset for A24/D32 cycles of 'E000000', and SFI base address of E00000. (HEX format is implied for all addresses and data values.)

General procedure for use of the Trigger Interface with interrupts:

1. Initialize Trigger Interface - write data 8000 to Trigger Interface register (see details below).
2. Setup VME Single Board Computer - enable VME interrupts and connect interrupt service routine (details depend on computer and OS used).
3. Set SFI VME Interrupt Level and Status ID - write to address E0E02X10 the binary data [1,Lev2,Lev1,Lev0,ID7,...,ID0], where (Lev3,Lev2,Lev1) is the binary encoded VME interrupt level, and (ID7,...,ID0) is the Interrupt Status ID.
4. Enable Auxiliary Port Interrupts on SFI - write data value 10 to address E0E02X14.
5. Select Trigger Source on Trigger Interface - write appropriate data to Trigger Interface register to select TS or External trigger source. (Enable bit must also be set for External triggers.)

An incoming trigger will now cause the execution of the user's Interrupt Service Routine (ISR). The ISR routine should do the following:

1. Read Trigger Interface Register - (if desired).
2. Execute User Code - (application dependent).
3. Set Trigger Acknowledge - write data 1000 to address E0E01X00.
4. Clear SFI Interrupt Flag - write data 1000 to address E0E02X14.
5. Re-enable Interrupt Source - write data 10 to address E0E02X14.
6. Clear Trigger Acknowledge - write data 10000000 to address E0E01X00. This MUST be the last action in the ISR.

General procedure for use of the Trigger Interface with polling:

1. Initialize Trigger Interface - write data 8000 to Trigger Interface register (see details below).
2. Disable Auxiliary Port Interrupts on SFI - write data value 1000 to address E0E02X14.
3. Select Trigger Source on Trigger Interface - write appropriate data to Trigger Interface register to select TS or External trigger source. (Enable bit must also be set for External triggers.)

An incoming trigger will now cause a ZERO value for bit 15 of the SFI Input Register (address E0E02X0C). Upon detecting this, the user should do the following:

1. Read Trigger Interface Register - (if desired).
2. Execute User Code - (application dependent).
3. Set Trigger Acknowledge - write data 1000 to address E0E01X00.
4. Clear Trigger Acknowledge - write data 10000000 to address E0E01X00.

Writing and Reading the Trigger Interface Register

(HEX format is implied for all addresses and data values.)

Write Data to Trigger Interface Register:

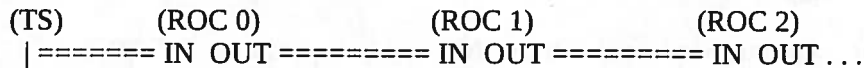
1. Disable Fastbus Sequencer - write ANY data to key address E0E02X24.
2. Write Data to INTERNAL Auxiliary Port Register - address E0E01X10.
3. Enable Data Path to Auxiliary Connector - write data value 4000 to address E0E01X00.
4. Generate Write Strobe to Auxiliary Port - write ANY data to address E0E01X14. A pulse is created.
5. Disable Data Path to Auxiliary Port - write data 40000000 to address E0E01X00.
6. Enable Fastbus Sequencer (if desired) - write ANY data to key address E0E02X20.

Read Data from Trigger Interface Register:

1. Disable Fastbus Sequencer - write ANY data to key address E0E02X24.
2. Enable Data Path from Auxiliary Connector - write data value 2000 to address E0E01X00.
3. Read Internal Fastbus I/O - read of address E0E01X00 has data of Trigger Interface Register.
4. Disable Data Path from Auxiliary Port - write data 20000000 to address E0E01X00.
5. Enable Fastbus Sequencer (if desired) - write ANY data to key address E0E02X20.

Connecting and Configuring the Trigger Interface (Refer to Figure 1).

TS Connection - the IN/OUT connector pair is associated with the TS trigger data cable. This cable is designed to link multiple ROCs with the TS in a linear fashion. The IN connector accepts the cable from the TS. The OUT connector is cabled to the next ROC interface's IN connector. This pattern is repeated for the additional ROCs in the chain. Up to 8 ROCs can be supported on such a link. The TS drives 4 independent links for a maximum of 32 ROCs in a system. The cables should be twisted pair (ribbon or bundled) having a nominal impedance of 100 ohms.



The last ROC in the chain must properly terminate the signals of the link. This is accomplished with SIP resistor packs as shown below. Only the LAST card along the cable should have the resistors inserted.

<u>Location</u>	<u>Package</u>	<u>Resistor Type</u>	<u>Comment</u>
R10	8-pin SIP	100 ohm isolated	-----
R11	8-pin SIP	100 ohm isolated	-----
R18	8-pin SIP	100 ohm isolated	-----
R12	10-pin SIP	180 ohm bussed	NOTE PIN 1
R13	10-pin SIP	180 ohm bussed	NOTE PIN 1

ROC Number - The ROC number is the Acknowledge line (ACK 0-7) that the ROC is assigned to on the TS trigger data cable. This assignment must be unique on a cable. The physical location of the ROC along the TS trigger data cable is independent of this logical ROC number.

The ROC number is set using the 8-row x 6-column PIN HEADER array illustrated in Figure 1. The rows are labeled 0-7 on the board correspond to Acknowledge lines 0-7. We refer to the columns from left to right as columns 1-6. To set ROC number 'N', go to row 'N' and place a jumper that bridges columns 2-3, and a jumper that bridges columns 4-5. ALL other rows must have jumpers that bridge columns 1-2 and columns 5-6.

External Trigger Inputs - Triggers 0-3 can be individually enabled to contribute to the OR of trigger inputs by installing jumpers at locations labeled J0-J3 on the board. The absence of a jumper means that the corresponding input cannot itself trigger the interface. However, the state of such an input will be latched when the OR signal of the other enabled inputs is asserted. At least one of the 4 trigger inputs must be enabled to generate the OR signal.

Connector Signal Definitions

TS IN/OUT Connectors - signal levels are RS-485 (differential).

<u>Signal Name (Q)</u>	<u>Pin # (Q,/Q)</u>
Strobe	1,2
Sync	3,4
Late Fail	5,6
ROC Code Bit 0	7,8
ROC Code Bit 1	9,10
ROC Code Bit 2	11,12
ROC Code Bit 3	13,14
ROC Code Bit 4	15,16
ROC Code Bit 5	17,18
ROC 0 Acknowledge	19,20
ROC 1 Acknowledge	21,22
ROC 2 Acknowledge	23,24
ROC 3 Acknowledge	25,26
ROC 4 Acknowledge	27,28
ROC 5 Acknowledge	29,30
ROC 6 Acknowledge	31,32
ROC 7 Acknowledge	33,34

External Port Connector - signal levels are differential ECL.

<u>Signal Name (Q)</u>	<u>Pin # (Q,/Q)</u>	<u>Direction</u>
Trigger 0	1,2	Input
Trigger 1	3,4	Input
Trigger 2	5,6	Input
Trigger 3	7,8	Input
Data A	9,10	Input
Data B	11,12	Input
Level 1 Accept	15,16	Output
Busy	17,18	Output
Out 0	19,20	Output
Out 1	21,22	Output
Out 2	23,24	Output
Out 3	25,26	Output
Out 4	27,28	Output
Out 5	29,30	Output
Out 6	31,32	Output
Out 7	33,34	Output

Trigger Interface P2 Connector - rows A and C of connector P2 for VME slot 1 in the SFI are directly mapped to the DIN connector labeled P2 on the Trigger Interface. In addition, power/ground assignments of row B are P2 VME compatible.

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