Nuclear Physics Division

Data Acquisition Group

Description and Technical Information for the VME Trigger Interface and Distribution (TID) Module

J. William Gu (jgu@jlab.org)

Aug. 2nd, 2011

Table of Contents

1 Introduction

The Trigger Interface and Distribution (TID) module is being designed for the Jefferson Lab 12GeV upgrade, mainly for Hall-D[(Collaboration G. , 2009)] and Hall-B[(Collaboration C. , 2009)], with other experimental Halls [(experiments, 1990)] compatibility. This module is responsible for providing a low-jitter system clock and fixed latency trigger signals for the Front-end readout boards in the data acquisition crates. The modules also merge the front-end data acquisition crate status and generate a BUSY signal to request the Trigger Supervisor (TS) to pause the trigger. Figure 1a shows the placement of the TID modules in the global trigger distribution scheme in experiment setup. Figure 1b shows the crate level diagram

Figure 1a:

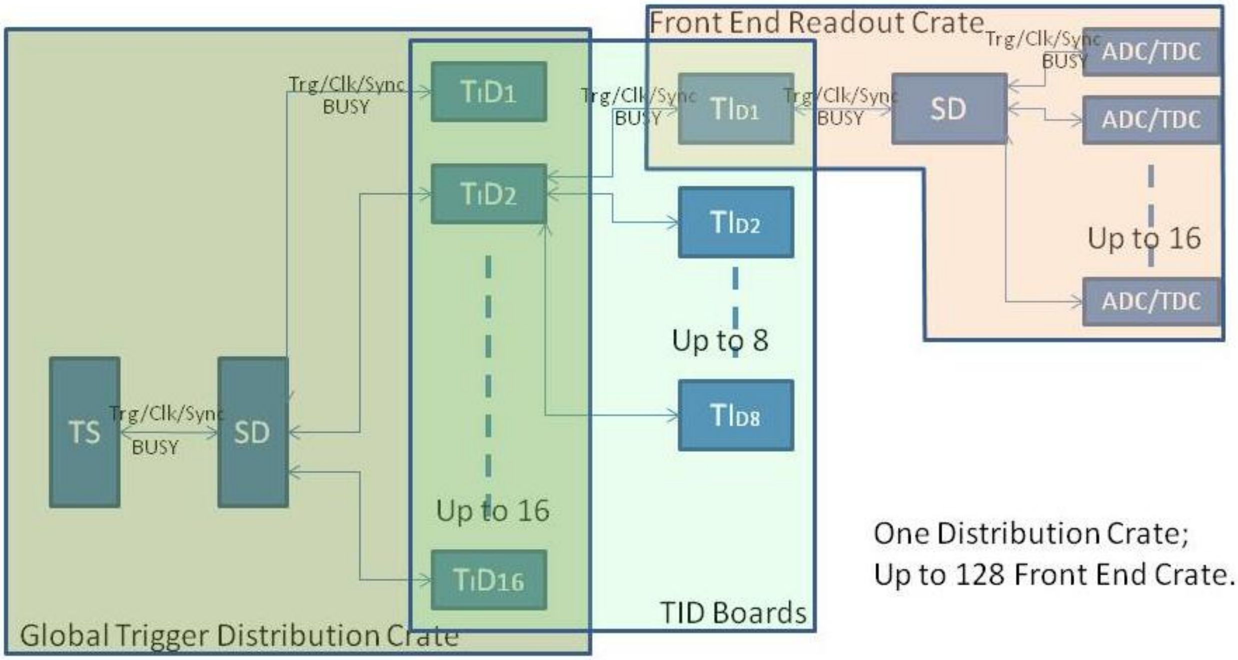
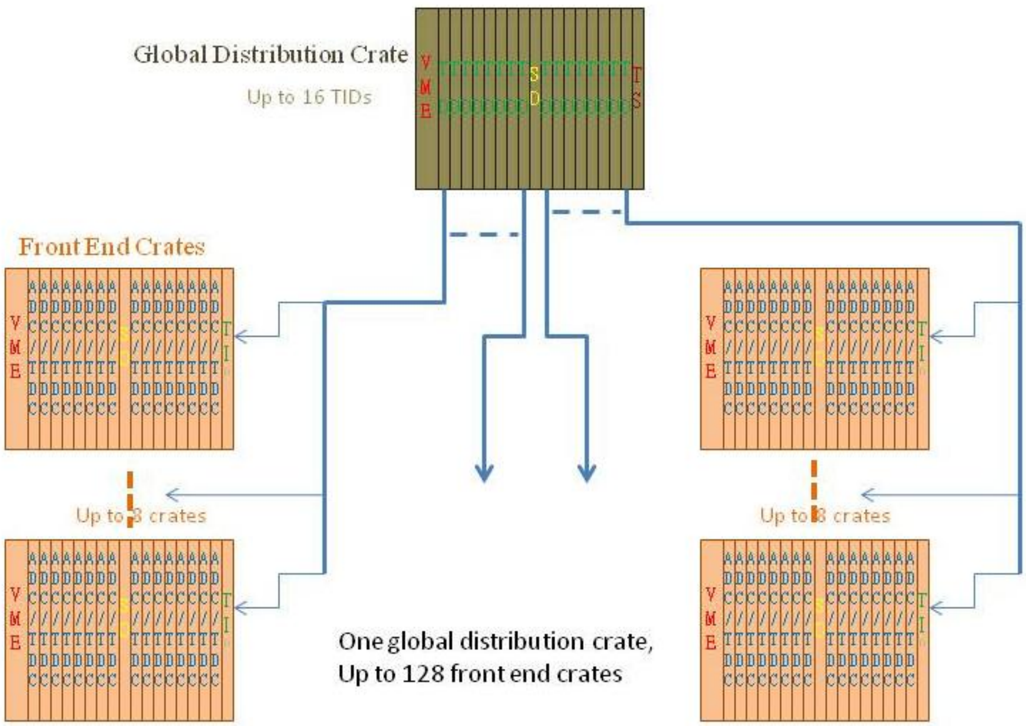


Figure 1b:


Global Distribution Crate
Up to 16 TIDs
VME
SD
TS
Front End Crates
VME
SD
TI
Up to 8 crates
Up to 8 crates
One global distribution crate,
Up to 128 front end crates

Depending on the PCB stuffing and mode settings, this module can sit in the Global Trigger/Clock Distribution Crate [(Chris, Hall_D trigger layout, 2009)] to fan out trigger and clock to the front-end crates, which is the functionality of Trigger Distribution (TD) [(Raydo, 2008)] modules; or sit in the last slot of a VME front-end data acquisition crate to send triggers to the Signal Distribution (SD) [(Cuevas, 2008)] module and Crate Trigger Processor (CTP) [(Chris, Gloabal Trigger Processor, 2009)], which is the functionality of the Trigger Interface (TI) [(GU, 2010)] module. The TID has simple Trigger Supervisor (TS) [(Ed, 2010)] functions built in. The TID can act as a subsystem trigger supervisor when used independently. With other TIDs, a subsystem with up to nine crates can be setup without a real TS module. The TID also has the flexibility to select the trigger and clock inputs from central trigger system or local (sub-system) trigger system.

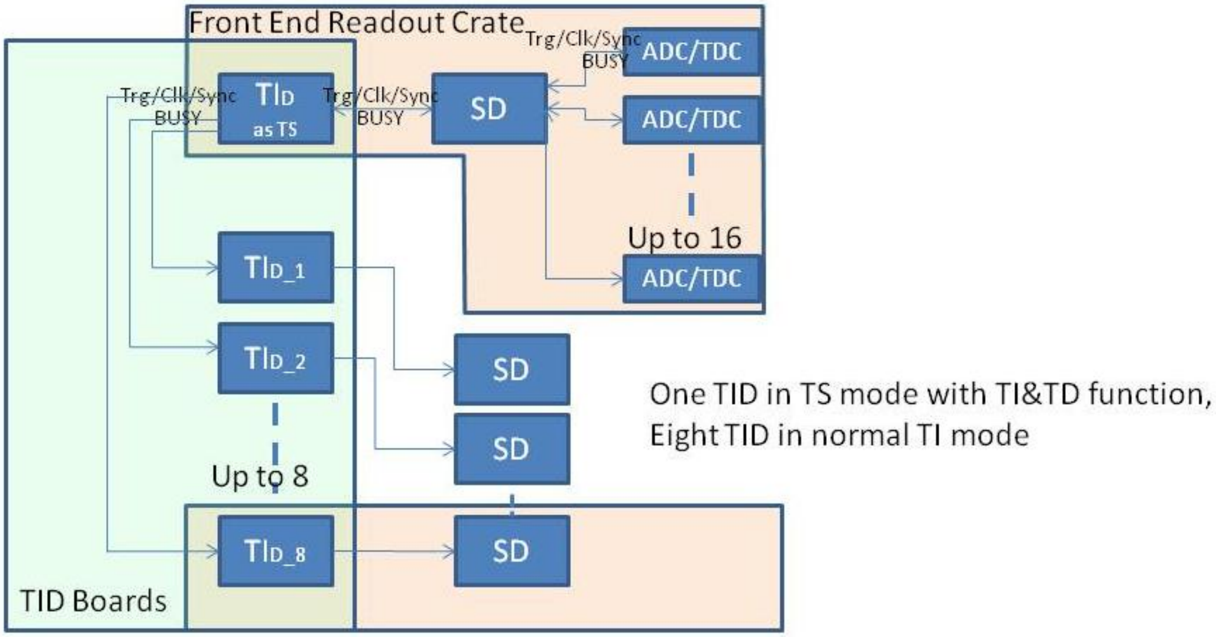
2 Purpose of the module

When the TID board is configured in Trigger Distribution (TD) mode, the TID in the global trigger distribution crate receives trigger/clock signals from the SD and fans out the signals for up to eight crates in the front end data acquisition system. The global trigger distribution crate is designed to house up to 16 TD modules, which provides trigger and clock for up to 128 crates. The TD distributes the following signals to each front end crates: global system clock, trigger words, and a custom serial link to establish a fixed latency from the trigger Supervisor to front end crates. In addition, the TD will receive status information from each crate that will be used to generate a ‘busy’ signal and also track various status registers of the front-end crates.

When the TID is configured in Trigger Interface (TI) mode, the TI to be positioned in the last slot of the front-end data acquisition crate connects to a TD module in the global trigger distribution crate. This is done using a four channels full-duplex fiber link, which provides a gigabit trigger link, global 250MHz clock and synchronization link to phase lock the trigger. The trigger link uses a reference clock derived from the 250MHz global pipeline clock allowing a trigger word to be distributed every 4 global pipeline clock cycles. Depending on the trigger word type the TI can issue a crate level trigger condition through the VXS switch port B. The trigger bits are sent to a Signal Distribution (SD) module that distributes these signals to all front-end modules in the crate. The TI also accepts status signals from the SD module, which is the logical OR of the status signals from all the other front-end modules. These status signals can be transmitted back to the TS through the fiber link to slow down or inhibit further distribution of triggers until the status has been resolved. For now, the status includes a BUSY only. When the BUSY is set, the front end boards are requesting for trigger inhibit. The assertion of a status signal will create a dead-time in the data acquisition system which should be a rare occurrence since the data acquisition is being designed to handle the full trigger rate that can occur from the physics events. The dead time will be monitored and recorded by the Trigger Supervisor board.

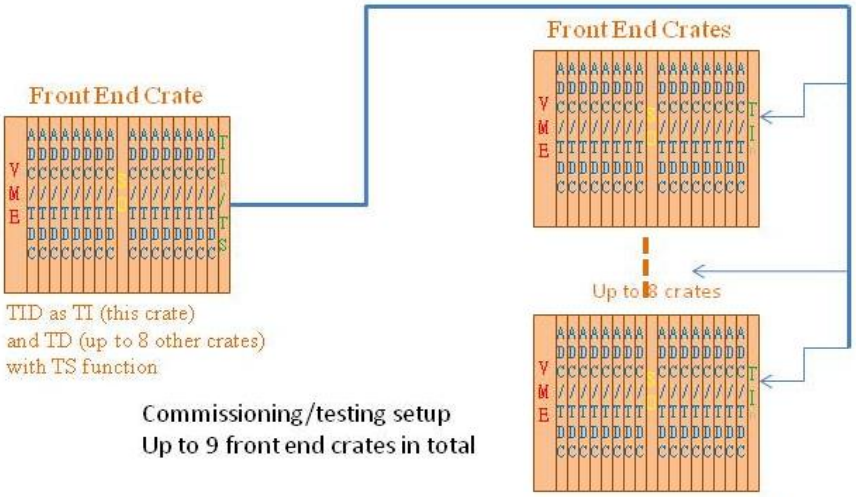
The TID can also perform simple Trigger Supervisor functions. In test setup or commissioning setup, the TID can perform as a TID Master (TM). In this case, it can take inputs from its front panel and generate trigger/clock like a TS, it can sends the trigger, clock, and SYNC to the backplane (P0 and P2) like a TI, and it can send the trigger, clock and SYNC to the front panel fibers like a TD. With the TM, a test setup can include up to nine (9) crates. Figure 2a shows the setup. Figure 2b shows the crate level diagram.

Figure 2a



One TID in TS mode with TI&TD function,
Eight TID in normal TI mode

Figure 2b



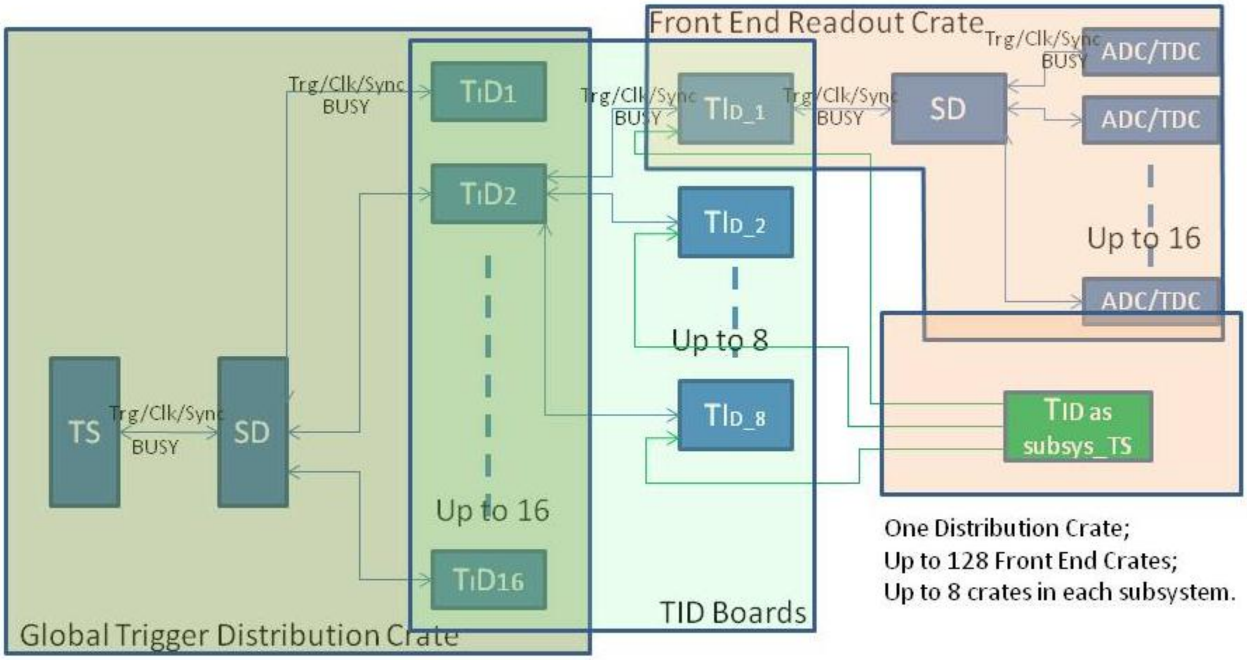
TID as TI (this crate)
and TD (up to 8 other crates)
with TS function

Commissioning/testing setup
Up to 9 front end crates in total

The TM will be the first TID boards used in various test stands. The TM FPGA firmware is different from that of a TI board. For easier trigger synchronization in the subsystem test or commissioning, the TRG/SYNC used in the TIM is similar to the TRG/SYNC sent in the optical transceiver. The TRG/SYN is looped back within the FPGA and decoded in a way similar to the TI boards. Some registers are valid on the TM only, as these registers are specific to the TS function. The TM can be used by itself in the setup. It can also drive another up to eight TIs if the setup needs be expanded.

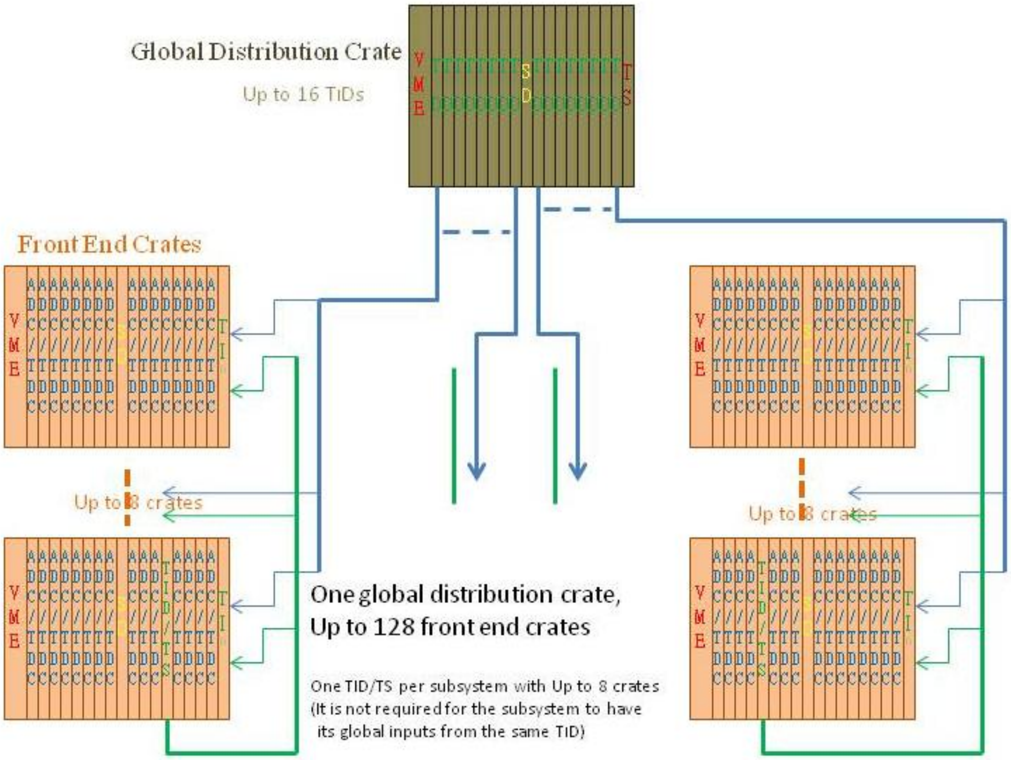
When the TID is in TI mode, it can have two HFBR-7924 modules stuffed. In this case, one can receive trigger from system TS, while the other can receive trigger from a sub-system TS. One TID can be located in any payload slots in a front-end crate, and configured as a subsystem TS. This configuration requires an extra optical transceiver on the TI module, and an extra TID board be configured as a subsystem TS with fiber outputs. Each optical transceiver module costs about $500. For a subsystem with eight crates, the extra cost is about $10K. The benefit is that the subsystem can have independent control without affecting the other subsystem. That is a lot of flexibility: independent subsystem control, independent subsystem calibration etc. This is called a luxury option. Refer to figure 3a for the setup. Figure 3b shows the crate level diagram

Figure 3a:



One Distribution Crate;
Up to 128 Front End Crates;
Up to 8 crates in each subsystem.

Figure 3b:


Global Distribution Crate
Up to 16 TIDs
Front End Crates
Up to 8 crates
Up to 8 crates
One global distribution crate,
Up to 128 front end crates
One TID/TS per subsystem with Up to 8 crates
(It is not required for the subsystem to have
its global inputs from the same TID)

The data from TID can also be sent to Signal Distribution board, in parallel with the TID to VME ROC data transfer, through a 250 Mbps (or 500 Mbps) serial link on the P0 backplane. The SD can be used to assemble events at the trigger by trigger basis. This provides a redundant data readout path.

With a mezzanine board, the TI is backward compatible with Trigger Supervisor Rev2 module. The TI with the mezzanine card will behave the same way as TI_Rev2 (produced in the year of 2001) board with added functionality.

For non-VXS crate, the TI will send trigger/clock to Row-C on VME P2 connector. With a fan out board (there is no SD in the crate, as the SD is a VXS switch slot module), the trigger, clock and SYNC are distributed to the front end data acquisition modules (CAEN VX1290 TDC for example), and the BUSY from these modules are summed in the fan out module, and sent back to the TI.

The TID (as TD) in Global trigger distribution crate will have different front panel from the TID (TI) in the front-end data acquisition crate.

It is very unlikely that the test setup (either commissioning or bench test) will have more than five crates. The firmware is designed as a universal version, that is, the firmware support the TID as TImaster and TI slave. The TI will treat HFBR#1 as trigger/clock/SYNC input, while treat HFBR#5, HFBR#6, HFBR#7 and HFBR#8 as trigger/clock/sync output. This setup can support up to five front end crates. This will be the default settings for the TI.

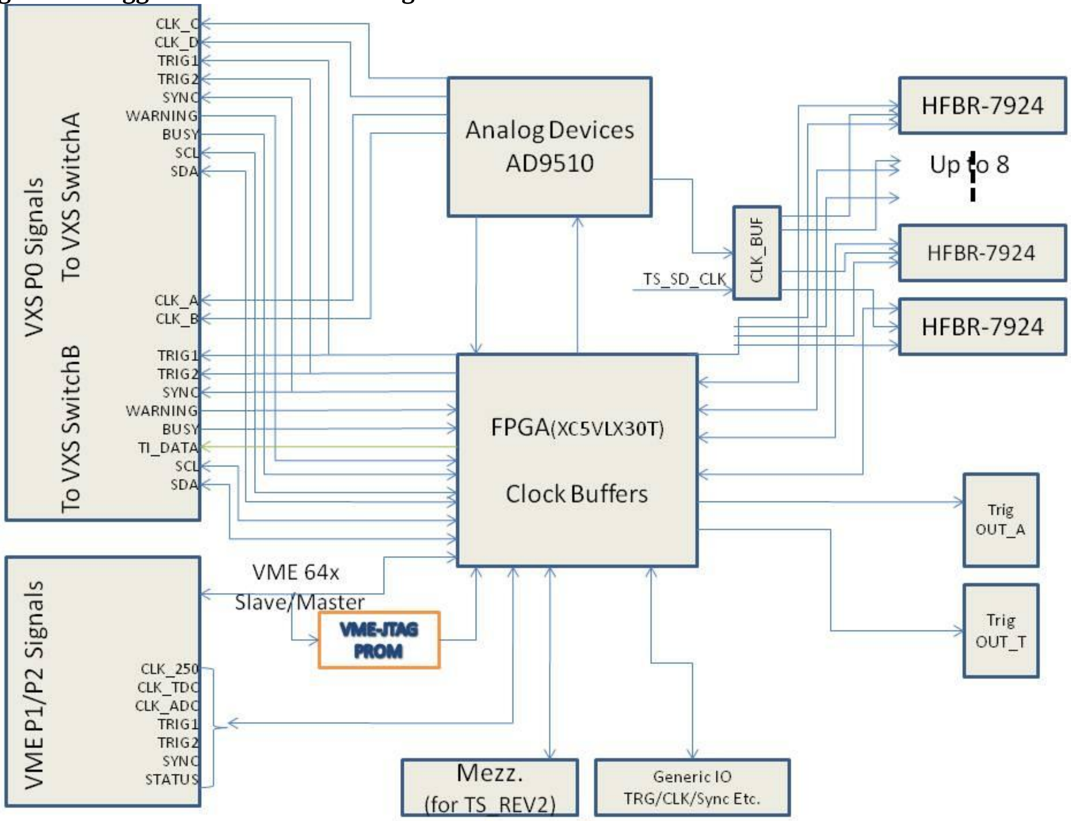
3 Functional Descriptions

3.1 General description

Figure 4 shows the block diagram of the TID module, indicating the major components used in the design. The HFBR-7924 is the multi-channel (4 Rx, 4 Tx) fiber link that the TID fans out/receives a low-jitter (<3ps

RMS) 250MHz global pipeline clock, serialized 16bit trigger words, and a fixed latency sync signal used in producing a fixed latency trigger. The AD9510 is the main clock driver and gets synchronized lower frequency clocks. The Xilinx XC5VLX30T is used to encode/decode the trigger words at 16ns, to interface with the VME, to control the working mode etc. The P0 is compatible with the VXS payload slots, which matches with GTP, CTP, SD positioned in switch slots.

Figure 4: Trigger Interface Block Diagram



3.2 Fiber links

The HFBR-7924 is the multi-channel (4 Rx, 4 Tx) fiber optic link for the TID. For the TD in the global trigger distribution crate, all the eight HFBR-7924 transceivers will be installed, so each can support up to eight front end data acquisition crates. For the TI in the front end crates and global trigger crate, One (maybe two) HFBR-7924 transceiver will be installed, to receive the trigger/clock/sync from central trigger (and subsystem trigger).

The HFBR_7924 is chosen over the HFBR-7934, because the HFBR-7924 is about $100 cheaper per piece, and there is no visible performance degradation comparing with HFBR-7934. [GU, 2010].

The first pair (Tx/Rx) is used to transfer trigger words from TD to TI, and status from TI to TD. The second pair is used to transmit the 250MHz clock from TD to TI. The third pair is used to transmit the SYNC from TD to TI. The TI to TD links on second pair and third pair are not used.

The fourth pair (Tx/Rx) is looped back on the TD for fiber length (latency) measurement. The fiber numbers #2, #3, #4, #6, #7 and #8 on TD are looped back by a short trace on the PCB between the HFBR Tx and Rx pads. The fiber#1 and #5 are looped back by the FPGA. Normally, the FPGA will connect the Rx directly to the Tx, and the extra latency caused by the FPGA is minimal (<4ns). The TD has the flexibility to use this connection when the latency measurement is not in use.

3.3: Clock Distribution

One of the TID's major functions is the pipeline clock distribution. There are five possible sources for the 250MHz clock: 'P0 connector from SD in trigger distribution crate', 'onboard oscillator', 'external clock input from twisted pair cable', 'optical fiber input from central trigger in front-end crate' and 'optical fiber input from subsystem trigger in front-end crate'. The five clock sources will be multiplexed. There will be only one 250MHz clock running on the TID.

The clock is fanned out by the MC100LVEP111 2:1:10 clock driver. On the TD, the clock from P0 is distributed directly to the optical fibers (eight HFBR-7924 modules). The extra output from the clock driver will drive the AD9510 CLK2 input and generate the onboard clock. In all the other cases, the clock will be multiplexed by MC100EP57 and go to the AD9510 CLK1 input, and the output of the AD9510 drives all the outputs.

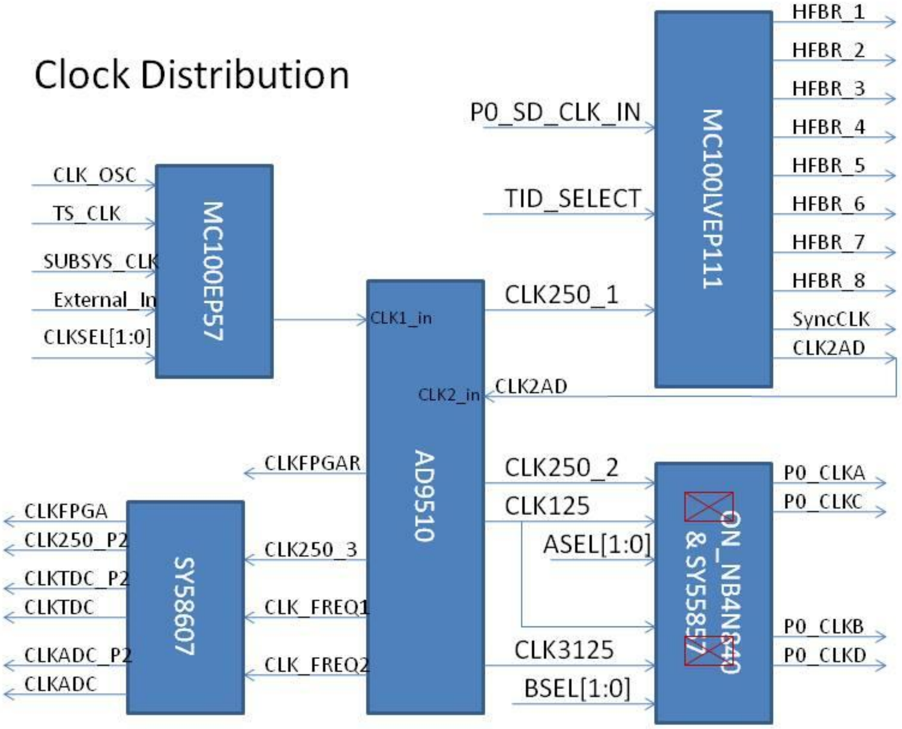
Three clocks (with frequencies of 250 MHz, 125 MHz, 31.25 MHz) are distributed to the P0 backplane. One On-Semiconductors' NB4N840M and two NB6L72 are used to switch the clocks, so that, the switch slot#A and switch slot#B can get two clocks. Each clock could be any of the three frequencies. The NB6L72 is also used as a level shifter from CML to LVPECL.

The clock is also distributed to the front panel connectors via ECL on twisted pair cables and VME P2 backplane user defined pins for VME ADC or TDC modules, which are NOT in the VXS crates.

The CAEN V1290 TDC will get a synchronized 41.67MHz clock through TID P2 connector via a fan out board in the crate, instead of the nominal 40MHz onboard oscillator frequency, because there will be too much effort involved to generate a system wide synchronized 40MHz clock, and the V1290 can be calibrated to accept the 41.67 MHz clock.

An eight-bit on board switch will be used to select the clock sources except for the AD9510, which will be configured by the FPGA firmware on power up and by demand.

Figure 5 shows the TID clock distribution diagram:

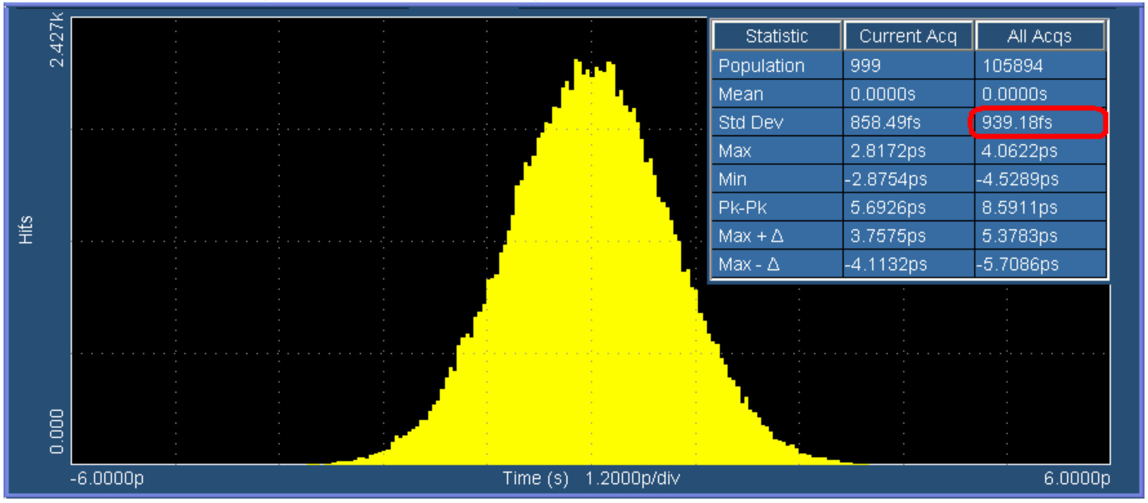


The clock is distributed in (LVP)ECL levels to keep the low jitter and low skew (faster propagation). The LVDS clock is used to drive the FPGA for easy termination.

The global 250MHz clock signal received over the fiber runs the L1 trigger pipeline electronics and nearly all of the front-end modules. Several front-end modules require this clock to have low-jitter and so the clock signal is buffered with components that contribute low-jitter, including the fiber driver and receiver. Figure 3c shows a measurement of the jitter contribution from the fiber driver/receiver pair, including a small increase in clock jitter (roughly 1.6ps additive jitter from the fiber driver/receiver with 150m of fiber between them) by GU et al. [(GU, 2010)]. Careful component selection, signaling, and layout techniques are employed to minimize overall clock jitter.

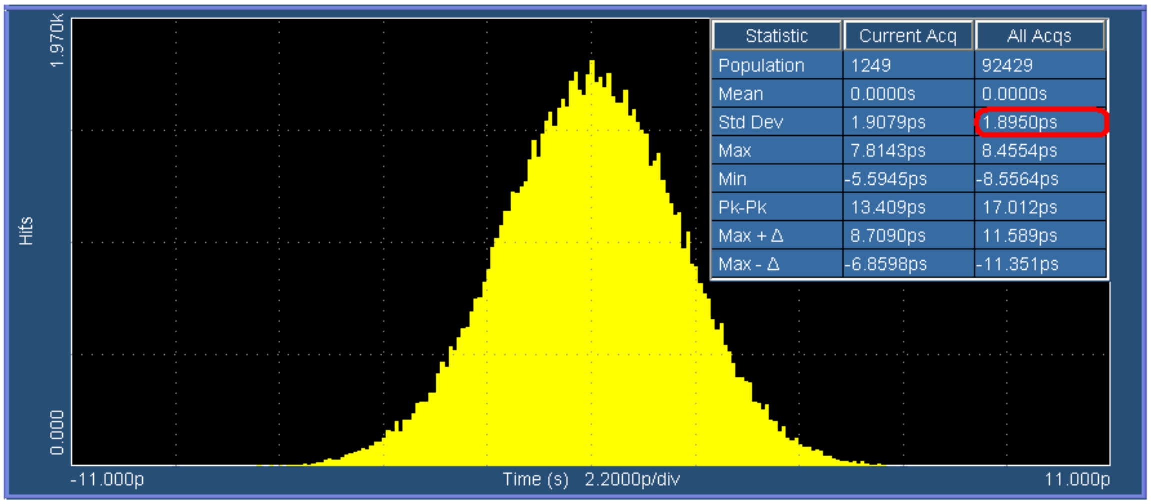
Figure 6: Global Clock (250 MHz) Jitter

Reference 250MHz Clock (before fiber modules+150m)



Statistic	Current Acq	All Acqs
Population	999	105894
Mean	0.0000s	0.0000s
Std Dev	858.49fs	939.18fs
Max	2.8172ps	4.0622ps
Min	-2.8754ps	-4.5289ps
Pk-Pk	5.6926ps	8.5911ps
Max + Δ	3.7575ps	5.3783ps
Max - Δ	-4.1132ps	-5.7086ps

Reference 250MHz Clock (After fiber modules+150m)

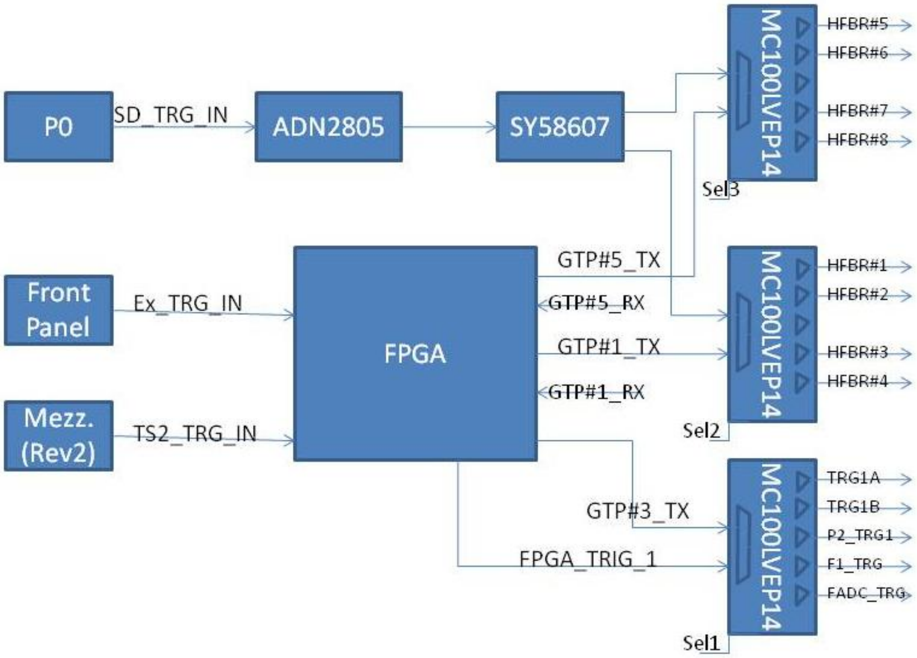


Statistic	Current Acq	All Acqs
Population	1249	92429
Mean	0.0000s	0.0000s
Std Dev	1.9079ps	1.8950ps
Max	7.8143ps	8.4554ps
Min	-5.5945ps	-8.5564ps
Pk-Pk	13.409ps	17.012ps
Max + Δ	8.7090ps	11.589ps
Max - Δ	-6.8598ps	-11.351ps

3.4 Trigger distribution:

Figure 7 shows the trigger distribution on TID. When in TD mode, the TID gets trigger from SD through P0 connector. The signal is cleaned up by ADN2805 and fanned out to the eight optical links (HFBR-7924). When in TI mode, the TID receives the trigger signal by the optical fiber and decoded by the FPGA. The trigger is sent to the fan out buffer then to the P0 backplane and other connectors. The TID can be in TS mode (as TM), which takes the trigger from the front panel input and send to the SD in gigabit serial mode (encoded), and it can also sent to the fiber in encoded format, though the HFBR#1, #2, #3 and #4 are identical, and HFBR#5, #6, #7 and #8 are identical. (Surely, these two groups can be the same too). The independent choices of the trigger enable the versatile functions of the TID to be TS, TI and TD, or a combination of these functions (as a TM).

Figure 7, Trigger distribution



3.5: Encoded Trigger Word

A 1.25Gbps serial link operating over the fiber is used for distributing a 16bit trigger word every 16ns. There is also a link going in the opposite direction, allowing status words to be sent back to the trigger distribution crate. The 16bit trigger words are decoded as follows (TS->TD->TI flow):

Trigger strobe word – generated by the TS in response to the acceptance of a level 1 trigger. Upon receipt, the TI drives prompt trigger signals to the front-end modules. The TS transmits these with fixed latency relative to the accepted trigger. This word is distributed every 16ns, so the trigger is distributed every 16ns. It is possible to add the timing information in the word to distinguish which quadrant of the 16 ns period the trigger is generated to be fully compatible with the 4ns pipeline design architecture. The TI can distribute trigger signal in 4ns precision. This could potentially reduce the FADC readout window width, and reduce the event size.

Trigger content word – additional information about the trigger for use by the ROCs. It is queued in a FIFO and sent in any frame not used by a trigger strobe word. The TI matches the trigger strobe and trigger content words by the order of their reception.

Control Word – establish synchronization, request status, or other command (VME trigger for example). They can be queued in a FIFO and sent in any frame not used by a trigger strobe word or trigger content word.

Master Time Word – to fully use the trigger link, bits [13:2] of the TS time is transmitted whenever no other word types are available. By continuously receiving bits [13:2] of the TS time, each TID can promptly detect if its frontend crate has lost global synchronization (i.e. compare the global time with its own time). Otherwise, the loss of synchronization could only be detected at the event building stage. The continuous transmission of ‘known’ (i.e. predictable) data also allows one to monitor the integrity of the link.

This table shows the format of the trigger word.

Bit13	Bit12	Word Type	Meaning of Bit[11:0]
0	0	Time	Lower 12 bits of TS time
0	1	Control	Control or Command
1	0	Trigger Strobe	Trigger type/Trigger quadrant

1	1	Trigger Content	Additional Trigger data

Bits [15,14] are used for error detection for all word types, this could be simply one parity bit and one TS busy bit. For now, the bit14 is the reverse of bit 15, which is word parity.

The Trigger content word includes a trigger counter word. The TID can use this content word to check its synchronization if any trigger is missing by the TID.

The following defines the data format for the opposite direction of the link (TI->TD->TS flow):

Bit [15] parity bit;
Bit [14:12] 000 right now;
Bit [11] TI (including the front end crate) BUSY: ‘1’ = busy, ‘0’ = not busy;
Bit [10] Trigger_1 acknowledge;
Bit [9] Trigger_2 acknowledge;
Bit [8] one block of triggers received;
Bit [7] ROC readout acknowledge (one block of trigger is readout and acknowledge by ROC);
Bit [6:0] status.

3.6: Fixed Latency SYNC

The SYNC signal is a 250Mbps serial line operating in synchronous mode. This serial link allows a 4bit command to be sent at chosen 4ns points in time. SYNC is synchronized to the master clock CLK250 and is sampled every 4ns cycle. The line is considered to be idle when more than 4 samples in a row are read ‘1’. A command is sent between idle times by sending first a ‘0’ followed by the 4bits that comprise the command, LSB first. After the command has been sent a final ‘1’ is sent so that the line will return back to the IDLE state. The encoding portion of this serial protocol is performed on the TS. Since the TD distributes this serial line over the fiber module, additional encoding (Manchester) is performed to balance the 1’s and 0’s of the line and to keep the maximum run length of the signal below the requirements of the fiber module. The TID decodes the SYNC signal (Manchester and command). Careful design in minimizing SYNC to the distributed master CLK250 skew guarantees a fixed latency link.

The SYNC is fiber delay adjusted on each TI. The fiber latency is measured using the fourth pair of the fiber. The SYNC is delayed so that all the TI modules will execute the SYNC command at exactly the same time (within the skew of the global 250MHz clock distribution).

The SYNC link is used in conjunction with a synchronous FIFO to enforce a fixed latency on the serial trigger link. The TD uses LVPECL buffers to fan out the trigger signal and the Sync signal, which is encoded (Manchester encoding) in the FPGA, to the HFBR_7924 transceivers. In the TI, the trigger word is clocked into a FIFO using the FPGA built in MGT transceivers and the user clock, which is the same as the external 62.5MHz clock. Data words are clocked out of the FIFO using a 62.5MHz clock derived from (and in phase with) the system CLK250. At startup the FIFO is reset (0 words) and reading the FIFO is disabled. No words are written into the FIFO since the TS is not yet transmitting data words on the trigger link (i.e. received data valid signal is not asserted). Acceptance of triggers by the TS is also disabled. The TS starts transmission (time words) on the trigger link, and after a fixed number of 62.5MHz clock cycles issues a trigger start command on the SYNC line. In response to the trigger start command, the TI enables continuous readout of the FIFO. There must always be a non-zero number of words in the FIFO to maintain a fixed latency link. This will be true if the number of words pre-filled into the FIFO x 16 ns is greater than the latency uncertainty of the link. In the case of the MGT, several words (e.g. 3 or 4) are enough when the latency is set to minimum as the elastic buffer is not necessary as all the clocks are the same or derived from the same 250MHz clock (no clock frequency difference). The TS must always be transmitting valid data to maintain the fixed latency of the link. This is illustrated in figure 8:

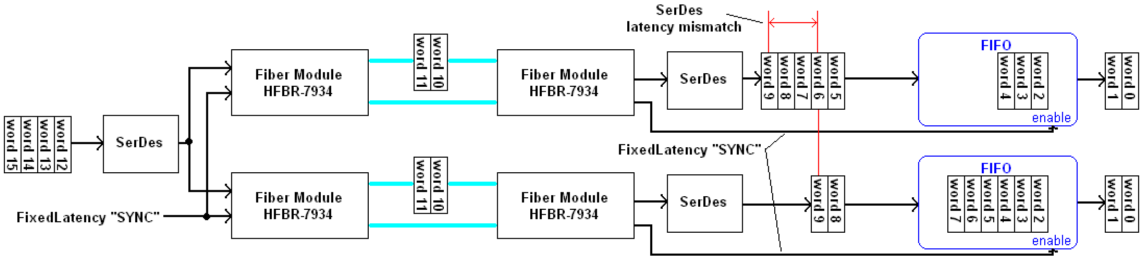
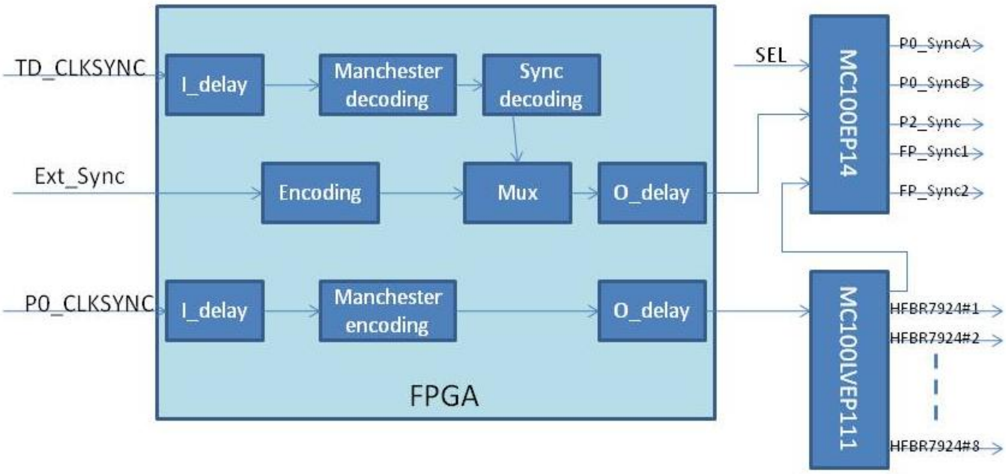


Figure 8: Illustration of the Trigger synchronization process

The SYNC link is also useful in ensuring that the lower frequency clocks derived in the TID from the distributed system clock (CLK250) have the same phase across all TI modules in the front-end data acquisition system. At startup, the TS issues a SYNC command CLKRESET. This resets the clock distribution chip (AD9510) in each TI on the same CLK250 edge, assuring that the lower frequency clocks (125MHz, 62.5MHz, 41.67MHz and 31.25MHz) are in phase across the entire system. This command is sent before the TID sync command. The delay between them is determined by the maximum MGT reset recovery time, as the MGT clock is changed (AD9510 clock reset) during clock reset. The time is several milliseconds.

Figure 9 shows the block diagram of the SYNC distribution on the TID board:



3.7 VME interface

The TID is a VXS payload slot board. It is compatible with VME64x backplane. Normally, it is a VME slave board, with interrupt capability.

The TID can also be a master VME board. It supports single level bus request (BR3, level 3) only, as we do not expect many boards to be a VME master in the crate.

For simplicity, three kinds of VME address modifier codes are implemented. (1), User defined address modifier. (0x19,0x1A, 0x1C and 0x1D) This is similar to the A24 address modifier. It is used to load the PROM by the emergency logic. (2), Standard A24 address modifier. This is used to readout the registers on the FPGA, slow controls of the TID peripherals, and to request data from other boards in the crate when in master mode. (3), A32 BLT data transfer. This is used to transfer data to the ROC (Read Out Controller). This is implemented the same as other ADC/TDC board, so the ROC needs only one read to get all the front end boards' data out for higher efficiency.

3.8: The Xilinx PROM programming.

The Xilinx XCF32P PROM is used to program the FPGA. It can save two different versions of the FPGA (XC5VLX30T) firmware when used in non-compression mode. It can save four different versions of the firmware when bit stream compression is used, in which case, only the slave serial and slave SelectMAP modes are supported. The PROM is programmed using VME with emergency logic decoding. It can be addressed in the VME64x crates by its geographical address. If it is in the crate without geographical address, only one TID in the crate should be addressed as geographical slot#0. To avoid conflict with other VME addressing, the user-defined address modifiers are used for the PROM loading. The emergency logic supports A24 user defined address modifier codes: 0x19, 0x1A, 0x1D and 0x1E (Similar to 0x39, 0x3A, 0x3D and 0x3E). Out of the data, bit[1] is used for TDI, bit[0] is used for TMS, and all the other bits are unused. This approach is fully tested in CMS on LHC. The emergency loading is tested. With M6100 controller, the 32 Mbit PROM (XC32P) can be loaded in less than five minutes. The emergency loading provides VME remote firmware re-loading and broadcast firmware loading even if the FPGA is not working. One 33 MHz (25MHz on earlier revision of TID) on-board oscillator is used to program the FPGA in slave mode, and used by the FPGA for slow control, for example, the VME to AD9510 serial control engine.

The PROM can also be programmed by the on-board JTAG connector and VME-JTAG engine (after the FPGA is programmed and working) in the FPGA. The JTAG engine in the FPGA provides VME remote firmware loading when the FPGA is working with more efficient VME data transfer (32 bits versus 1 bit).

3.9: Status passing

The TID can merge the status together and pass on to upper level. Specifically, the TI can merge the status from the CTP and SD via P0 backplane and pass on to TD in the global trigger/clock distribution crate via optical links. The TD in trigger distribution crate can merge the status from up to eight front-end crates and send to SD (to TS) via P0 backplanes. Right now, only the BUSY is defined as status. We have the capability to add a less severe state, WARNING, to the status.

The TI in the front end crate can send its timing information back to the TD in the trigger distribution crate. This information can be used to check the system synchronization status. Here is how this will work.

On the start of the run, a global sync command will reset all the counters synchronously. Each TID will have its own clock counter, that count how many clock cycles since the sync reset. As the trigger is synchronized on all the TIs, all the TI should receive the same trigger at the same clock cycle. The TI in the front end crate will send the clock counter, recorded when it receives the trigger, to the TD in the distribution crate. This signal may be received asynchronously as a status word (ref to section 3.5), but all the eight words should match on the TD. This can also serve as trigger acknowledge from the front end crates to the distribution crate. This transfer could be pre-scaled to every N (N is settable by VME) triggers. If the TID received un-matching numbers from front-crate, it is most likely a trigger loss if the difference is large; it is most likely a clock loss if the difference is small. In this way, the trigger synchronization can be checked at the crate level.

3.10: Serial data communication with SD

The TID can send data to the SD via a 250Mbps link, (it is possible to increase it to 500 Mbps using DDR techniques). This is implemented using the Xilinx SelectIO standard differential IO pin pair. In this case, the SD can be implemented as a data concentrator card to collect data from the VXS crate (the payload modules include FADC, FTDC, TID, etc). The TID will send data to SD on every trigger (event). This is another data readout path in addition to the standard VME readout. The maximum data rate is 50 MB/sec per slot. The full crate can reach up to 900 MB/sec assuming all 18 payload slots are used. This is the pilot implementation of hardware data acquisition system based on CMS/LHC experiences. The data from SD is event based, and there is no need to re-format the data as needed by the VME readout (block readout is used for high efficient usage of the VME bus data transfer).

The SD can also send data to TID using this link. The direction of the data link depends on the firmware (TID and SD) implementation.

3.11: legacy compatibility

When the TID is in TI mode, a mezzanine board is used to interface with the TS_rev2 module directly for backward compatibility, which may still be used in the experiment halls. The Mezzanine board has the same connector as the TI_rev2 board (matching with Trigger Supervisor rev2). With the mezzanine board plugged in, the TID will behave like a TI_rev2 board (produced in 2001) to interface with TS_rev2 board.

3.12 Other functions

The TID has a generic IO connector with up to 34 pins, which can accept one external trigger input, and six trigger input codes. It can also accept external clocks. Using these, some of the Trigger Supervisor functions can be implemented in the TID. The TID can serve as a subsystem trigger supervisor board. A nine crates setup can be implemented by TIDs for (sub)system commissioning and subsystem test setups.

4. Specification Sheet

4.1 Mechanical

- Single width VITA 41 Payload Module. As a TD, it will be positioned in the PP01 to PP16 in global clock/trigger distribution crate; as a TI, it will be positioned in PP18 in front-end data acquisition crate and global trigger crate; it can also be plugged into any slots in standard VME crates without VXS. In system commissioning, it can be in PP18 and support up to 9 crates with some TS functions. In luxury setup (optional), it can be in any payload slots (except PP18) of the subsystem crates, and serve as a subsystem Trigger Supervisor, which can group up to 8 crates together as a subsystem.

4.2 High speed serial P0 and P2 inputs:

- BUSY LVDS signals on P0;
- BUSY ECL signals on P2;
- I^2C to VXS Switch A & B;
- Clock, trigger and sync signals from SD when in trigger distribution crate.

4.3 High speed serial P0 and P2 outputs:

- Any two of these clocks (250MHz LVPECL Clock, 125MHz LVPECL Clock, and 31.25MHz LVPECL Clock) to Switch slot#A and Switch slot#B.
- Trig 1 LVPECL Trigger Signal
- Trig 2 LVPECL Trigger Signal
- Sync LVPECL Trigger Signal
- 250/500 Mbps data (LVDS) to SD at per event basis

4.4 Front panel inputs and outputs:

- 250MHz ECL Clock Input & Output
- Trig 1 ECL Trigger Input & Output
- Trig 2 ECL Trigger Input & Output
- Sync ECL Trigger Input & Output
- Busy ECL Input & Output
- Up to eight HFBR-7924 transceivers for TD in distribution crate; up to two HFBR-7924 transceivers for TI in front-end data acquisition crate; up to eight HFBR-7924 transceivers for TM or subsystem TS in system test or subsystem commissioning.

4.5 Fiber channel signals:

- SYNC Fixed Latency Link

    - 250Mbps Serial Communication
    - Manchester Encoded
    - SYNC to CLK skew variation adjusted at FPGA receiver.
- TRIGLINKTX/TRIGLINKRX
    - 1.25Gbps Trigger Word Line
    - Provides 16bit parallel data every 16ns
    - A BUSY status word in the opposite direction.
- CLK
    - 250MHz Clock <3ps RMS Jitter

4.6 Indicators: Front Panel:

- Bit 1 (close to the PCB): FPGA programmed and the clock (DCM locked) is ready;
- Bit 2: VME DTACK, VME activity;
- Bit 3: Trigger_1 is sent out;
- Bit 4: HFBR#1 MGT Rx error;

On board:

- Power OK near each regulator or DC-DC converter;
- FPGA program DONE;
- Fiber optical transmitter FAULT and receiver SIGNAL_DETECTED near each HFBR-7924 module.

4.7 Programming:

- VME to JTAG A24D32 with user defined AM (Address Modifier) for remote loading with redundant On board JTAG connector;
- Custom VME to JTAG engine implemented in the FPGA using A24D32 for firmware loading;
- Up to four revisions of the firmware can be stored in the PROM simultaneously.

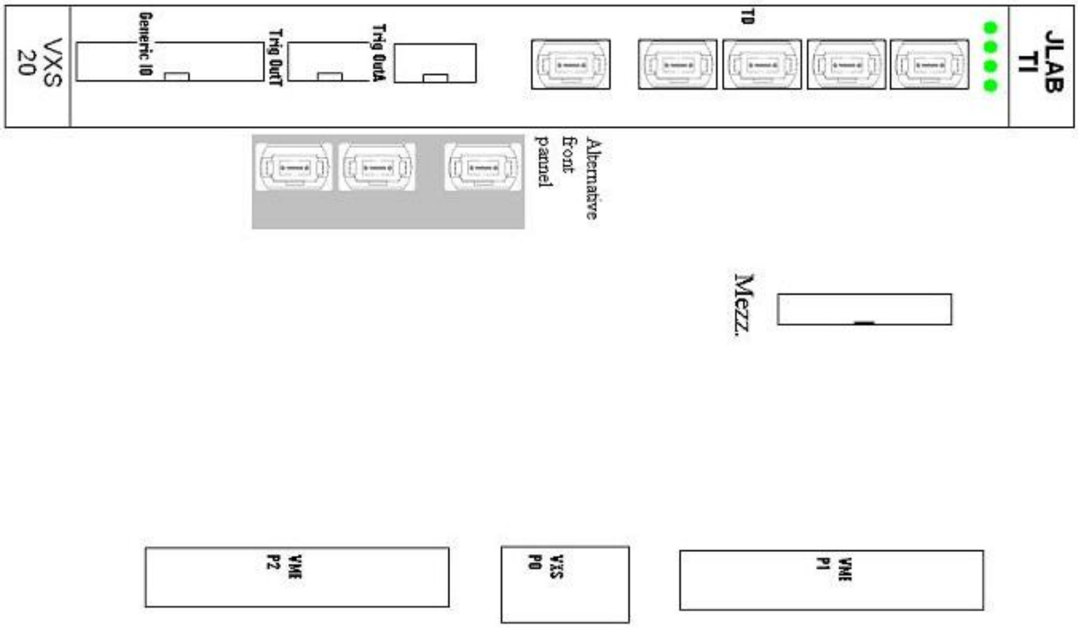
4.8 Power requirements:

- +5v @ 4 Amps; -12V @ 0.25 Amp; +12V @0.25 Amp (From Backplane)
- Optional DC-DC converters for +3.3V, and Local regulators for other required voltages: +1.0V, +1.2V, +1.8V, +2.5V, +3.3V, and -5V.

4.9 Environment:

- Forced air cooling: Weiner standard VME64x/VXS
- Commercial grade components (0-75 Celsius)

Figure 10 shows the front panel and onboard connectors:



5 TID operation procedures:

The TID needs be properly set, and plugged into the proper crate and slot. Damage may happen to the TID, the crate, or other PCBs in the crate if the right procedure is not followed.

5.1 TID Power supply:

The TID can use +3.3V directly from VME64x crate. It can also generate its own +3.3V supply by a DC-DC converter. Another dedicated +3.3V DC-DC converter can be used to power the optical transceivers (HFBR-7924). The HFBR_7924 can also be powered by the main +3.3V supply for the board. Proper settings are needed to avoid damage to the board or backplane.

If the dedicated +3.3V DC-DC converter is to be used to power the HFBR-7924:
(1). Make sure that the DC-DC converter LTM4604, UP01, is stuffed.
(2). Inductor, LP3 is removed.
If the TID main +3.3V power is used to power the HFBR-7924:
(1). Make sure that either UP1_NL is NOT stuffed,
(2). Inductor LP3 is stuffed.

If the VME64x crate +3.3V power is used for the TID:
(1). The fuse, FP1 is stuffed;
(2). The DC-DC converter UP1 is removed.

If the VME64x crate +3.3V power is not used for the TID:
(1). The fuse, FP1 is removed;
(2). The UP1 is stuffed.

5.2 Hardware setting (Switch etc.):

When the TID is in TD mode, it receives signals from P0 connector; when the TID is in TI mode, it drives signals to the P0 connector. This is set by three pairs of resistors or capacitors. If the 0 Ohm resistors are used, the signals are DC coupled, if 0.047uF capacitors are used, the signals are AC coupled. When in TD mode, stuff C0001/C0002, C0003/C0004, and C0007/C0008; when in TI mode, stuff C0011/C0012, C0013/C0014, and

C0017/C0018; when in TM mode, used for system commissioning, stuff as TI; when used as a subsystem trigger supervisor, stuff as TD. This will avoid driving conflict with SD.

There are four 8-bit switches on the TID, and marked as: S1, S2 (VME address space setting switches), SC01 (TID mode setting) and SC1 (TID clock setting). Some switches are LVTTL, some are LVPECL. When the switch is ON, the switch is LOW, (0V for LVTTL, and 1.4V for LVPECL); when the switch is OFF, the switch is HIGH, (3.3V for LVTTL, and 2.5V for LVPECL). Here are the details of the switch setting:

5.2.1. SC1 setting:

Bit1: LVPECL, open=high, trigger_1 source selection. When low, the trigger_1 source is FPGA MGT_112 output (serialized trigger data); when high, the trigger_1 source is standard FPGA differential output (pulse);

Bit2-5: LVTTL, open=high, P0 CLK_A, CLK_B, CLK_C, CLK_D selection. Clk_A is the same as CLK_C and CLK_B is the same as CLK_D. The clocks are selected in two stages:

Switch \ clock out	Clock_X	Clock_Y
Bit3=0; bit5=0	250	31.25
Bit3=1; bit5=0	250	125
Bit3=0; bit5=1	125	31.25
Bit3=1; bit5=1	125	125

Switch \ clock out	Clock_A, Clock_C	Clock_B, Clock_D
Bit2=0; bit4=0	Clock_X	Clock_X
Bit2=1; bit4=0	Clock_X	Clock_Y
Bit2=0; bit4=1	Clock_Y	Clock_X
Bit2=1; bit4=1	Clock_Y	Clock_Y

Bit[7:6]: LVPECL, open=controlled by the FPGA, closed = LOW: TID 250MHz clock source selection. When bit7=0&bit6=0, on-board oscillator is selected; when bit7=1&bit6=0, TD input from optical transceiver #1 is selected; when bit7=0&bit6=1: subsystem clock input from optical transceiver#5 is selected; when bit7=1&bit6=1: front panel generic connector inputs is selected; For FPGA control, refer to A24 register offset 0x08 bit(13:12).

Bit8: LVPECL, open=high, TID connectors' sync signal source selection. When low, Sync_reset is selected; when high, Manchester encoded SYNC signal is selected.

5.2.2 SC01 setting:

Bit[2:1]: LVTTL, open=high. Firmware revision selection. When Bit2=0&Bit1=0, select firmware Rev0; when Bit2=0&Bit1=1, select firmware Rev1; when Bit2=1&bit1=0, select firmware Rev2; when Bit2=1&Bit1=1, select firmware Rev3. If the program bits are not compressed, the PROM XCV32P can only fit two revisions of the firmware.

Bit[8:3]: LVTTL, open=high. FPGA function control. These switches are used to control the functions of the FPGA to match with the requirement of the TI/TD/TS mode selection.

Bit[4:3]	Board function
0 0	TD only, simplest mode
0 1	Subsystem TS; receives clock from P0 as TD, generate trigger/Sync as TS, and fans out trigger/Sync as TD
1 0	TI mode, could have TS functions
1 1	TM mode, Trigger Master as in standalone setup

For now, the Bit(4:3) are decoupled from Bit(2:1). The Bit(2:1) controls the firmware revision, while the Bit(4:3) is a firmware variable. If Bit(4) = 1, the CLK1 input of AD9510 is selected, which is the mux of four independent 250MHz clocks. If Bit(4)=0, the CLK2 input of AD9510 is selected, which is the clock from P0 backplane. If Bit(4)=1 and Bit(3)=0, the FiberMode=1, which will power down the HFBR#2, #3, #4, #6, #7 and #8. When the FiberMode=1, the TID is in pure TI mode.

5.2.3 S1 setting:

Bit[1:3]: These three bits are used to control the OUTPUT(5:2) of the front panel 34-pin connector. The switches are used to multiplex the eight FPGA internal monitoring sources (32 signals) on the four output pins.
Bit[4]: Add an extra word if the total number of words in a block is odd. ‘1’ to enable, ‘0’ to disable;
Bit[8]: keep high, for TID_rev1, this pin is used as IACK input to the FPGA;
Bit[8:7]: keep high, for TID_rev2, these two pins are used as clock source selection output from the FPGA;
Bit[5:6]: not used.

5.2.4 S2 setting:

Bit[1:5]=A[23:19], VME address space in A32 or A24 mode. Be careful about the bit order. When in VME64x crate, these addresses should be set the same as its geographical address.
Bit6: LVPECL, open=high. The HFBR#1, #2, #3 and #4 trigger source selection. When low, the source is P0 (from SD), when high, the source is FPGA GTP_116.
Bit7: LVPECL, open=high. The HFBR#1_8 fan out clock source selection. When low, the fan out source is P0 (from SD), when high, the source is on-board clock manager AD9510. This should be consistent with the bit(4:3) of SC01 switch setting.
Bit8: LVPECL, open=high. The HFBR#5, #6, #7 and #8 trigger source selection. When low, the source is P0 (from SD), when high, the source is FPGA GTP_114.

5.3 Software setting:

After the board is properly set, and plugged in the right slot, some software setting needs be applied for the board to work. Some parts of the board needs be powered down to reduce the power consumption. The FPGA GTP transceivers will be automatically powered depending on the mode setting (TI/TD).

The delay settings will be automatically loaded by the Serial Flash Memory (SFM) on FPGA re-programming in real experiment. The parameters (delay etc.) can be set by the VME, and stored in the SFM. We expect the parameter to be stable, but adjustment may be necessary when moving the board (different fiber connection etc.)

In the test setup and commissioning test, some delay parameters needs be manually set.

6. VME Programming Requirements (This part will be updated as the firmware develops)

There are three categories of Address Modifier codes are supported on the TID: the user-defined codes (A24) for emergency firmware loading; Standard A24 for FPGA register read/write and slow control; A32 block transfer for VME data readout.

6.1 VME to JTAG emergency loading:

The AM[5:0] user defined codes are used for this logic. This works even before the FPGA is programmed and working. It is almost the same as A24D32 mode. The valid AM codes are: 0x19, 0x1A, 0x1D and 0x1E. These AM codes are user defined, and similar to the AM codes 0x39, 0x3A, 0x3D and 0x3E.

The valid address bits are A[31:24] do not care; A[23:19]=GA[4:0] for VME64x crates, or A[23:19]=0 for non-VME64x crates; A[18:2]=b’00011111111111111.

Data bit[1] is TDI; data bit[0] is TMS.

For example, if the board is in slot#5 (that is ~GA(4:0)= 11010), you need write to A(23:0)=0x28fffc. If data(1:0)=00, both TMS and TDI will be low; if data(1:0)=01, TMS is high, TDI is low; if data(1:0)=10, TMS is low, TDI is high; if data(1:0)=11, both TDI and TMS are high. The normal A24 address should try to avoid this address (0x0fffc).

A more advanced example: Instruction register shift (8-bit, shift in 0x5a) starting from/end up at the 'reset idle' mode: 14 consecutive writes to the address 0x28fffc with AM=0x19, 1a, 1d or 1e, the data are 1, 1, 0, 0, 0, 2, 0, 2, 2, 0, 2, 1, 1, 0 respectively.

Data	1	1	0	0	0	2	0	2	2	0	2	1	1	0
TMS	H	H	L	L	L	L	L	L	L	L	L	H	H	L
TDI	0x	0x	0x	0x	0	1	0	1	1	0	1	0	0x	0x

- "TMS H" means logic High, "TMS L" means logic Low, "TDI 0" means 0 or Low, "TDI 1" means 1 or High, and "TDI 0x" means DO NOT CARE by the JTAG, but the set value is 0.

6.2 Configuration Registers:

A24D32 are used for register read/write. Similar to the emergency loading logic, the base address is determined by the Geographic Address in VME64x crate, and external switch for non-VME64x crate. That is, A[23:19]=GA[4:0], or SW[5:1].

Address offset: 0x00000 (R/W): Trigger/Data Acquisition/Sync setting:
- Bit 7-0: Crate ID;
- Bit 15-8: Block size, that is the number of triggers per block;
- Bit 23-16: Trigger input source enables, '1' enable, '0' disable;
  - Bit 16: P0 trigger input;
  - Bit 17: HFBR#1 trigger input;
  - Bit 18: TS loopback trigger input;
  - Bit 19: Front Panel trigger input;
  - Bit 20: VME trigger;
  - Bit 21: Front Panel Trigger Codes (as Supervisor) inputs;
  - Bit 22: TS_rev2 trigger input;
  - Bit23: Random Trigger.
- Bit 28-24: Sync input source enables, '1' enable, '0' disable.
  - Bit 24: P0 sync input;
  - Bit 25: HFBR#1 sync input;
  - Bit 26: HFBR#5 sync input;
  - Bit 27: Front panel sync input;
  - Bit 28: TS loopback SYNC enable
- Bit 29: if '1', two block placeholder words are enabled; '0' disabled.
- Bit 31-30: Event format control:
  - 00: Shortest words per trigger;
  - 01: The TI timing word is enabled;
  - 10: The TI status word is enabled;
  - 11: The TI timing word and status word are enabled;

Address offset: 0x00004 (R/W): HFBR-7924 ENABLE. Bit description:
- Bit 0: '1' enable HFBR#1, '0' disable HFBR#1; ('disable' means 'power down')
- Bit 1: '1' enable HFBR#2, '0' disable HFBR#2;
- Bit 2: '1' enable HFBR#3, '0' disable HFBR#3;
- Bit 3: '1' enable HFBR#4, '0' disable HFBR#4;
- Bit 4: '1' enable HFBR#5, '0' disable HFBR#5;

Bit 5: ‘1’ enable HFBR#6, ‘0’ disable HFBR#6;
Bit 6: ‘1’ enable HFBR#7, ‘0’ disable HFBR#7;
Bit 7: ‘1’ enable HFBR#8, ‘0’ disable HFBR#8;
Bit 15-8: VME readout related setting:
Bit 12, 14, 15 not used;
Bit 8: ‘1’ I2C device address 0x1101xxx, ‘0’ I2C device address 0x0000xxx;
Bit 9: ‘1’ token_in high, ‘0’ token_in low;
Bit 10: ‘1’ first_board true, ‘0’ first_board false;
Bit 11: ‘1’ last_board true, ‘0’ last board false;
Bit 13: ‘1’ Enable IRQ, ‘0’ disable the IRQ;
Bit 16: ‘1’ enable the Switch Slot #A BUSY input, ‘0’ disable;
Bit 17: ‘1’ enable the Switch Slot #B BUSY input, ‘0’ disable;
Bit 18: ‘1’ enable the VME P2 BUSY input, ‘0’ disable;
Bit 19: ‘1’ enable the FTDC front panel BUSY input, ‘0’ disable;
Bit 20: ‘1’ enable the FADC front panel BUSY input, ‘0’ disable;
Bit 21: ‘1’ enable the Front Panel BUSY, which is the same as TsRev2 busy;
Bit 22: ‘1’ Use P2 BUSY input as trigger1 input (useful and valid for TD only);
Bit 23: ‘1’ enable TS feed_back BUSY, ‘0’ disable the busy. (this bit is useful in TM mode)
Bit 24-31: HFBR #1-8 BUSY enables: ‘1’ enable the HFBR BUSY input, ‘0’ disable;

Address offset: 0x00008(R/W): Sync_Interrupt registers
Bit 7-0: Interrupt ID;
Bit 10-8: Interrupt level, the default is level 1;
Bit 11: not used;
Bit 13:12: software bit switch to control the TI board clock source.
Bit[13:12] = 00: oscillator clock;
Bit[13:12] = 01: HFBR#5 clock input; (not valid for current setup)
Bit[13:12] = 10: HFBR#1 clock input;
Bit[13:12] = 11: Front panel 34-pin connector clock input.
Bit 21-16: Individual GTP input bits enable. For now, six bits for the six TS input codes.
Bit 31-24: TS trigger inhibit threshold (in the unit of event blocks).

Address offset: 0x0000C (R/W): Trigger delay registers
Bit 7-0: Trigger_1 delay in 4ns steps;
Bit 15-8: Trigger_1 pulse width: (bit[12:8]+1)*4ns, Bit[15:13] not used;
Bit 23-16: Trigger_2 delay in 4ns steps;
Bit 27-24: Trigger_2 pulse width: (bit[27:24]+1)*4ns;
Bit 31-28: External trigger input prescale. Scale factor is $2^{\mathrm{Bit}[31:28]}$.

Address offset: 0x00010 (R/W): A32 control registers
Bit 0 (r/w); ‘1’ enable Bus_Error_En, so the block read can be terminated by event block trailer;
Bit 1; ‘1’ en_token_in is true, ‘0’ en_token_in is false;
Bit 2; ‘1’ enable ‘Multi-board’ readout, ‘0’ disable ‘Multi-board’;
Bit 3; ‘1’ enable en_A32m, ‘0’ disable en_A32m;
Bit 4; ‘1’ enable en_A32, ‘0’ disable en_A32;
Bit 13-5: Address Max;
Bit 22-14: Address Min;
Bit 31-23: A32 Base address;

Address offset: 0x000XX (XX is between 0x14 and 0xFC): Status and timing registers
Bit 31-0 (r/w): to be assigned (or as assigned as following).

Address offset: 0x00014 (R): DAQ status registers
Bit 31-24 (r): Number of blocks in the DAQ system READY to be read out.
Bit 23-16 (r): Number of events for the current block (start from 0)

Bit 15-0 (r): Number of blocks in the DAQ system. This can be used to control the event data readout. If the number of blocks has changed, there are blocks of data to be read out.

Address offset: 0x00018 (R): Fiber latency measurement result

Bit 31-23: latency data in 4ns steps

Bit 22-16: Delay in the IODelay, in 5000/64=78.125ps steps

Bit 15:0: Delay in the carry chain, two bits per slice, (or two mux per bit)

Address offset: 0x0001C: Fiber SYNC delay and phase alignment

Bit 31-24 (r/w): HFBR#5 sync delay;

Bit 23-16 (r/w): (read) on TI: HFBR#5 IODelay, for phase adjustment;
(write) On TM: delay for TS sync loopback

Bit 15-8 (r/w) HFBR#1 Sync delay (in 4ns steps);

Bit 7-0 (r): HFBR#1 IODelay, for phase adjustment.

Address offset: 0x00020 (R): TID trigger live timer

Bit 31-0 (r): board live time counter. The real time is Bit(31:0)*256*40ns.

Address offset: 0x00024 (R): TID busy (trigger dead) timer

Bit 31-0 (r): TID busy (can not accept trigger, or trigger dead) time counter. The real time is Bit(31:0)*256*40ns. This counter and the live time counter make up the total time counter, which is the total time since any one of the trigger sources is enabled.

Address offset: 0x00028 (R): Trigger/Sync/Busy monitoring

Bit 31-24 : Trigger monitoring;

Bit 23-16 : Sync input monitoring;

Bit 15-0 : Busy input monitoring.

Address offset: 0x0002C (R): Trigger Interrupt counter

Bit 31-24 : Number of data blocks READY for VME interrupt;

Bit 23-0 : to be re-assigned, right now, it is the repeat of A24(offset 0x14);

Address offset: 0x00030 (R): GTP STATUS_A

Bit 7-0: GTP[7:0] reset_done;

Bit 11-8: GTP PLL lock detected (two GTPs per PLL lock);

Bit 31-12 : not used yet;}

Special for two crate test at EEL119 with TID_rev1: Address offset: 0x00030 (R): TS trigger sync information (V10.4 and later)

Bit 7-0: Number of blocks to be read out on HFBR#5

Bit 15-8: Number of blocks the HFBR#5 is still missing (may be in the fiber);

Bit 23-16: Number of blocks to be read out on HFBR#6

Bit 31-24: Number of blocks the HFBR#6 is still missing (may be in the fiber);

Address offset: 0x00034 (R): GTP STATUS_B registers (valid for FPGA firmware V9 and after)

Bit 7-0: Channel bonding sequence detected in GTP[7:0];

Bit 15-8: received data is not an 8B/10B character, or has disparity error in GTP[7:0];

Bit 23-16: RX disparity error has occurred in GTP[7:0];

Bit 31-24: Rx data not in 8B/10B table has occurred in GTP[7:0];

Address offset: 0x00038 (R): GTP trigger data buffer length (firmware V10 and after)

Bit 9-0: Global trigger data buffer length (to be minimized to 0 for the longest fiber);

Bit 25-16: Sub-system trigger data buffer length;

Bit 28: HFBR#1 MGT receiver error;

Bit 29: CLK250 DCM locked;

Bit 30: Clk125 DCM locked;

Bit 31: VME CLK (33MHz or 25MHz) DCM locked

Address offset: 0x0003C (R): TS input trigger counter

Bit 31-0: Number of triggers received by TS (before BUSY inhibits);

Address offset: 0x00040 (R): valid for TM (or with TS function), not valid for TI
Bit 7-0: Number of blocks to be readout on HFBR#1;
Bit 15-8: Number of blocks is still missing on HFBR#1
Bit 23-16: Number of blocks to be readout on HFBR#2
Bit 31-24: Number of blocks is still missing on HFBR#2
Address offset: 0x00044 (R): valid for TM (or with TS function), not valid for TI
Bit 7-0: Number of blocks to be readout on HFBR#3;
Bit 15-8: Number of blocks is still missing on HFBR#3;
Bit 23-16: Number of blocks to be readout on HFBR#4;
Bit 31-24: Number of blocks is still missing on HFBR#4;

As the HFBR#1 is configured as trigger input, HFBR#2,3,4 is not used, so offset 0x40 and 0x44 should all be 0.

Address offset: 0x00048 (R): valid for TM (or with TS function), not valid for TI
Bit 7-0: Number of blocks to be readout on HFBR#5;
Bit 15-8: Number of blocks is still missing on HFBR#5;
Bit 23-16: Number of blocks to be readout on HFBR#6;
Bit 31-24: Number of blocks is still missing on HFBR#6;
Address offset: 0x0004C (R): valid for TM (or with TS function), not valid for TI
Bit 7-0: Number of blocks to be readout on HFBR#7;
Bit 15-8: Number of blocks is still missing on HFBR#7;
Bit 23-16: Number of blocks to be readout on HFBR#8;
Bit 31-24: Number of blocks is still missing on HFBR#8;
Address offset: 0x00050 (R): valid for TM (or with TS function), not valid for TI
Bit 7-0: Number of blocks to be readout on HFBR#8; (redundant with 0x4C)
Bit 15-8: Number of blocks is still missing on HFBR#8; (redundant with 0x4C)
Bit 23-16: Number of blocks to be readout on TM itself;
Bit 31-24: Number of blocks is still missing on TM itself;

Address offset: 0x00100 (W): Reset and one-shot registers. The signal will be one ClkVme cycle. If the ClkVme is 25 MHz, the one-shot will be 40ns wide. Positive logic.

Bit 0: not used;
Bit 1: if ‘1’, RESET signal to reset the VME_to_I2C engine;
Bit 2: if ‘1’, RESET signal to reset the VME_to_JTAG engine;
Bit 3: if ‘1’, RESET signal to reset the VME_to_SFM engine;
Bit 4: if ‘1’, RESET signal to reset the VME registers (TID settings) to their default values;
Bit 7: if ‘1’, this register will generate a BUSY reset, and Trg_Ack pulse (TS rev2 compatible).
Bit 8: if ‘1’, Reset the CLK250/Clk200 DCM.
Bit 9: if ‘1’, Reset the CLK125 DCM.
Bit 11: if ‘1’, Auto alignment of SYNC phase from HFBR#1;
Bit 12: if ‘1’, Auto alignment of SYNC phase from HFBR#5;
Bit 13: if ‘1’, Auto alignment of fiber latency measurement signals;
Bit 14: if ‘1’, Reset the IODELAY;
Bit 15: if ‘1’, Measure the fiber latency
Bit 16: if ‘1’, this register will generate a ‘TAKE_TOKEN’
Address offset: 0x00800 (W): VME Trigger Command Register
Bit 11-0: Trigger Command code transmitted in the trigger link;
Bit 31-12: not used.
Address offset: 0x00804 (W): VME Trigger Generation
Bit 15-0: Number of triggers to be generated;
Bit 31-16: (trigger rate control) Time between triggers. T = (160+80*Bit(30:20)*1024$^{\text{Bit(31)}}$) ns. (Assuming that the ClkVme=25MHz or 40ns period).

Address offset: 0x00808 (W): VME Random Trigger Command Register
Bit 2-0: Random trigger_1 rates: 500KHz/($2^{\text{Bit}(2:0)}$);
Bit 3: enable/disable random trigger_1.
Bit 7-4: same as Bit(3-0) for redundancy check. No match, no trigger_1.
Bit 10-8: Random trigger_2 rates: 500KHz/($2^{\text{Bit}(2:0)}$);
Bit 11: enable/disable random trigger_2.
Bit 15-12: same as Bit(11-8) for redundancy check. No match, no trigger_2.
Address offset: 0x0080C (W): VME Trigger_2 Generation
Bit 15-0: Number of triggers to be generated;
Bit 31-16: (trigger rate control) Time between triggers. T = (160+80*Bit(30:20)*$1024^{\text{Bit}(31)}$) ns. (Assuming that the ClkVme=25MHz or 40ns period).

Address offset: 0x008CX (W): Trigger table loading: (prototype for TS)
Bit 31-0: 32-bit wide table loading.
Address bits(5-2) are used to load 16 32-bit words;
6-bit read addressing with 8-bit trigger type (byte wide)

Address offset: 0x00900 (W): VME Sync Load
Bit 7-4 == Bit 3-0: 4-bit sync code;
Bit 31-8: not used.
Decoding of the Sync command (bit[7:0]):
0x11: VME clock DCM reset;
0x22: CLK250 resync (AD9510, DCM resync and GTP reset);
0x44: Reset the GTP status_B registers;
0x55: Trigger link enable (serial link started), FIFO read counter reset;
0x77: Trigger link disable, trigger FIFO write counter reset;
0xDD: (SyncReset), FPGA logic and counter reset, this reset all goes to SD, CTP/GTP;
0x33, 0x66, 0x88, 0x99, 0xaa, 0xbb, 0xcc, 0xee: to be assigned;
0x00, 0xff: reserved, not to be assigned
Address offset: 0x00904 (W): VME Sync Delay. The latency before being serialized.
Bit 6-0: latency, in 4ns steps;
Bit 12-8: Reset (to SW#A, SW#B and on-board) pulse width, in 4-ns steps;
Bit 7, 31-13: not used.

6.3 VME to Serial engines:

A24D32 are used for VME to serial engines. The engines include: VME to JTAG engine for the FPGA, VME to JTAG engine for the PROM, VME to I2C for the switch slot#A, VME to I2C engine for the switch slot#B, and VME to I2C engine for the P2 connector (could be used for anything). In the I2C engines design, only the lower one-byte or 2-byte of the 32-bit data word is used. The higher bytes are not used.

Address offset: 0x1XXXX: JTAG for PROM; Refer to the programming manual for VME to JTAG design for details.
Address offset: 0x2XXXX: JTAG for FPGA;
Address offset: 0x3XXXX: I2C for VXS switch slot#A; Refer to the programming manual for VME to I2C design for details.
Address offset: 0x4XXXX: I2C for VXS switch slot#B;
Address offset: 0x5XXXX: I2C for VME P2 connector (to be assigned);
Address offset: 0x6XXXX: Serial Flash memory interface.
Address offset: 0x0NXXX: SFM memory readout: (to be implemented)
0x07X0: IO_Delay #X reset;
0x07X4: IO_Delay #X delay increment (by 1);

0x07X8: IO_Delay #X de-serialized data readout, idle=’0xFFFF’;
0x07Xc: IO_Delay #X automatic delay increment by a number stored in SFM.

6.4 VME data acquisition:

For data acquisition, the A32 block reads are used. The base address is set by the upper 9 bits of A24 register 0x00010, that is A[31:23] = RegData[31:23] of A24=0x00010.

7 Backplane pin out tables:

7.1 VXS P0 Pinout Table

Payload slot#18, used in TI mode			
Pin name	Signal Description	Signal Level	Direction
DP1 (A1+, B1-)	CLOCK_C	LVPECL(DP)	PP18 → SWA
DP2 (D1+, E1-)	CLOCK_D	LVPECL(DP)	PP18 → SWA
DP3 (B2+, C2-)	Not Used		
DP4 (E2+, F2-)	SYNC	LVPECL(DP)	PP18 → SWA
DP5 (A3+, B3-)	TRIG1	LVPECL(DP)	PP18 → SWA
DP6 (D3+, E3-)	TRIG2	LVPECL(DP)	PP18 → SWA
DP7 (B4+, C4-)	TP_Data_LINK	LVDS(DP)	PP18 ←→ SWA
DP8 (E4+, F4-)	BUSY	LVDS	PP18 ← SWA
SE1 (G1)	SCL	I2C (+3.3V)	PP18 → SWA
SE2 (G3)	SDA	I2C (+3.3V)	PP18 ←→ SWA
DP23 (B12+, C12-)	CLOCK_A	LVPECL(DP)	PP18 → SWB
DP24 (E12+, F12-)	CLOCK_B	LVPECL(DP)	PP18 → SWB
DP25 (A13+,B13-)	TOKEN_OUT	LVDS(DP)	PP18 → SWB
DP26 (D13+, E13-)	SYNC	LVPECL(DP)	PP18 → SWB
DP27 (B14+, C14-)	TRIG1	LVPECL(DP)	PP18 → SWB
DP28 (E14+, F14-)	TRIG2	LVPECL(DP)	PP18 → SWB
DP29 (A15+,B15-)	SD/GTP_Data_Link	LVDS, 250Mbps	PP18←→SWB
DP30 (D15+,E15-)	BUSY	LVDS	PP18 ← SWB
SE7 (G13)	SCL	I2C(+3.3V)	PP18 → SWB
SE8 (G15)	SDA	I2C(+3.3V)	PP18 ←→ SWB

7.2 Standard payload slots for TID in trigger distribution crate:

DP23 (B12+, C12-)	TRIG_LINK	LVPECL(DP)	PP ← SWB
DP24 (E12+, F12-)	SYNC	LVPECL(DP)	PP ← SWB
DP25 (A13+, B13-)	CLK250MHz	LVPECL(DP)	PP ← SWB
DP26			
DP27			
DP28			
DP29	SD_Data_link	LVDS	PP←→SWB
DP30	BUSY	LVDS	PP → SWB
SE7			

SE8			

7.3 VME P2 User-defined pin table

Similar to this, but Row-C is used. The two adjacent pins are used as a pair for differential signals.

Pin name	Signal Name	Signal Level
C01	SCL	I2C (LVCMOS)
C02	SDA	I2C (LVCMOS)
C05	CLK250_P	ECL
C06	CLK250_N	ECL
C09	CLK_A_P	ECL
C10	CLK_A_N	ECL
C13	CLK_B_P	ECL
C14	CLK_B_N	ECL
C17	TRIG1_P	ECL
C18	TRIG1_N	ECL
C21	TRIG2_P	ECL
C22	TRIG2_N	ECL
C25	SYNC_P	ECL
C26	SYNC_N	ECL
C29	BUSY+	ECL
C30	BUSY-	ECL

8 TID Operation examples:

The following is some operating procedures at VxWorks interactive mode. This is just a memo for the quick test of the TID board. They may change as the TID debug proceeds. First, one needs to login the VME controller. Here is the sequence:

Xming to PHECDA, linux server computer

From any xterm (or PUTTY), telnet to DAVW1 (neither username, nor password is needed). Only one telnet process is supported for the MVME6100 module). The address mapping for A24 is 0x90xxxxxx. For DAVW8, which is a MVME5100 module, the address mapping for A24 is 0xFA000000. The M6100 has twice as much as M5100 in A32 memory. The M5100 is 0x08000000-0x0FFFFFFF; while the M6100 is 0x08000000-0x17FFFFFF.

The following commands are assuming that the TID is in slot#6 VME64x compatible crate (Geographic address available). 0x30 = 00110xxx, that is the Geographic Address GA=6 or 00110.

8.1 A24 register echoing (write and read):

➔ *(0x90300008)=0x5566aa99; the same register should be read out

8.2 A32 readout of event data:

The A32 mode has to be setup first for the proper data readout. In the VxWorks interactive mode:

➔ *(0x90300010)=0x10000010; use A32 and Fast_access, base address 0x10000000
➔ *(0x90300000)=0xa59; 10 events per block, crate ID is 0x59
➔ M 0x88000000,4; A32 memory access

8.3 Set the VME trigger:

It is better to set the event block size and the crate ID first. The lower 16-bits are used to set the number of VME trigger. The higher 16-bits are used to set the VME trigger rate. The trigger period (inverse of trigger rate) is D(30:16)*8*40*(2048**D(31)) ns. Right now, the VME triggers are evenly space.

- *(0x90300000)=0xa59: 0xa=10 events per block, crate ID is 0x59
- *(0x90300804)=0x8fff0032; 0x8fff the trigger period is 650ms, that is about 1.5Hz; 0x32=50 events (VME triggers). After 50 events, the VME trigger will stop automatically.

8.4 Readout the FPGA user_ID:

The FPGA user code is readout through VME_to_JTAG engine. The FPGA user_ID is firmware specific. If this code matches, it is TID and the right version of the firmware is loaded.

- *(0x90300100)=0x04: VME_to_JTAG engine logic reset
- *(0x9032003C)=0x0: Reset FPGA JTAG to 'reset_idle' state
- *(0x9032092C)=0x3C8: enable user_ID readback
- *(0x90321F1C)=0x00: shift in 32-bit data, and the readback is user_ID. The user_ID should be 5948nmmm: n is the major version of the firmware, mmm is the revision of the firmware. It is 0x59485012 for the I2C readout test.

8.5 SW#A I2C operation:

The VME_to_I2C engine hides the serialization, and the two-bytes write (and/or read) can be finished by a single VME write (and/or read) command. For SW#A, the I2C chain is 011; for device 1101000, the I2C device at the FPGA is 000; assuming the byte address is 0xAD (10101101).

- *(0x90300100)=0x01: VME_to_I2C engine reset
- *(0x90331EB4)=0xDADA: VME_to_I2C write
- m 0x90331EB4, 4: VME to I2C read. ignore the higher two bytes
- *(0x90300004)=0x100: Set the I2C address to 0b1101xxx
- *(0x90331eb4)=0xdata: VME to I2C write

8.6 VME sync command loading:

In Ts mode, the SYNC command can be loaded by VME A24 register. A=0x900 is the sync register. The data bits (7:0) are used for the four bits Sync command. For redundancy, the Bit(7:4)==Bit(3:0), and 0000, 1111 are illegal sync command. If the data is 0x55, the trigger link will switch from idle to normal trigger data transfer, mean while, a trigger buffer readout START command will be generated on the SYNC link. This is the mechanism to have all the triggers synced on the front end crates. The A24 register 0x904 is used to set the delay between VME write and the Sync out on the TS. The data bits (6:0) are used. With 250MHz clock, this gives 512 ns range with 4ns resolution. For the SYNC (using IODELAY) to work properly, a Delay_Reset is necessary, especially if the FPGA is reprogrammed without power cycling.

- *(0x90300100)=0x4000: Delay Reset
- *(0x90300904) = 0x2F: set the delay to ~200 ns
- *(0x90300900) = 0x55: send the 0x5 sync code through SYNC link
- *(0x90300900) = 0x77: send the 0x7 sync code through SYNC link, which will set the WriteStart for the trigger data elastic buffer.
- *(0x90300900) = 0x55: send the trigger link start command. The code 0x5 will set the ReadStart for the trigger data elastic buffer. Both the WriteStart and ReadStart will reset the write address counter and read address counter respectively.

8.7 VME trigger through trigger control word:

In Ts mode, the trigger control word can be loaded by VME A24 register. A=0x800 is the trigger control register. The trigger control register will be transferred on the trigger link when there is no trigger_strobe and trigger_content word. The trigger control word will be buffered, as the trigger strobe and trigger content words have higher priorities. Here is a sample when loop the HFBR#5 outputs to HFBR#1 inputs for the test:

- ➔ *(0x90300100)=0x4000: IODelayReset. This is required if the FPGA is reprogrammed without power recycling.
- ➔ *(0x90300900) = 0x77: SYNC command to reset the HFBR#1 data buffer address counter, and stop the HFBR#5 trigger data transfer. If the trigger data was enabled, another (same) VME may be required to clear the address counter. (the address counter is enabled by receiving trigger data on HFBR#1)
- ➔ *(0x90300904) = 0x53: set the latency for the SYNC command. The latency is in steps of 250MHz clock cycles (4ns per step).
- ➔ *(0x90300900) = 0x55: SYNC command to start the trigger data transfer on HFBR and to reset the alignment trigger data buffer readout address counter. The trigger data transfer is enabled when the VME command is received. The read address counter is reset when the SYNC is received, which has a latency set by the previous VME command. As the SYNC command latency is controllable across different TIs, the trigger data readout will be the same across different TIs. This is the mechanism for trigger sync (though different GTP may have different serialiser/deserialiser delays)
- ➔ *(0x90300800)=0x18: This register will set VME trigger control word 0x18 (VME data bits 11:0 are used). When the trigger control word is transmitted, the TrgData(12)=1 & TrgData(13)=0. In the current design, the TI will interpret the 0bxxxxxx1100xx as TRIGGER1 (x: do not care bit). The TRIGGER_1 width is set by the A24D32 register (next).
- ➔ *(0x9030000C)=0x300: This register set the trigger width and trigger latency.

8.8 TSrev2 trigger, VME interrupt and BUSY trigger throttling:

The TSrev2 trigger is input through the Mezzanine Board. The following commands are based on a MVME5100 VME controller (CPU module), and the TID is in slot#6, that is geographical address 0x00110. The test procedure is: load the library, setup the trigger, and the board, enable the trigger, readout data, and finally send trigger acknowledge to TSrev2 and reset the busy:

- ➔ ld < universeDma.o;
- ➔ ld < tid.o;
- ➔ intConnect(183,cpuDelay,10); The IRQ STATUS/ID is 0xb7 = 183
- ➔ sysIntEnable(5); The TID is requesting on IRQ level 5.
- ➔ *(0xfa30000c)=0x900; setup the trigger pulse width
- ➔ *(0xfa300004)=0x202000; enable front panel BUSY and enable IRQ
- ➔ *(0xfa300000)=0x4008a9; set the crate ID to 0xA9, event block to 8, enable the TSrev2 trigger only (be sure to loop the TSOUT_3 on GenIO connector to Trg_strobe IN on mezzanine board.
- ➔ tidRead(0x20); readout trigger data
- ➔ m 0xfa300020,4; readout the TID alive time counter
- ➔ m 0xfa300024, 4; readout the TID busy (trigger dead) time counter
- ➔ *(0xfa300100)=0x80; send the trigger acknowledge and reset the busy

9 TID Operation procedures (software setup):

The following is the operating procedures at VxWorks interactive mode. This is just a memo for the quick test of the TID board. The procedure will be optimized as the test goes along. This assumes that the hardware switch is set properly (as TI, TD, TS/TD/TI etc.)

The following commands are assuming that the TID is in slot#6 VME64x compatible crate (Geographic address available). The MVME6100 controller is used, which has A24 memory mapping to 0x90######. For slot#6 TID, the A24 address will be: 0x9030xxxx. The A32 address will be 0x08-0x17###### on VME, and mapped to 0x80000000-0x8FFFFFFF on CPU.

The software is located at phecda:~jgu/software/tid.c. The tid.c works with the ~jgu/usrTempeDma_AM.o, which is the modified version of usrTempeDma.o for user defined AM codes, on MVME6100. The software for different platforms can be written with minor changes.

9.1 Fiber latency measurement:

- *(0x90300100)=0x4000 //reset the digital IODELAY logic/clock
- *(0x90300100)=0x2000 //phase alignment of the latency measurement signal
- *(0x90300100)=0x8000 //Fiber latency measurement
- M 0x90300018,4 //Fiber latency readout
- *(0x90300100)=0x800 //Sync phase alignment relative to the 250MHz clock
- *(0x9030001c)=0xAAxxBBxx // load the Sync delay (AA for HFBR#5, BB for HFBR#1). The BB should be based on the previous measurement.
- M 0x9030001c,4 //check the SYNC delay setting and phase alignment.

9.2 Trigger/DAQ setup:

- *(0x90300000)=0x6200095a //CrateID=0x5A, block size= 0x09, no trigger source has been enabled yet, HFBR#1 sync enabled, TI timing and status words are disabled, two place-holder block words are enabled.
- *(0x90300004)=0x10030011 //HFBR#5 busy enabled, Switch slot#A and slot#B BUSY enabled (set to 0x10000011 to disable SW#A and SW#B busy inputs), optical transceiver#1 and #5 are enabled. Set to 0x10000011 if SD and CTP BUSY inputs will NOT be enabled.
- *(0x9030000C)=0x07000700 //External trigger input prescale=1, trigger 2 pulse width 32ns, trigger2 delay 0, trigger1 pulse width 32ns, trigger1 delay 0.
- *(0x90300010)=0x08000010 //A32 base address 0x08######, A32 readout enabled

9.3 Trigger link startup:

- *(0x90300900)=0x77
- *(0x90300900)=0x77 //WriteStart, buffer_write_address reset and trigger data transmit disable
- *(0x90300904)=0x754 //Sync latency, delay before SYNC being serialized. This delay should cover the largest latency on SYNC delay set by A24, 0x001C register. The Reset pulse width is (7+1)*4ns;
- *(0x90300900)=0x55 //Start the trigger link, and this SYNC command will enable the trigger link buffer readout.

9.4 Trigger source enable:

- M 0x90300000,4 //read back the current setting
- *(0x90300000) = (previous_readout bit_OR 0x120000) enable the VME trigger for TS and HFBR#1 trigger for TI.

9.5 Interrupt Request Enable:

- *(0x90300008) = (original Bit_OR 0x5b7 //set the IRQ level to 5, ID to 0xB7;
- *(0x90300004) = (original Bit_OR 0x202000 //enable VME interrupt request and front panel BUSY monitor.
- *(0x90300100)=0x80 // reset the BUSY and IRQ

9.6 VME Trigger:

- *(0x90300800)=0x18 //one trigger_1 is generated by “TRIGGER COMMAND”, or
- *(0x90300804)=0xa6950200 //0x200 triggers at the period of 0x569a.

- ➔ *(0x90300800)=0x180 //one trigger_2 is generated by trigger command.

9.7 Trigger/DAQ monitoring:

- ➔ M 0x90300014, 4 //polling the register to see if there is data block to read
- ➔ M 0x90300020, 4 //TID trigger live timer (live time)
- ➔ M 0x90300024, 4 //TID trigger busy timer (dead time)

9.8 Data Readout:

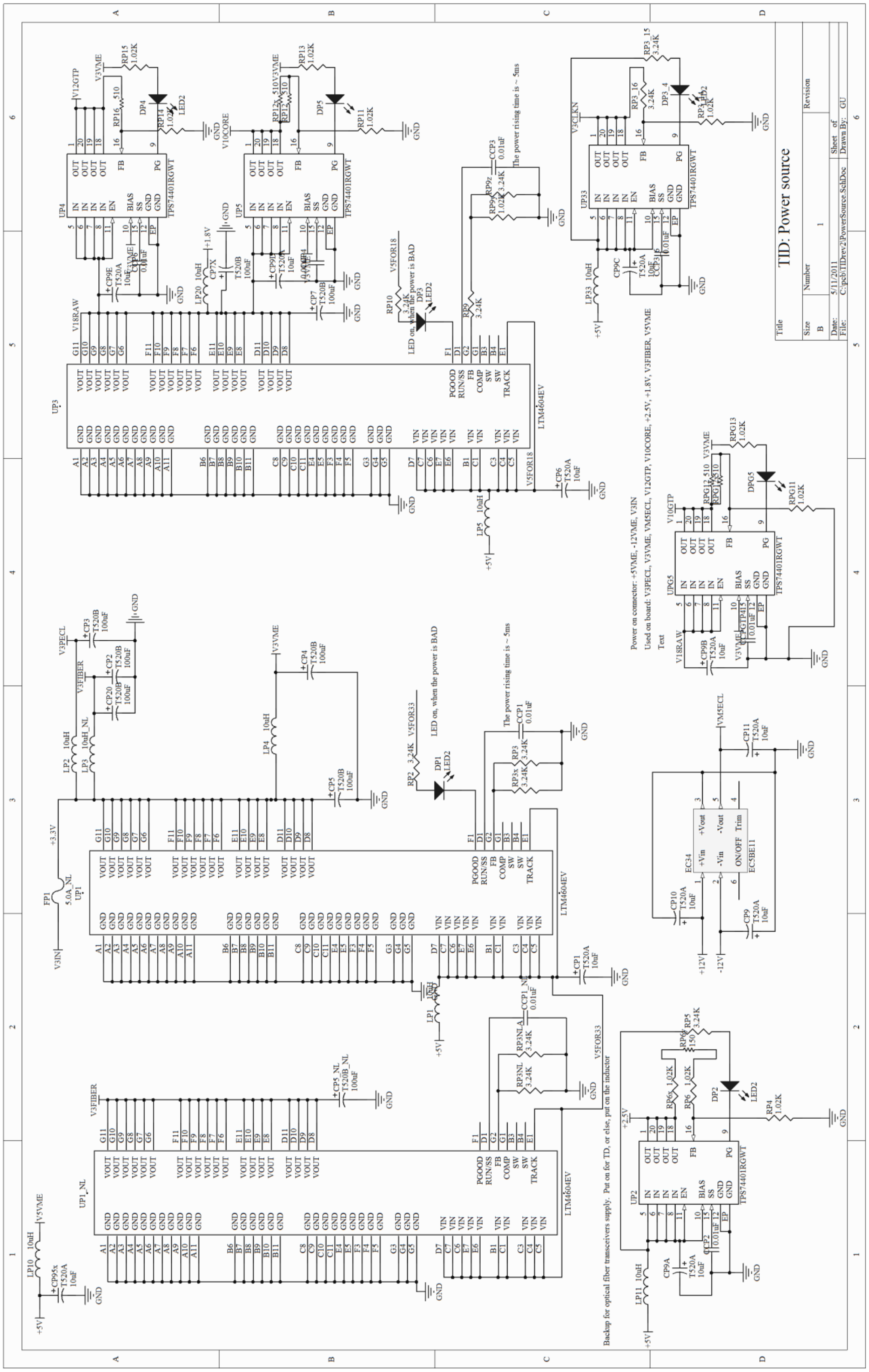
- ➔ M 0x80300100,4 //A32 readout; or
- ➔ tidRead(nwords) //readout nwords from TID; or
- ➔ tidBERead // readout a block, and using Bus_error to terminate the read; or
- ➔ ……

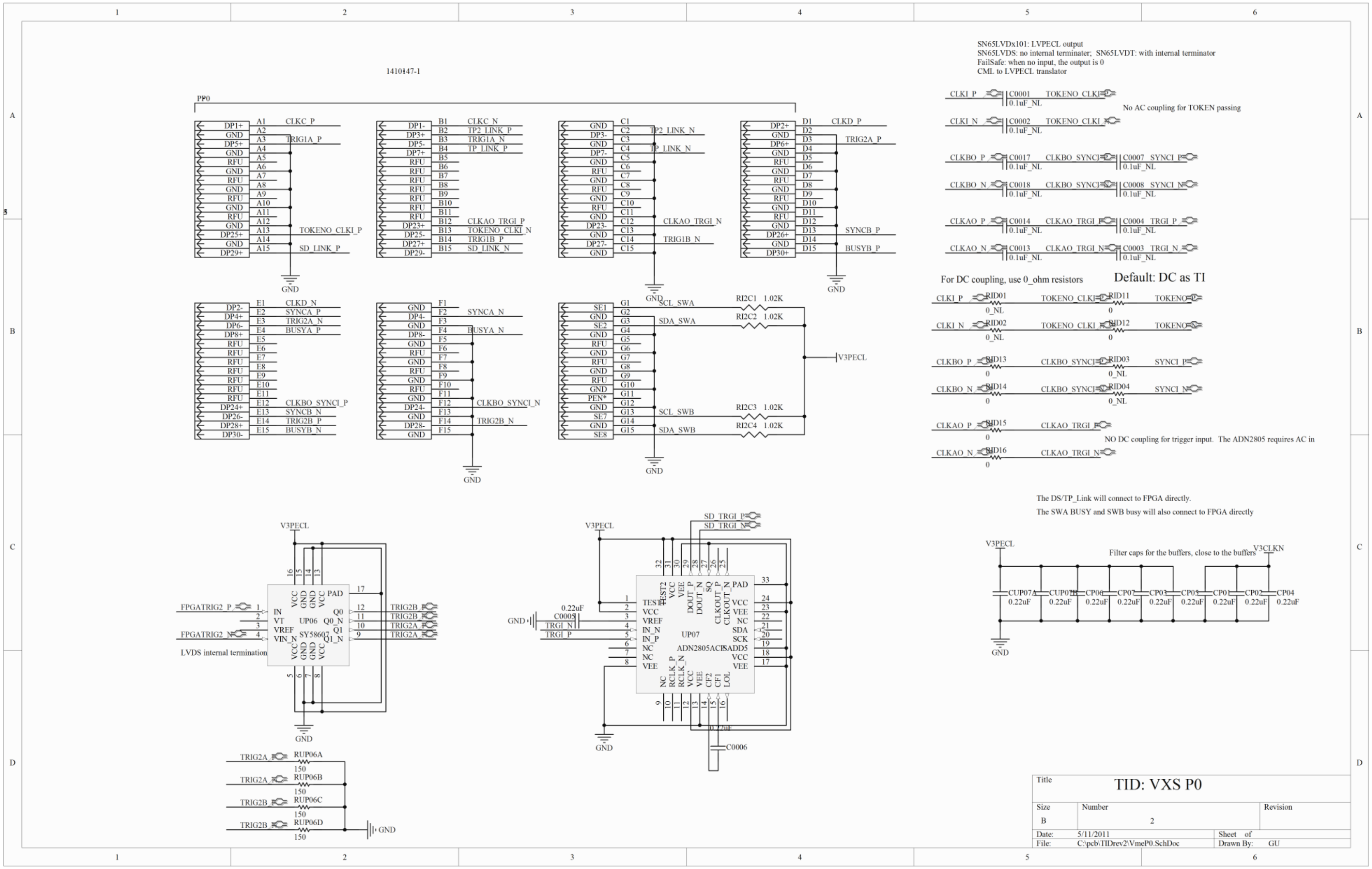
10. Citations:

Works Cited

Chris. (2009). Gloabal Trigger Processor., (pp. 1-14).
Chris. (2009). Hall_D trigger layout., (pp. 20-25). Virginia.
Collaboration, C. (2009). CLAS12 experiment. *Journal* , 1-25.
Collaboration, G. (2009). GlueX experiment. *journal* , 1-20.
Cuevas, C. (2008). Signal Distribution Module., (pp. 1-10).
Ed. (2010). Trigger Supervisor Module., (pp. 1-19).
experiments, C. (1990). CEBAF experiements. *journal* , 1-10.
GU. (2010). Optical transceiver jitter measurement., (pp. 1-12).
Raydo, B. (2008). Trigger Distribution board., (pp. 1-10).
GU, (2010). VME to JTAG implementation
GU, (2010). VME to I2C implementation

Appendix A: TID Schematics:


TID: Power source
Title
Size
B
Number
1
Revision
Date: 5/11/2011
File: C:\pcb\TIDrev2\PowerSource.SchDoc
Sheet of
Drawn By: GU
Power on connector: +5VME, -12VME, V3IN
Used on board: V3PECL, V3VME, VM5ECL, V12GTP, V10CORE, +2.5V, +1.8V, V3FIBER, V5VME
Text
The power rising time is ~ 5ms
LED on, when the power is BAD
Backup for optical fiber transceivers supply. Put on for TID, or else, put on the indicator
LTM4604EV
TPS74401RGWT
EC5BE11
EC34
UP1
UP1_NL
UP2
UP3
UP4
UP5
UP33
UPG5
V3IN
+3.3V
+5V
+12V
-12V
VM5ECL
V3PECL
V3FIBER
V3VME
V5VME
V5FOR18
V5FOR33
V18RAW
V12GTP
V10CORE
V10GTP
V3CLKN
+1.8V
+2.5V
GND
FP1
5.0A_NL
A
B
C
D
1
2
3
4
5
6



SN65LVDx101: LVPECL output
SN65LVDS: no internal terminater; SN65LVDT: with internal terminator
FailSafe: when no input, the output is 0
CML to LVPECL translator

No AC coupling for TOKEN passing

For DC coupling, use 0_ohm resistors

Default: DC as TI

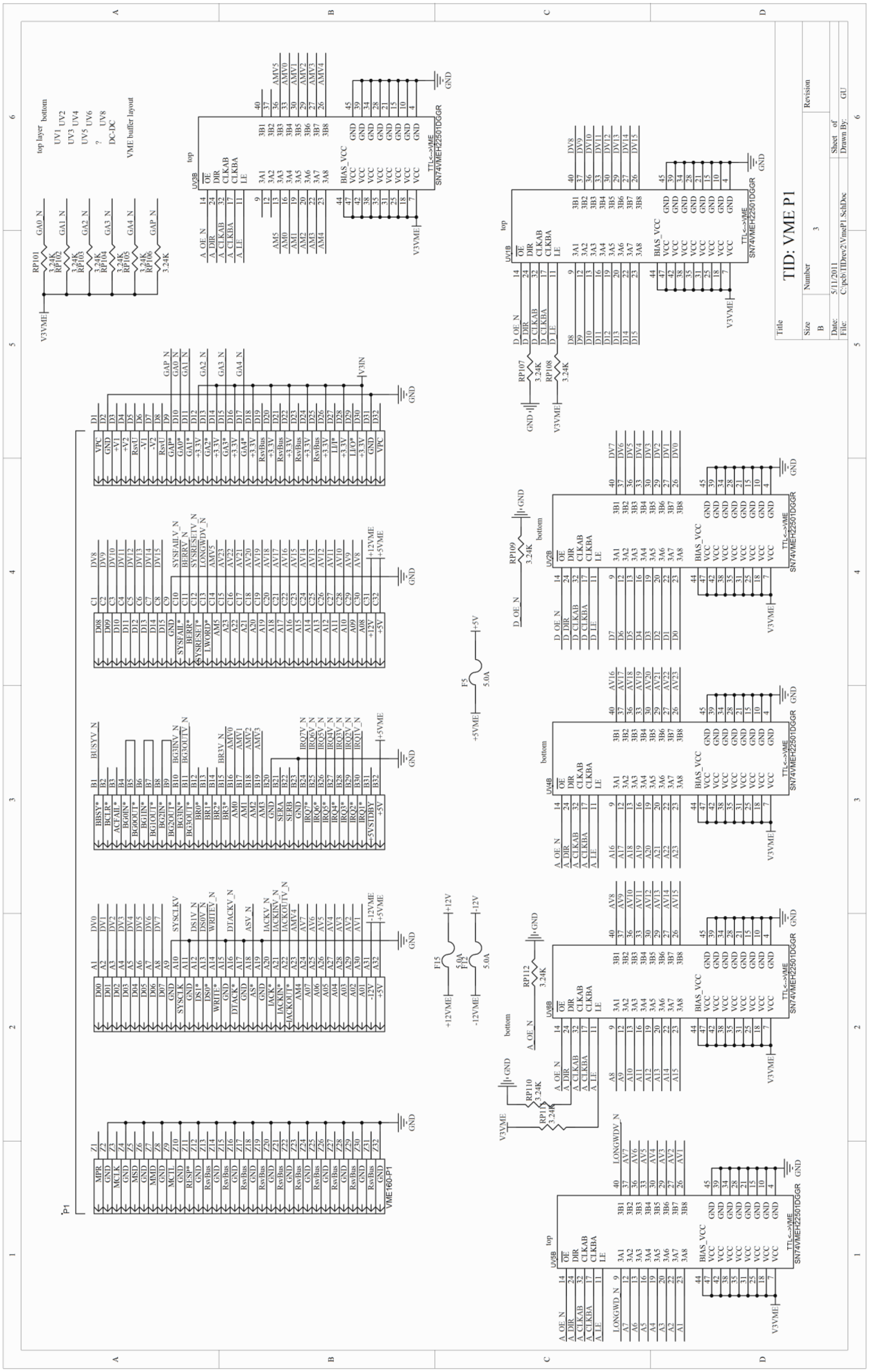
NO DC coupling for trigger input. The ADN2805 requires AC in

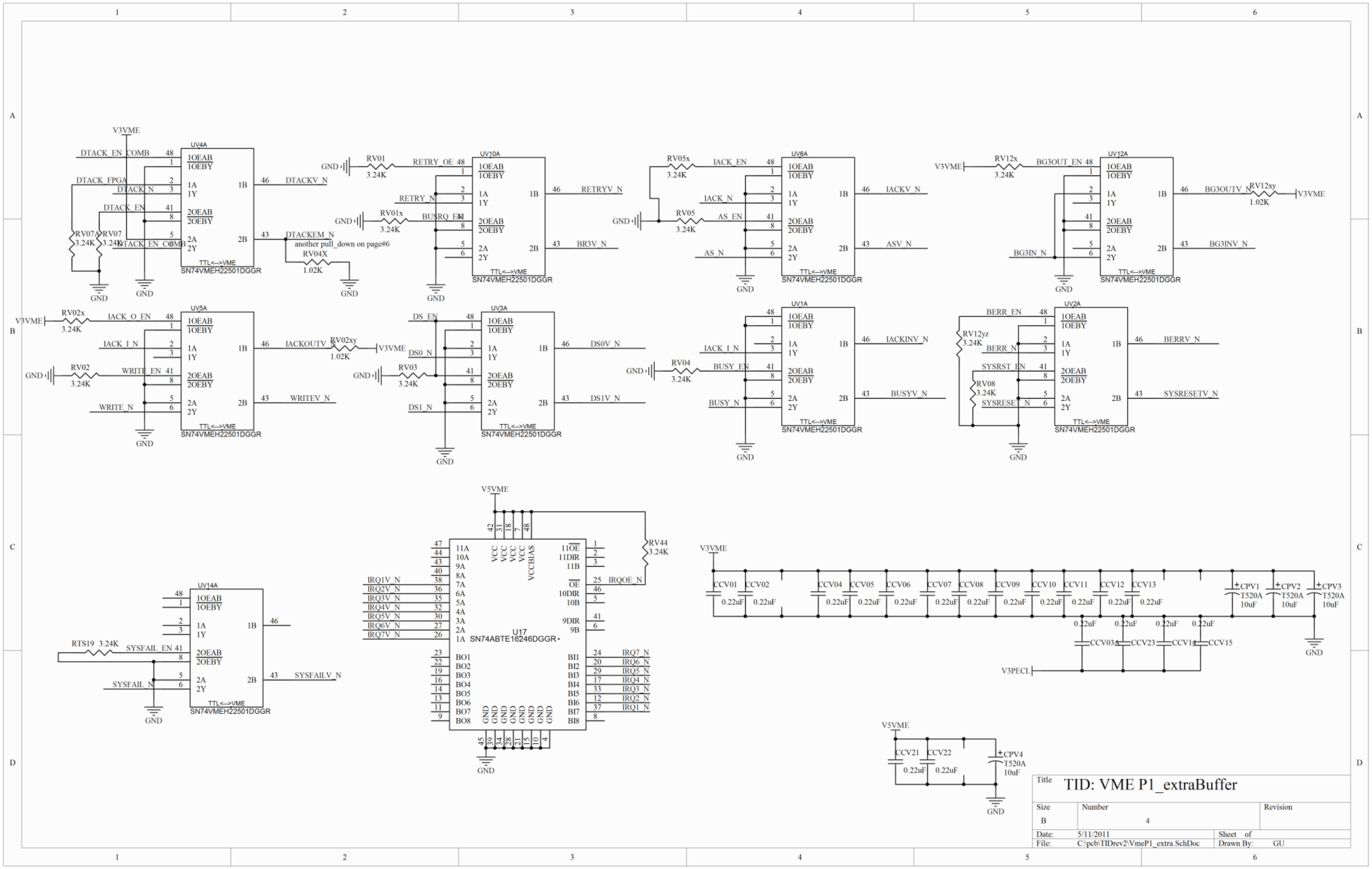
The DS/TP_Link will connect to FPGA directly.
The SWA BUSY and SWB busy will also connect to FPGA directly

Filter caps for the buffers, close to the buffers

LVDS internal termination

Title: TID: VXS P0
Size: B
Number: 2
Revision
Date: 5/11/2011
File: C:\pcb\TIDrev2\VmeP0.SchDoc
Sheet of
Drawn By: GU


TID: VME P1
Title
Size
B
Number
3
Revision
Date: 5/11/2011
Sheet of
File: C:\pcb\TIDrev2\VmeP1.SchDoc
Drawn By: GU
top layer bottom
UV1 UV2
UV3 UV4
UV5 UV6
? UV8
DC-DC
VME buffer layout
P1
VME160-P1
UV1B
UV2B
UV3B
UV4B
UV5B
UV6B
top
bottom
SN74VMEH22501DGGR
TTL<->VME
RP101
RP102
RP103
RP104
RP105
RP106
RP107
RP108
RP109
RP110
RP111
RP112
3.24K
F5
5.0A
F12
5.0A
F15
5.0A
+12VME
-12VME
+5VME
+12V
-12V
+5V
V3VME
V3IN
GND
A OE N
D OE N
LONGWD N
GA0 N
GA1 N
GA2 N
GA3 N
GA4 N
GAP N

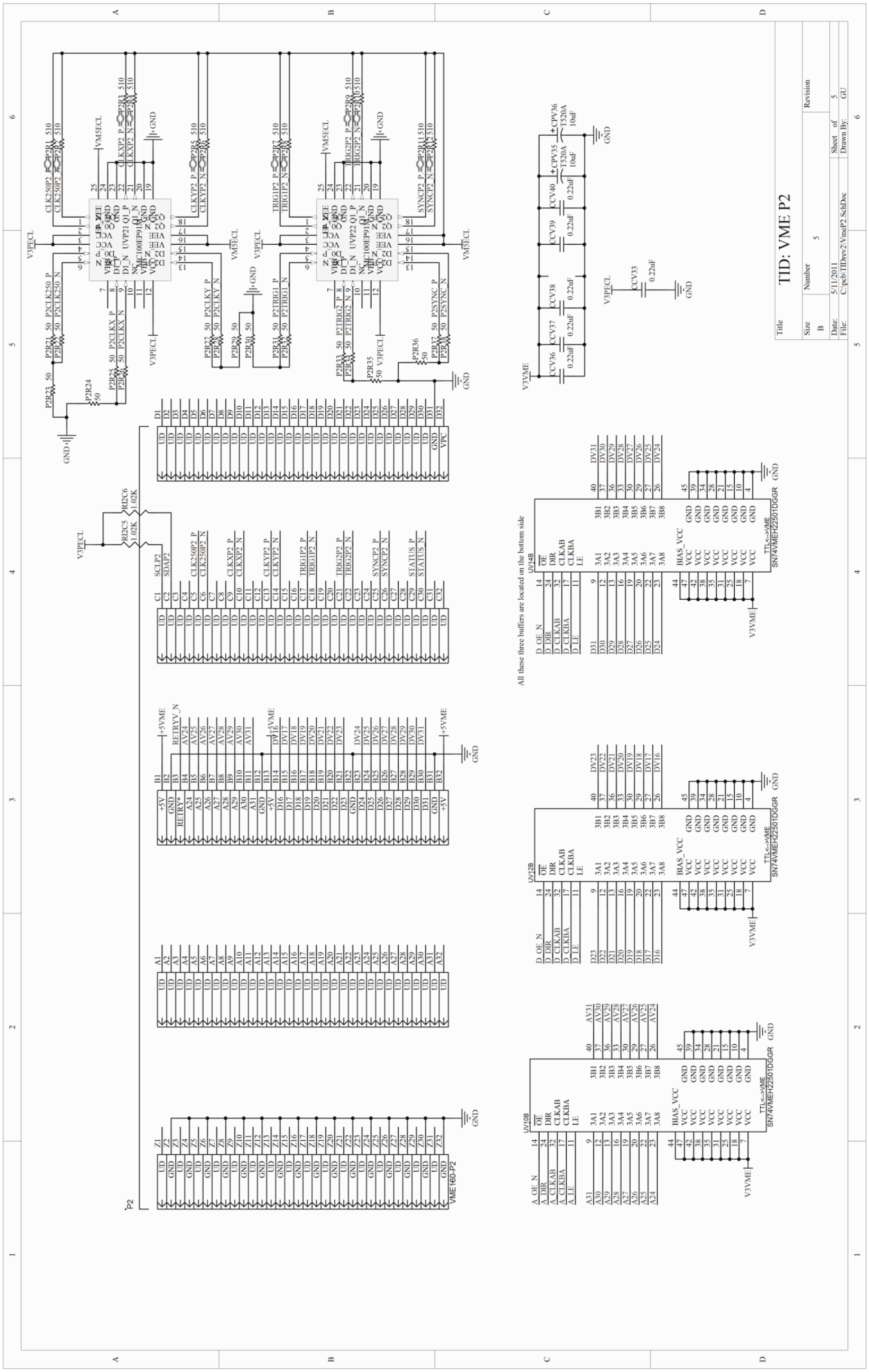


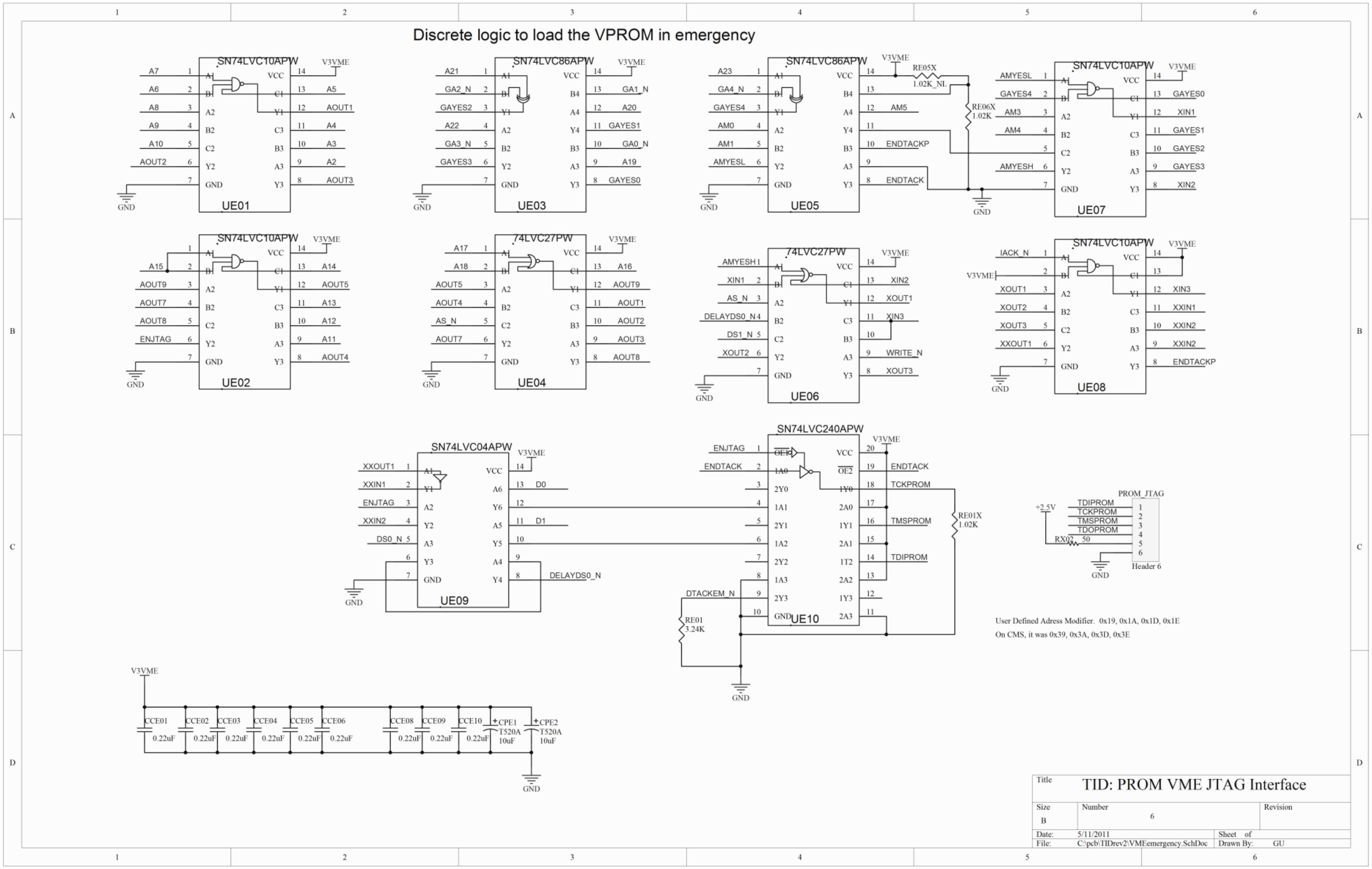
Title TID: VME P1_extraBuffer

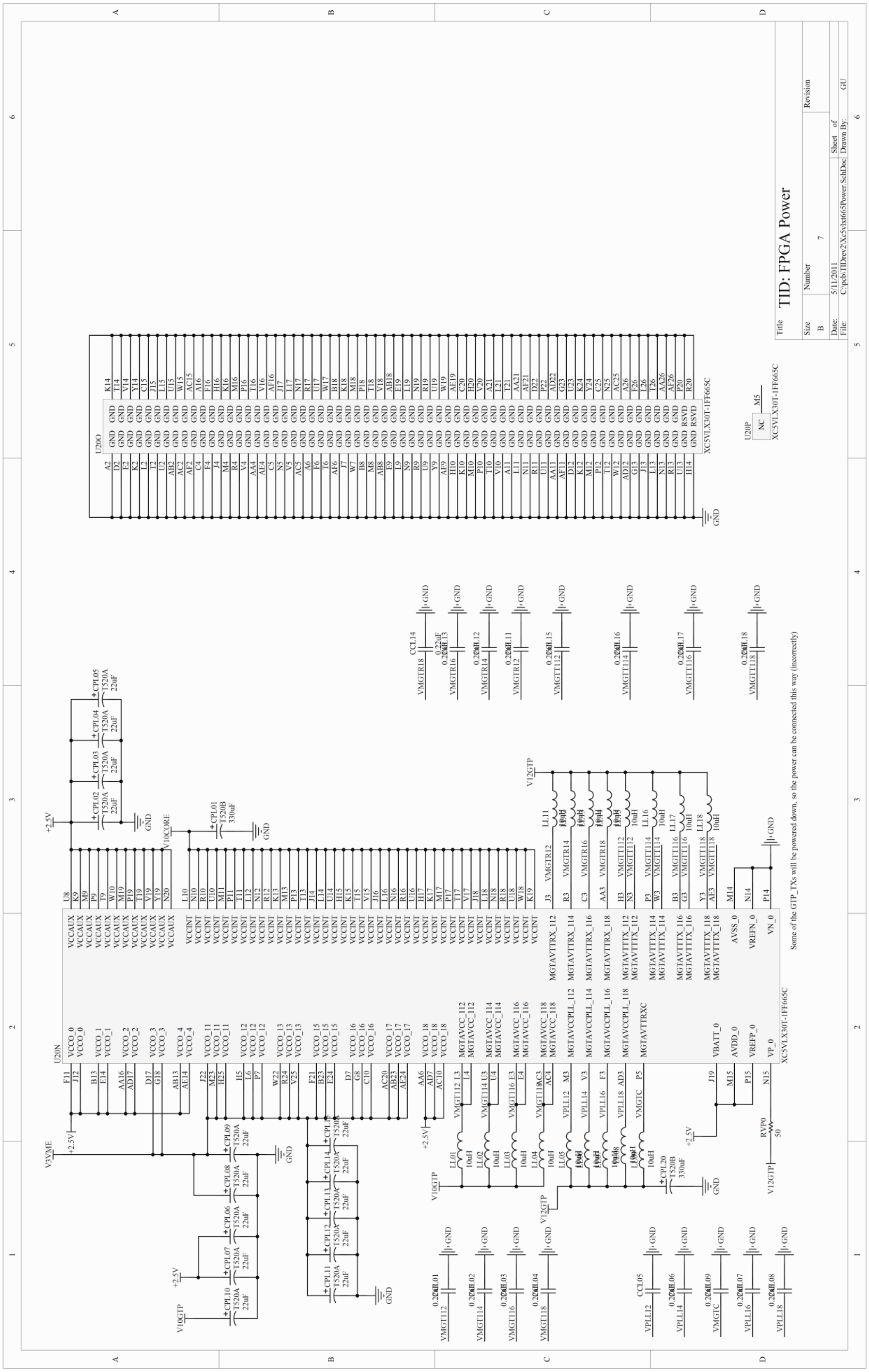
Size B | Number 4 | Revision

Date: 5/11/2011 | Sheet of

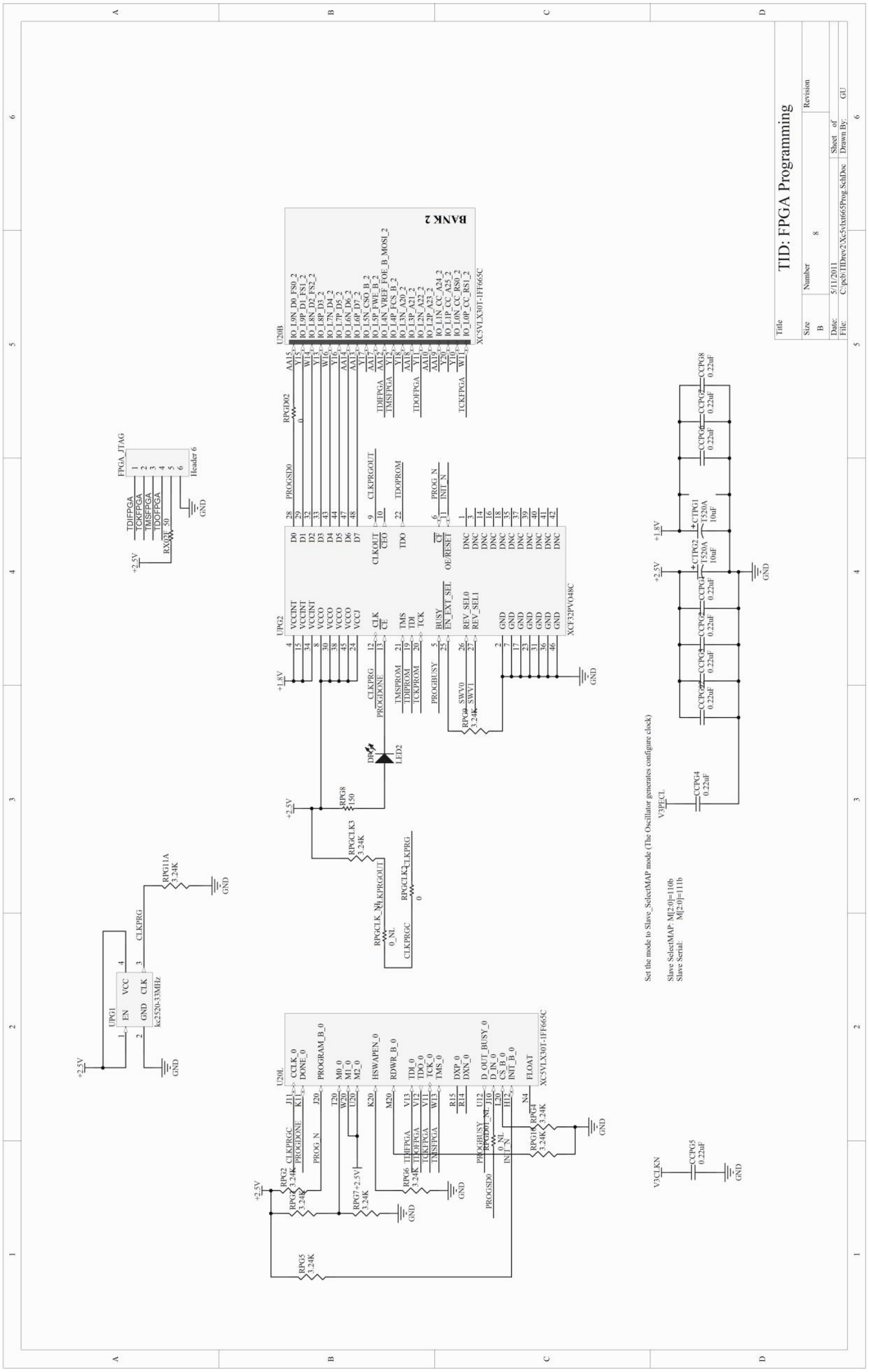
File: C:\pcb\TIDrev2\VmeP1_extra.SchDoc | Drawn By: GU


TID: VME P2
Title
Size
B
Number
5
Revision
Date: 5/11/2011
File: C:\pcb\TIDrev2\VmeP2.SchDoc
Sheet 5 of
Drawn By: GU
All these three buffers are located on the bottom side
P2
VME160-P2
UV10B
UV12B
UV14B
SN74VMEH22501DGGR
TTL<->VME
UVP21
UVP22
MC100EP91
V3PECL
VM5ECL
V3VME
+5VME
GND
CLK250P2_P
CLK250P2_N
CLKXP2_P
CLKXP2_N
CLKYP2_P
CLKYP2_N
TRIG1P2_P
TRIG1P2_N
TRIG2P2_P
TRIG2P2_N
SYNCP2_P
SYNCP2_N
STATUS_P
STATUS_N
SCLP2
SDAP2
RETRYV_N
CPV35
CPV36
T520A
10uF
0.22uF
RI2C5
RI2C6
1.02K
A
B
C
D
1
2
3
4
5
6

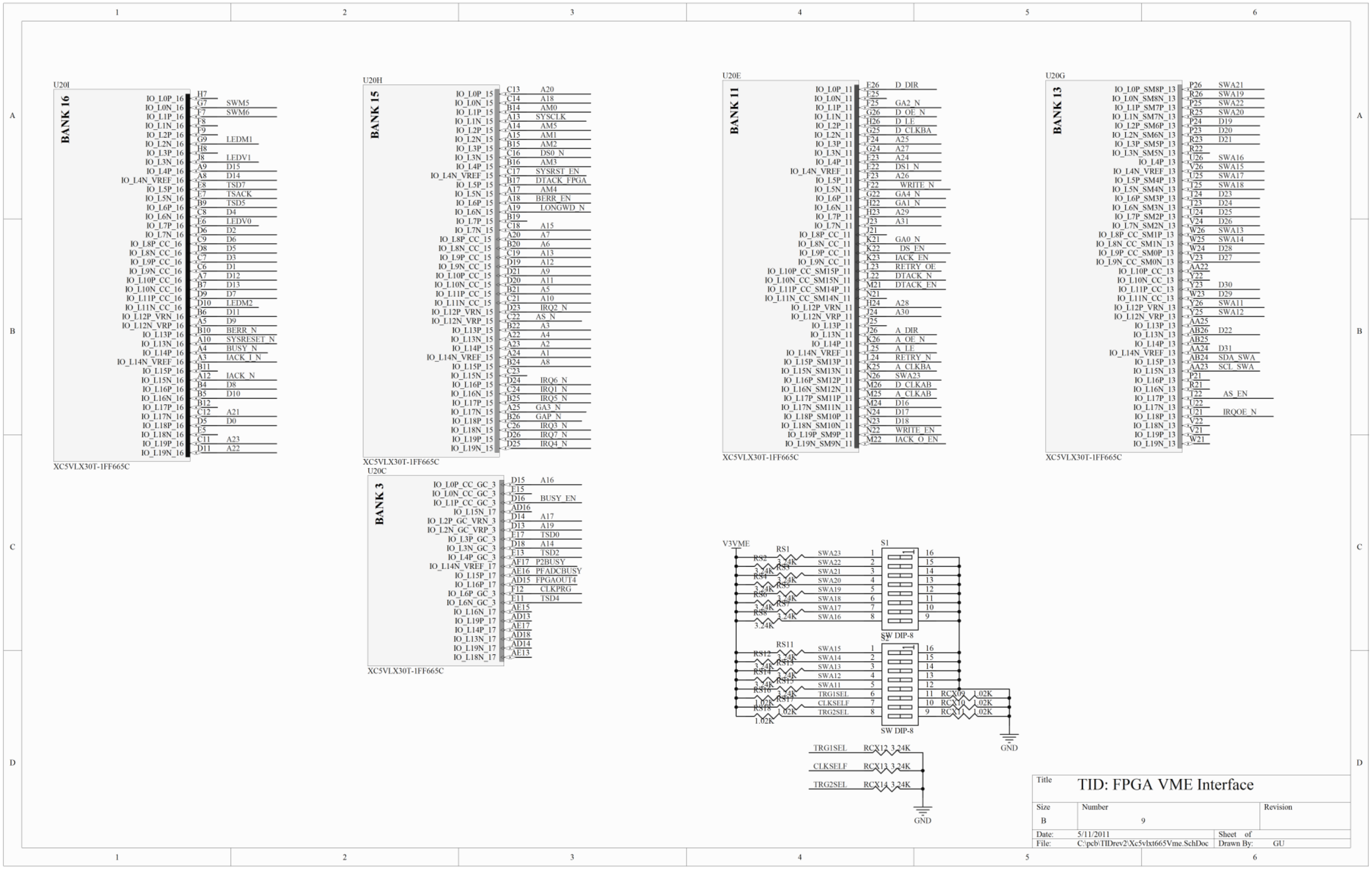

Discrete logic to load the VPROM in emergency
SN74LVC10APW
UE01
A7
A6
A8
A9
A10
AOUT2
A5
AOUT1
A4
A3
A2
AOUT3
V3VME
GND
SN74LVC86APW
UE03
A21
GA2_N
GAYES2
A22
GA3_N
GAYES3
GA1_N
A20
GAYES1
GA0_N
A19
GAYES0
SN74LVC86APW
UE05
A23
GA4_N
GAYES4
AM0
AM1
AMYESL
AM5
ENDTACKP
ENDTACK
RE05X
1.02K_NL
RE06X
1.02K
SN74LVC10APW
UE07
AMYESL
GAYES4
AM3
AM4
AMYESH
GAYES0
XIN1
GAYES1
GAYES2
GAYES3
XIN2
SN74LVC10APW
UE02
A15
AOUT9
AOUT7
AOUT8
ENJTAG
A14
AOUT5
A13
A12
A11
AOUT4
74LVC27PW
UE04
A17
A18
AOUT5
AOUT4
AS_N
AOUT7
A16
AOUT9
AOUT1
AOUT2
AOUT3
AOUT8
74LVC27PW
UE06
AMYESH1
XIN1
AS_N
DELAYDS0_N
DS1_N
XOUT2
XIN2
XOUT1
XIN3
WRITE_N
XOUT3
SN74LVC10APW
UE08
IACK_N
XOUT1
XOUT2
XOUT3
XXOUT1
XIN3
XXIN1
XXIN2
XXIN2
ENDTACKP
SN74LVC04APW
UE09
XXOUT1
XXIN1
ENJTAG
XXIN2
DS0_N
D0
D1
DELAYDS0_N
SN74LVC240APW
UE10
ENJTAG
ENDTACK
DTACKEM_N
ENDTACK
TCKPROM
TMSPROM
TDIPROM
RE01
3.24K
RE01X
1.02K
PROM_JTAG
+2.5V
TDIPROM
TCKPROM
TMSPROM
TDOPROM
RX02
50
Header 6
User Defined Adress Modifier. 0x19, 0x1A, 0x1D, 0x1E
On CMS, it was 0x39, 0x3A, 0x3D, 0x3E
CCE01 0.22uF
CCE02 0.22uF
CCE03 0.22uF
CCE04 0.22uF
CCE05 0.22uF
CCE06 0.22uF
CCE08 0.22uF
CCE09 0.22uF
CCE10 0.22uF
CPE1 T520A 10uF
CPE2 T520A 10uF
Title TID: PROM VME JTAG Interface
Size B
Number 6
Revision
Date: 5/11/2011
Sheet of
File: C:\pcb\TIDrev2\VMEemergency.SchDoc
Drawn By: GU

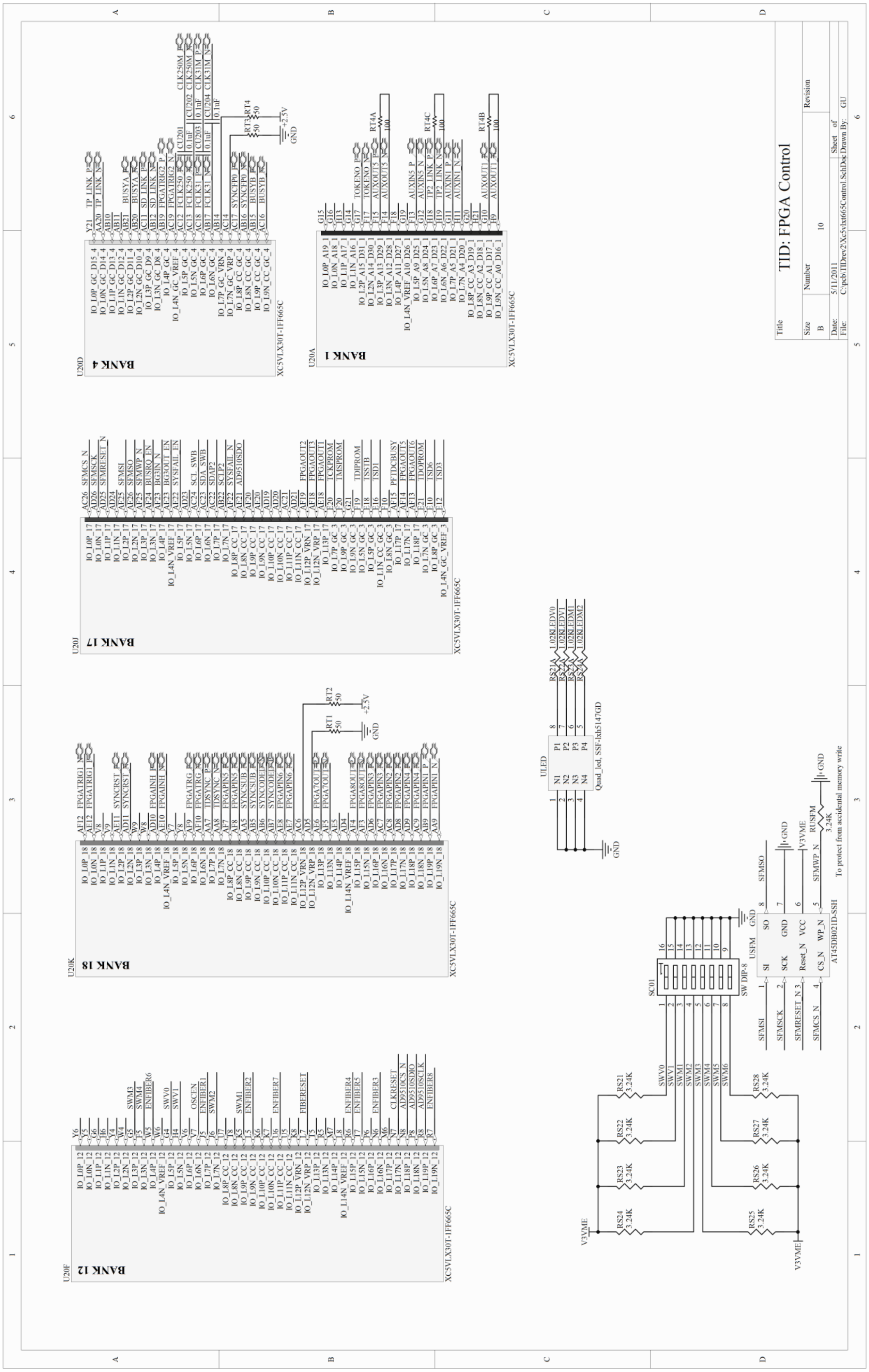


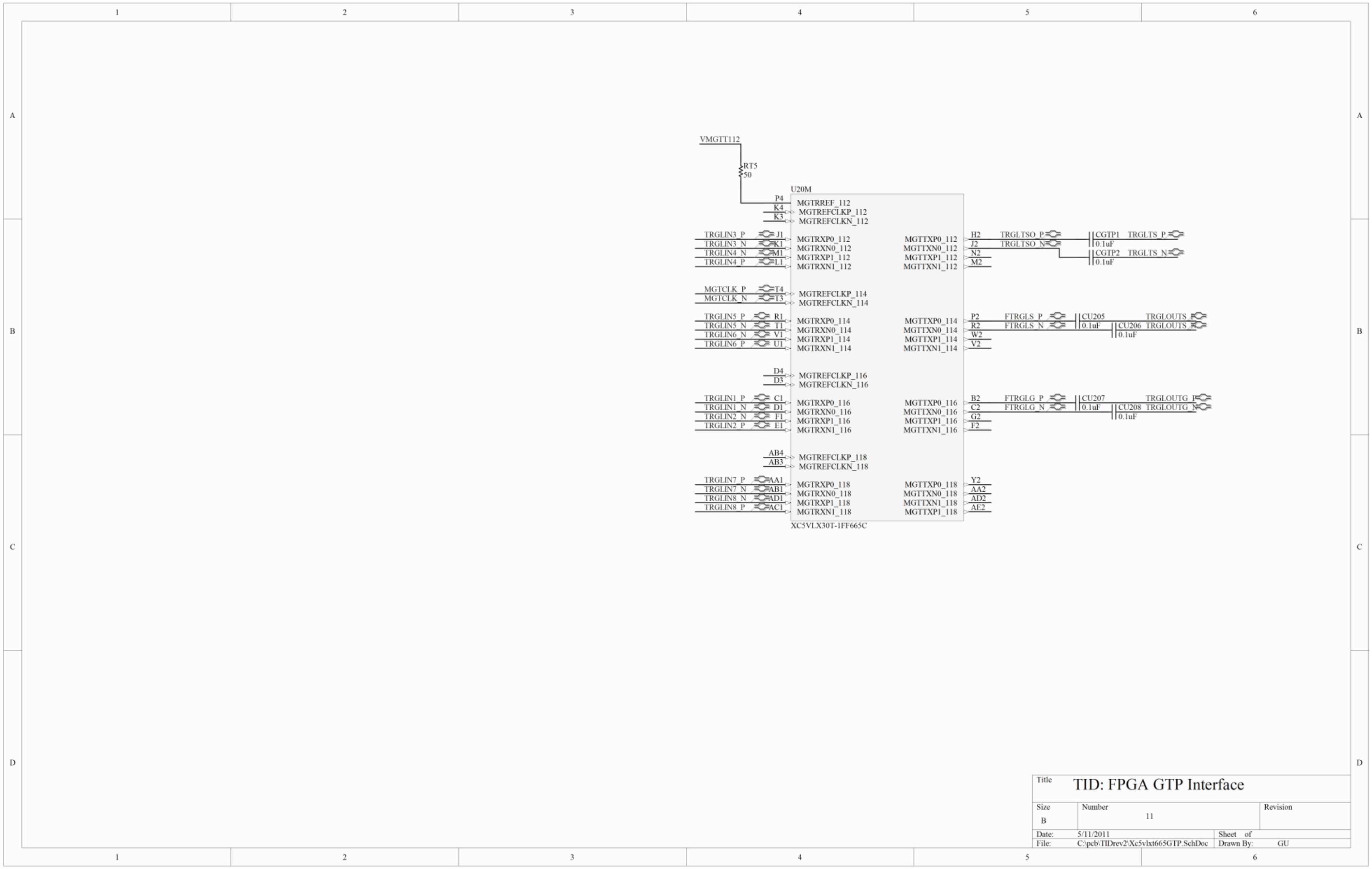
Some of the GTP_TXs will be powered down, so the power can be connected this way (incorrectly)

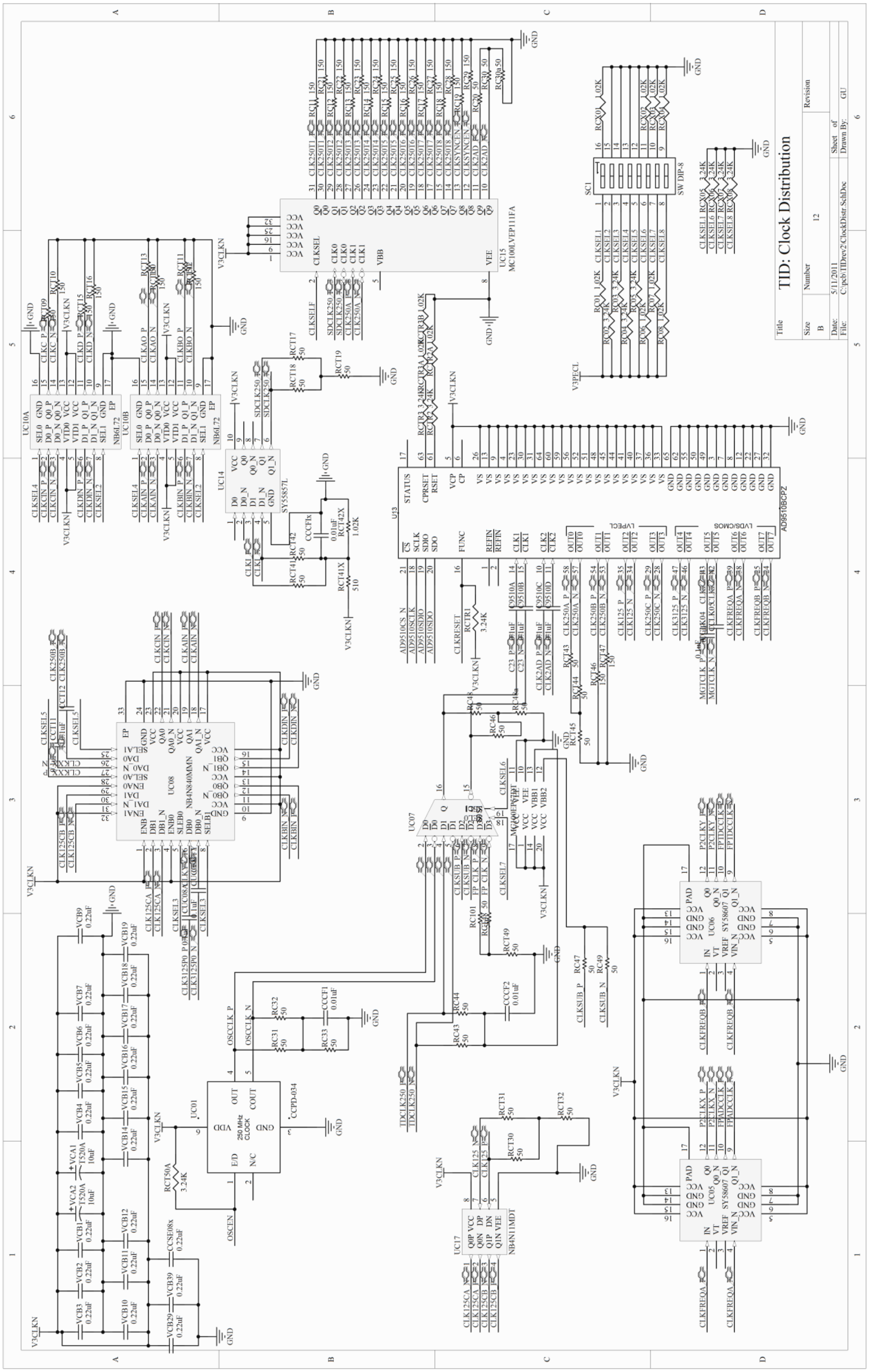


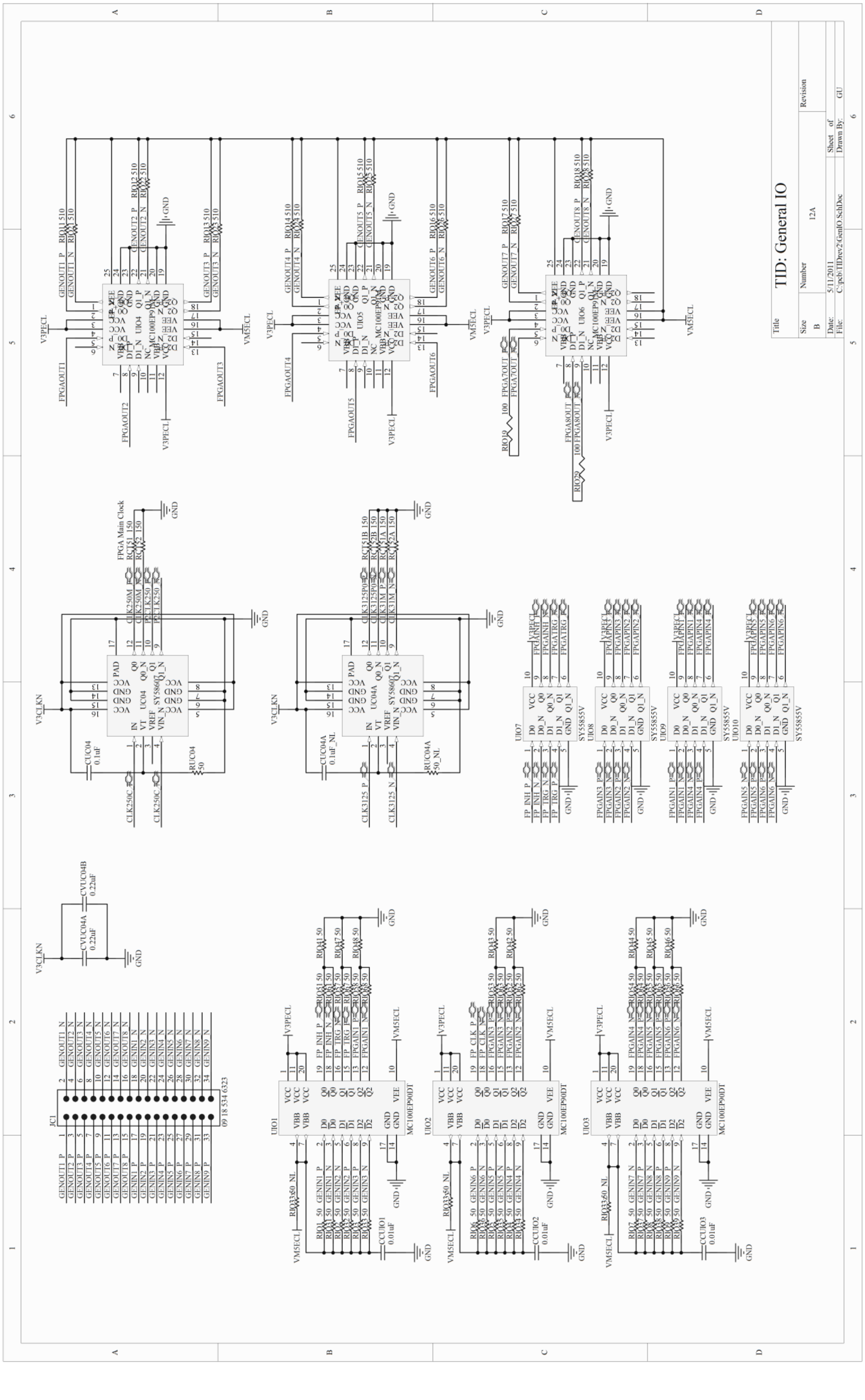
TID: FPGA Programming
Title
Size
B
Number
8
Revision
Date: 5/11/2011
Sheet of
File: C:\pcb\TIDrev2\Xc5vlx8665Prog.SchDoc
Drawn By: GU
BANK 2
U20B
XC5VLX30T-1FF665C
U20L
UPG2
XCF32PVO48C
UPG1
kc2520-33MHz
FPGA_JTAG
Header 6
LED2
Set the mode to Slave_SelectMAP mode (The Oscillator generates configure clock)
Slave SelectMAP: M[2:0]=110b
Slave Serial: M[2:0]=111b
PROGSD0
RPGD02
CLKPRGOUT
TDOPROM
PROG_N
INIT_N
TDIFPGA
TMSFPGA
TDOFPGA
TCKFPGA
CLKPRG
PROGDONE
PROGBUSY
TMSPROM
TDIPROM
TCKPROM
CLKPRGC
V3PECL
V3CLKN
+2.5V
+1.8V
GND

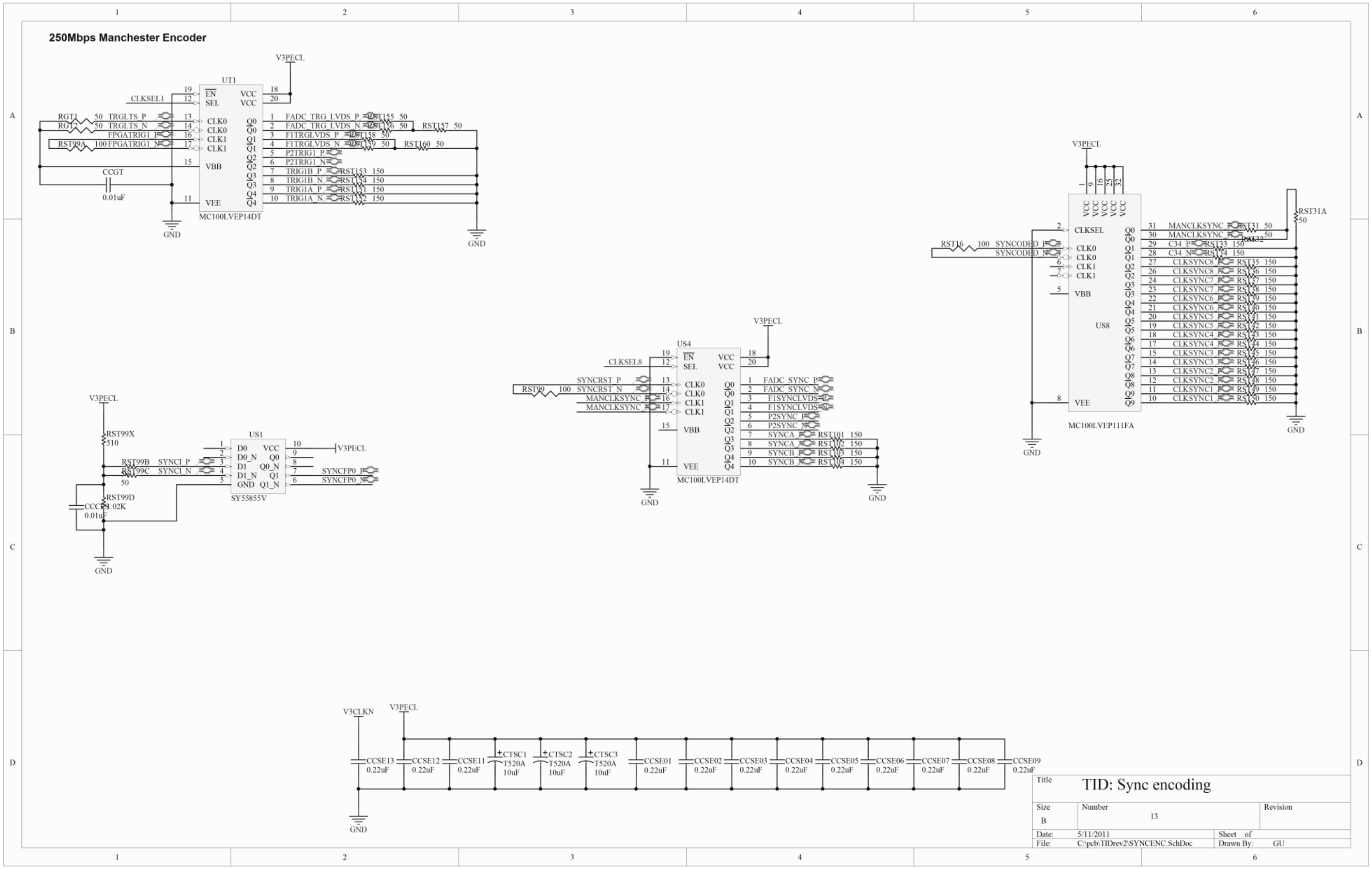

U20I
BANK 16
XC5VLX30T-1FF665C
SWM5
SWM6
LEDM1
LEDV1
D15
D14
TSD7
TSACK
TSD5
D4
LEDV0
D2
D6
D5
D3
D1
D12
D13
D7
LEDM2
D11
D9
BERR_N
SYSRESET_N
BUSY_N
IACK_I_N
IACK_N
D8
D10
A21
D0
A23
A22
U20H
BANK 15
XC5VLX30T-1FF665C
A20
A18
AM0
SYSCLK
AM5
AM1
AM2
DS0_N
AM3
SYSRST_EN
DTACK_FPGA
AM4
BERR_EN
LONGWD_N
A15
A7
A6
A13
A12
A9
A11
A5
A10
IRQ2_N
AS_N
A3
A4
A2
A1
A8
IRQ6_N
IRQ1_N
IRQ5_N
GA3_N
GAP_N
IRQ3_N
IRQ7_N
IRQ4_N
U20C
BANK 3
XC5VLX30T-1FF665C
A16
BUSY_EN
A17
A19
TSD0
A14
TSD2
P2BUSY
PFADCBUSY
FPGAOUT4
CLKPRG
TSD4
U20E
BANK 11
XC5VLX30T-1FF665C
D_DIR
GA2_N
D_OE_N
D_LE
D_CLKBA
A25
A27
A24
DS1_N
A26
WRITE_N
GA4_N
GA1_N
A29
A31
GA0_N
DS_EN
IACK_EN
RETRY_OE
DTACK_N
DTACK_EN
A28
A30
A_DIR
A_OE_N
A_LE
RETRY_N
A_CLKBA
SWA23
D_CLKAB
A_CLKAB
D16
D17
D18
WRITE_EN
IACK_O_EN
U20G
BANK 13
XC5VLX30T-1FF665C
SWA21
SWA19
SWA22
SWA20
D19
D20
D21
SWA16
SWA15
SWA17
SWA18
D23
D24
D25
D26
SWA13
SWA14
D28
D27
D30
D29
SWA11
SWA12
D22
D31
SDA_SWA
SCL_SWA
AS_EN
IRQOE_N
V3VME
RS1
S1
SW DIP-8
S2
SW DIP-8
RS11
3.24K
1.02K
TRG1SEL
CLKSELF
TRG2SEL
RCX12 3.24K
RCX13 3.24K
RCX14 3.24K
GND
Title
TID: FPGA VME Interface
Size
B
Number
9
Revision
Date:
5/11/2011
Sheet of
File:
C:\pcb\TIDrev2\Xc5vlxt665Vme.SchDoc
Drawn By:
GU

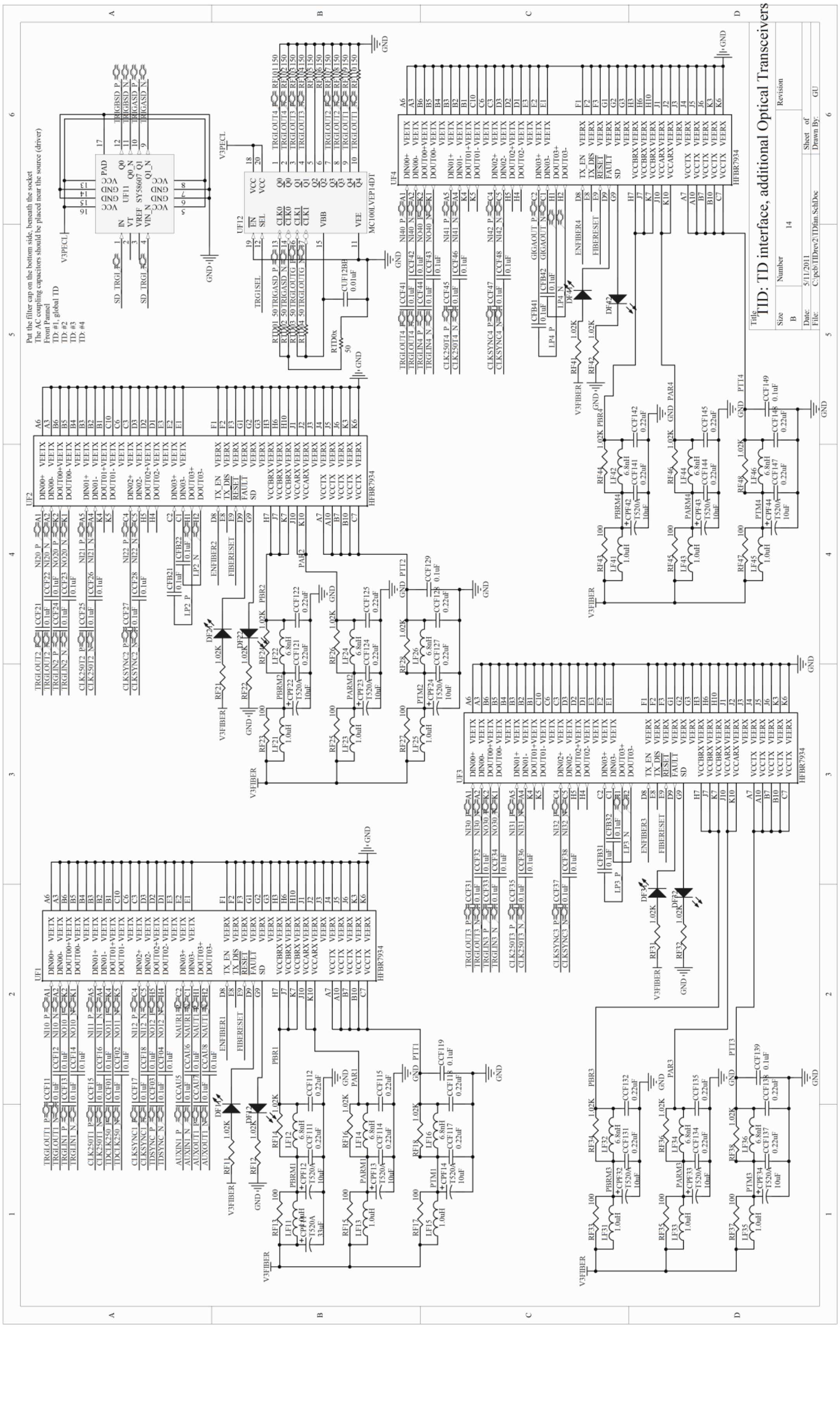

TID: FPGA Control
Title
Size
B
Number
10
Revision
Date: 5/11/2011
Sheet of
File: C:\pcb\TIDrev2\Xc5vlx665Control.SchDoc
Drawn By: GU
BANK 4
U20D
XC5VLX30T-1FF665C
BANK 1
U20A
XC5VLX30T-1FF665C
BANK 17
U20J
XC5VLX30T-1FF665C
BANK 18
U20K
XC5VLX30T-1FF665C
BANK 12
U20F
XC5VLX30T-1FF665C
ULED
Quad_led, SSF-lxh5147GD
SC01
SW DIP-8
USFM
AT45DB021D-SSH
To protect from accidental memory write
V3VME
GND
+2.5V

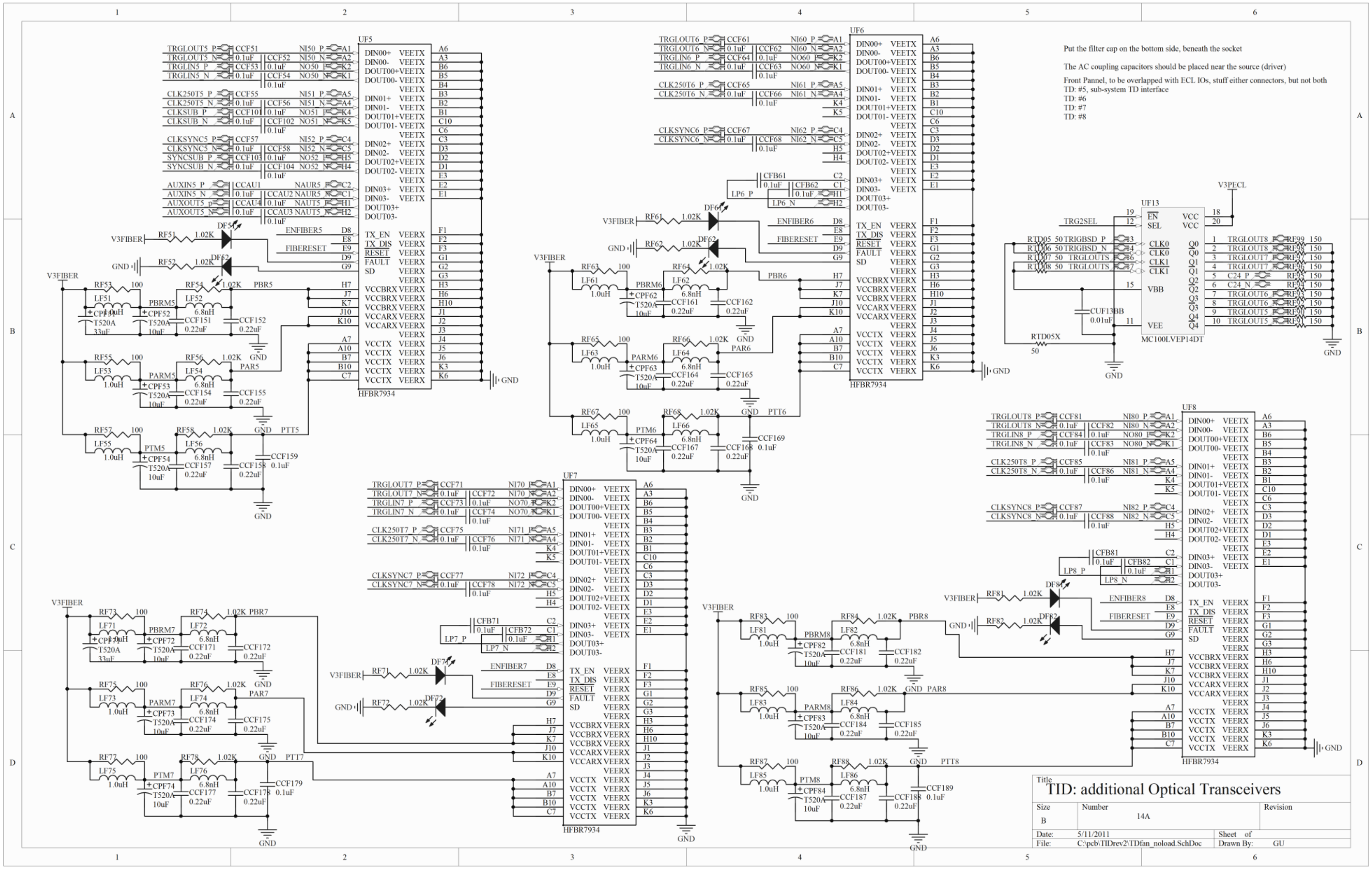

1
2
3
4
5
6
A
B
C
D
VMGTT112
RT5
50
U20M
P4
MGTRREF_112
K4
MGTREFCLKP_112
K3
MGTREFCLKN_112
TRGLIN3_P
J1
TRGLIN3_N
K1
TRGLIN4_N
M1
TRGLIN4_P
L1
MGTRXP0_112
MGTRXN0_112
MGTRXP1_112
MGTRXN1_112
MGTCLK_P
T4
MGTCLK_N
T3
MGTREFCLKP_114
MGTREFCLKN_114
TRGLIN5_P
R1
TRGLIN5_N
T1
TRGLIN6_N
V1
TRGLIN6_P
U1
MGTRXP0_114
MGTRXN0_114
MGTRXP1_114
MGTRXN1_114
D4
D3
MGTREFCLKP_116
MGTREFCLKN_116
TRGLIN1_P
C1
TRGLIN1_N
D1
TRGLIN2_N
F1
TRGLIN2_P
E1
MGTRXP0_116
MGTRXN0_116
MGTRXP1_116
MGTRXN1_116
AB4
AB3
MGTREFCLKP_118
MGTREFCLKN_118
TRGLIN7_P
AA1
TRGLIN7_N
AB1
TRGLIN8_N
AD1
TRGLIN8_P
AC1
MGTRXP0_118
MGTRXN0_118
MGTRXP1_118
MGTRXN1_118
XC5VLX30T-1FF665C
MGTTXP0_112
H2
MGTTXN0_112
J2
MGTTXP1_112
N2
MGTTXN1_112
M2
TRGLTSO_P
TRGLTSO_N
CGTP1
0.1uF
CGTP2
0.1uF
TRGLTS_P
TRGLTS_N
MGTTXP0_114
P2
MGTTXN0_114
R2
MGTTXP1_114
W2
MGTTXN1_114
V2
FTRGLS_P
FTRGLS_N
CU205
0.1uF
CU206
0.1uF
TRGLOUTS_P
TRGLOUTS_N
MGTTXP0_116
B2
MGTTXN0_116
C2
MGTTXP1_116
G2
MGTTXN1_116
F2
FTRGLG_P
FTRGLG_N
CU207
0.1uF
CU208
0.1uF
TRGLOUTG_P
TRGLOUTG_N
MGTTXP0_118
Y2
MGTTXN0_118
AA2
MGTTXN1_118
AD2
MGTTXP1_118
AE2
Title
TID: FPGA GTP Interface
Size
B
Number
11
Revision
Date:
5/11/2011
Sheet of
File:
C:\pcb\TIDrev2\Xc5vlxt665GTP.SchDoc
Drawn By:
GU


Title
TID: Clock Distribution
Size
B
Number
12
Revision
Date: 5/11/2011
Sheet of
File: C:\pcb\TIDrev2\ClockDistr.SchDoc
Drawn By: GU
UC10A
UC10B
NB6L72
UC14
SY55857L
UC15
MC100LVEP111FA
SC1
SW DIP-8
UC13
AD9510BCPZ
UC08
NB4N840MMN
UC07
MC100EP56DT
UC01
250 MHz CLOCK
UC06
SY58607
UC05
SY58607
UC17
NB4N11MDT
V3CLKN
V3PECL
GND

TID: General IO
Title
Size
B
Number
12A
Revision
Date:
5/11/2011
File:
C:\pcb\TIDrev2\GenIO.SchDoc
Sheet of
Drawn By:
GU
JC1
09 18 534 6323
UIO1
UIO2
UIO3
MC100EP90DT
UIO4
UIO5
UIO6
MC100EP91
UC04
UC04A
SY58607
UIO7
UIO8
UIO9
UIO10
SY55855V
FPGA Main Clock
V3PECL
VM5ECL
V3CLKN
GND
CVUC04A
0.22uF
CVUC04B
0.22uF
CUC04
0.1uF
CCUIO1
0.01uF
CCUIO2
0.01uF
CCUIO3
0.01uF
A
B
C
D
1
2
3
4
5
6


250Mbps Manchester Encoder
UT1
MC100LVEP14DT
V3PECL
CLKSEL1
EN
SEL
VCC
CLK0
CLK1
VBB
VEE
Q0
Q1
Q2
Q3
Q4
RGT1 50 TRGLTS_P
RGT2 50 TRGLTS_N
FPGATRIG1_P
RST99A 100 FPGATRIG1_N
CCGT
0.01uF
GND
FADC_TRG_LVDS_P RST155 50
FADC_TRG_LVDS_N RST156 50
F1TRGLVDS_P RST158 50
F1TRGLVDS_N RST159 50
RST157 50
RST160 50
P2TRIG1_P
P2TRIG1_N
TRIG1B_P RST153 150
TRIG1B_N RST154 150
TRIG1A_P RST151 150
TRIG1A_N RST152 150
US1
SY55855V
D0
D0_N
D1
D1_N
GND
Q0_N
Q1_N
RST99X
510
RST99B
RST99C
50
SYNCI_P
SYNCI_N
RST99D
1.02K
CCC99
0.01uF
SYNCFP0_P
SYNCFP0_N
US4
MC100LVEP14DT
CLKSEL8
RST99 100
SYNCRST_P
SYNCRST_N
MANCLKSYNC_P
MANCLKSYNC_N
FADC_SYNC_P
FADC_SYNC_N
F1SYNCLVDS_P
F1SYNCLVDS_N
P2SYNC_P
P2SYNC_N
SYNCA_P RST101 150
SYNCA_N RST102 150
SYNCB_P RST103 150
SYNCB_N RST104 150
US8
MC100LVEP111FA
CLKSEL
RST16 100 SYNCODED_P
SYNCODED_N
MANCLKSYNC_P RST31 50
MANCLKSYNC_N RST32 50
RST31A
50
C34_P RST33 150
C34_N RST34 150
CLKSYNC8_P RST35 150
CLKSYNC8_N RST36 150
CLKSYNC7_P RST37 150
CLKSYNC7_N RST38 150
CLKSYNC6_P RST39 150
CLKSYNC6_N RST40 150
CLKSYNC5_P RST41 150
CLKSYNC5_N RST42 150
CLKSYNC4_P RST43 150
CLKSYNC4_N RST44 150
CLKSYNC3_P RST45 150
CLKSYNC3_N RST46 150
CLKSYNC2_P RST47 150
CLKSYNC2_N RST48 150
CLKSYNC1_P RST49 150
CLKSYNC1_N RST50 150
Q5
Q6
Q7
Q8
Q9
V3CLKN
CCSE13 0.22uF
CCSE12 0.22uF
CCSE11 0.22uF
CTSC1 T520A 10uF
CTSC2 T520A 10uF
CTSC3 T520A 10uF
CCSE01 0.22uF
CCSE02 0.22uF
CCSE03 0.22uF
CCSE04 0.22uF
CCSE05 0.22uF
CCSE06 0.22uF
CCSE07 0.22uF
CCSE08 0.22uF
CCSE09 0.22uF
Title
TID: Sync encoding
Size
B
Number
13
Revision
Date:
5/11/2011
Sheet of
File:
C:\pcb\TIDrev2\SYNCENC.SchDoc
Drawn By:
GU
1
2
3
4
5
6
A
B
C
D


Put the filter cap on the bottom side, beneath the socket
The AC coupling capacitors should be placed near the source (driver)
Front Pannel
TD: #1, global TD
TD: #2
TD: #3
TD: #4
UF1
UF2
UF3
UF4
HFBR7934
UF11
SY58607
UF12
MC100LVEP14DT
V3PECL
V3FIBER
GND
Title
TID: TD interface, additional Optical Transceivers
Size
B
Number
14
Revision
Date:
5/11/2011
Sheet of
File:
C:\pcb\TIDrev2\TDfan.SchDoc
Drawn By:
GU



Put the filter cap on the bottom side, beneath the socket

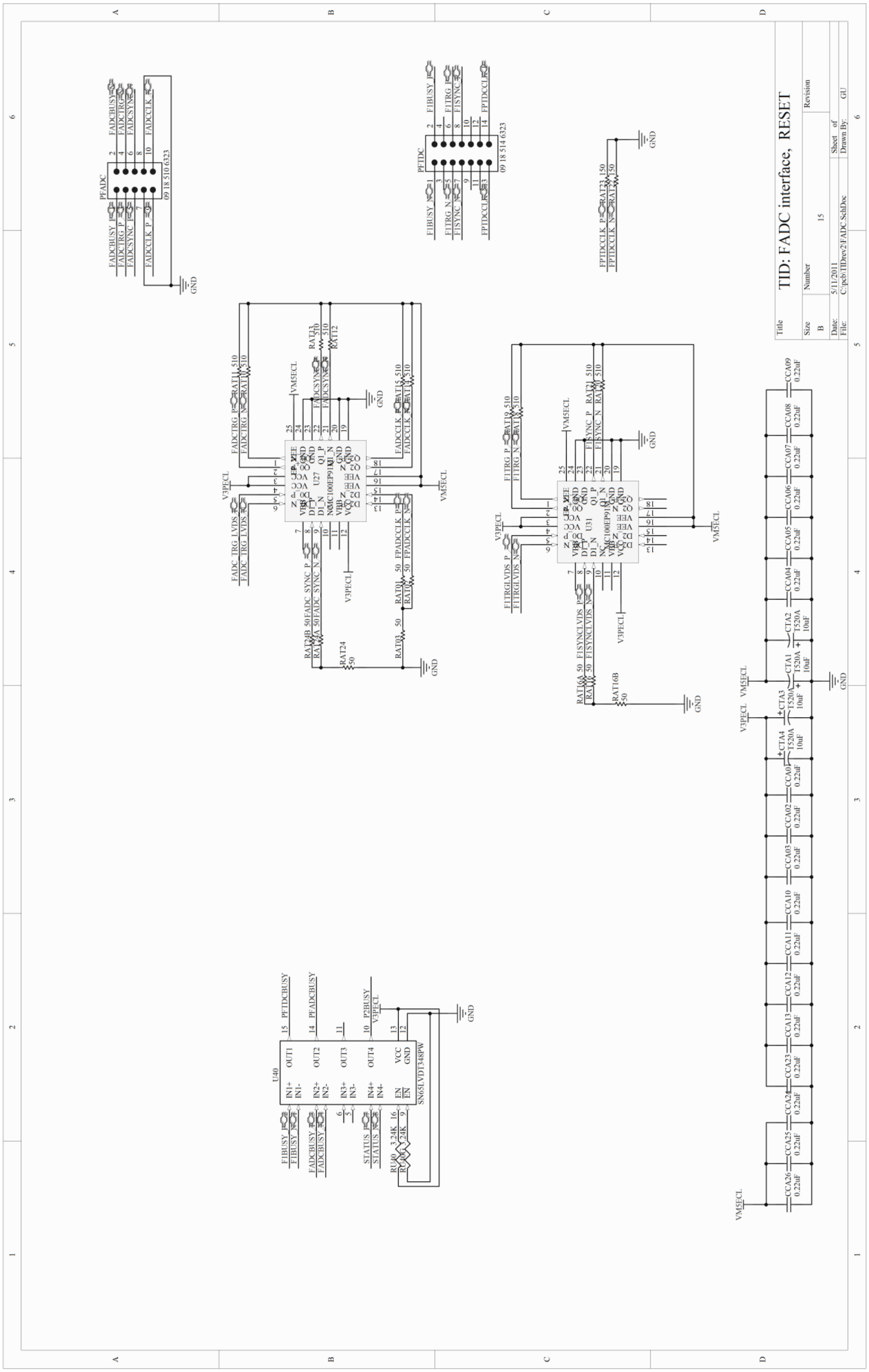
The AC coupling capacitors should be placed near the source (driver)

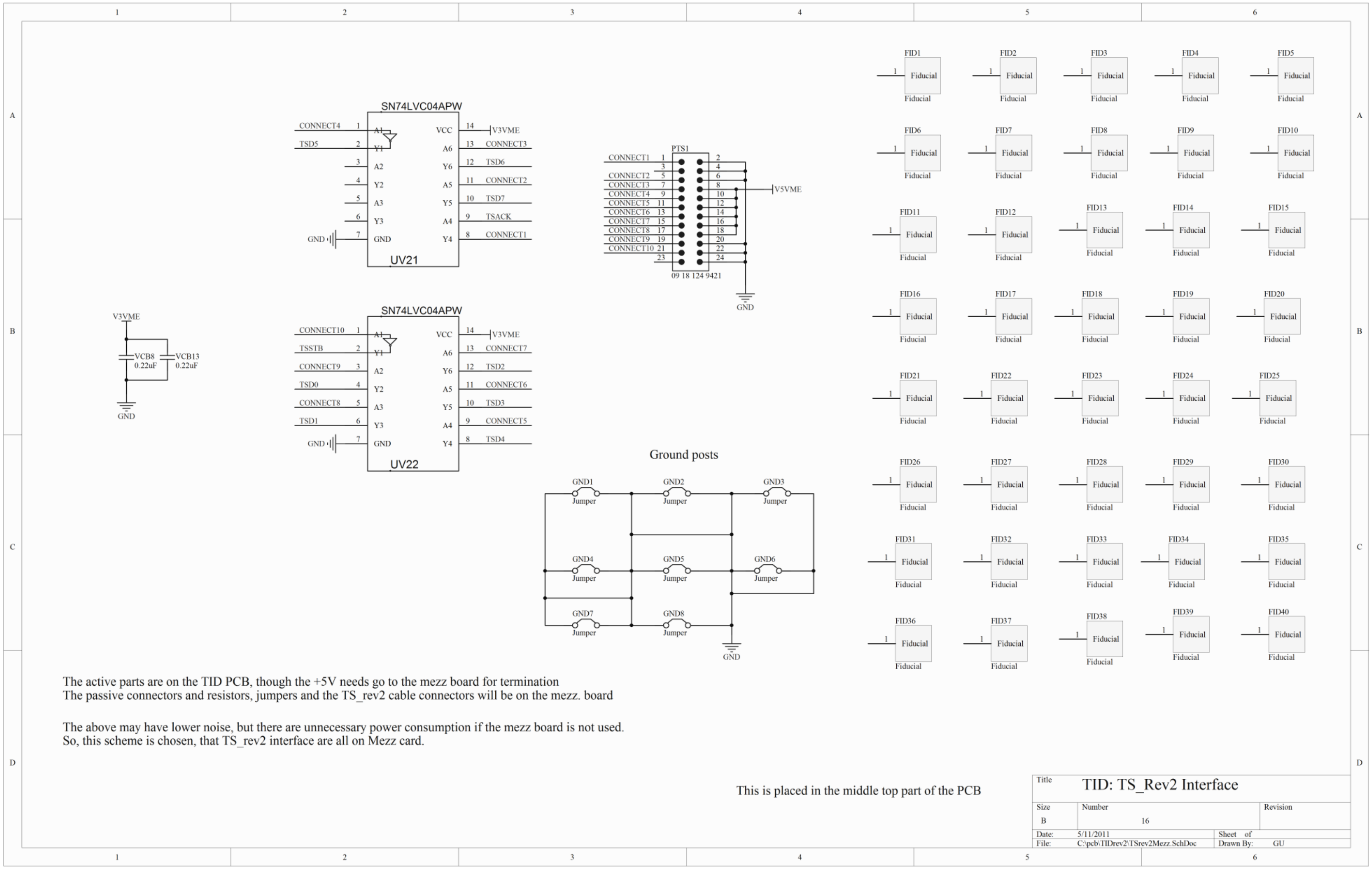
Front Pannel, to be overlapped with ECL IOs, stuff either connectors, but not both
TD: #5, sub-system TD interface
TD: #6
TD: #7
TD: #8

Title
TID: additional Optical Transceivers

Size	Number	Revision
B	14A	

Date: 5/11/2011 Sheet of
File: C:\pcb\TIDrev2\TDfan_noload.SchDoc Drawn By: GU


Title
TID: FADC interface, RESET
Size
B
Number
15
Revision
Date: 5/11/2011
Sheet of
File: C:\pcb\TIIDrev2\FADC.SchDoc
Drawn By: GU
PFADC
09 18 510 6323
FADCBUSY_P
FADCBUSY_N
FADCTRG_P
FADCTRG_N
FADCSYNC_P
FADCSYNC_N
FADCCLK_P
FADCCLK_N
PFTDC
09 18 514 6323
F1BUSY_P
F1BUSY_N
F1TRG_P
F1TRG_N
F1SYNC_P
F1SYNC_N
FPTDCCLK_P
FPTDCCLK_N
U27
MC100EP91
U31
MC100EP91
V3PECL
VM5ECL
GND
FADC_TRG_LVDS_P
FADC_TRG_LVDS_N
FADC_SYNC_P
FADC_SYNC_N
FPADCCLK_P
FPADCCLK_N
F1TRGLVDS_P
F1TRGLVDS_N
F1SYNCLVDS_P
F1SYNCLVDS_N
U40
SN65LVDT348PW
F1BUSY_P
F1BUSY_N
FADCBUSY_P
FADCBUSY_N
STATUS_P
STATUS_N
PFTDCBUSY
PFADCBUSY
P2BUSY
CCA01 CCA02 CCA03 CCA04 CCA05 CCA06 CCA07 CCA08 CCA09 CCA10 CCA11 CCA12 CCA13 CCA23 CCA24 CCA25 CCA26
0.22uF
CTA1 CTA2 CTA3 CTA4
T520A
10uF



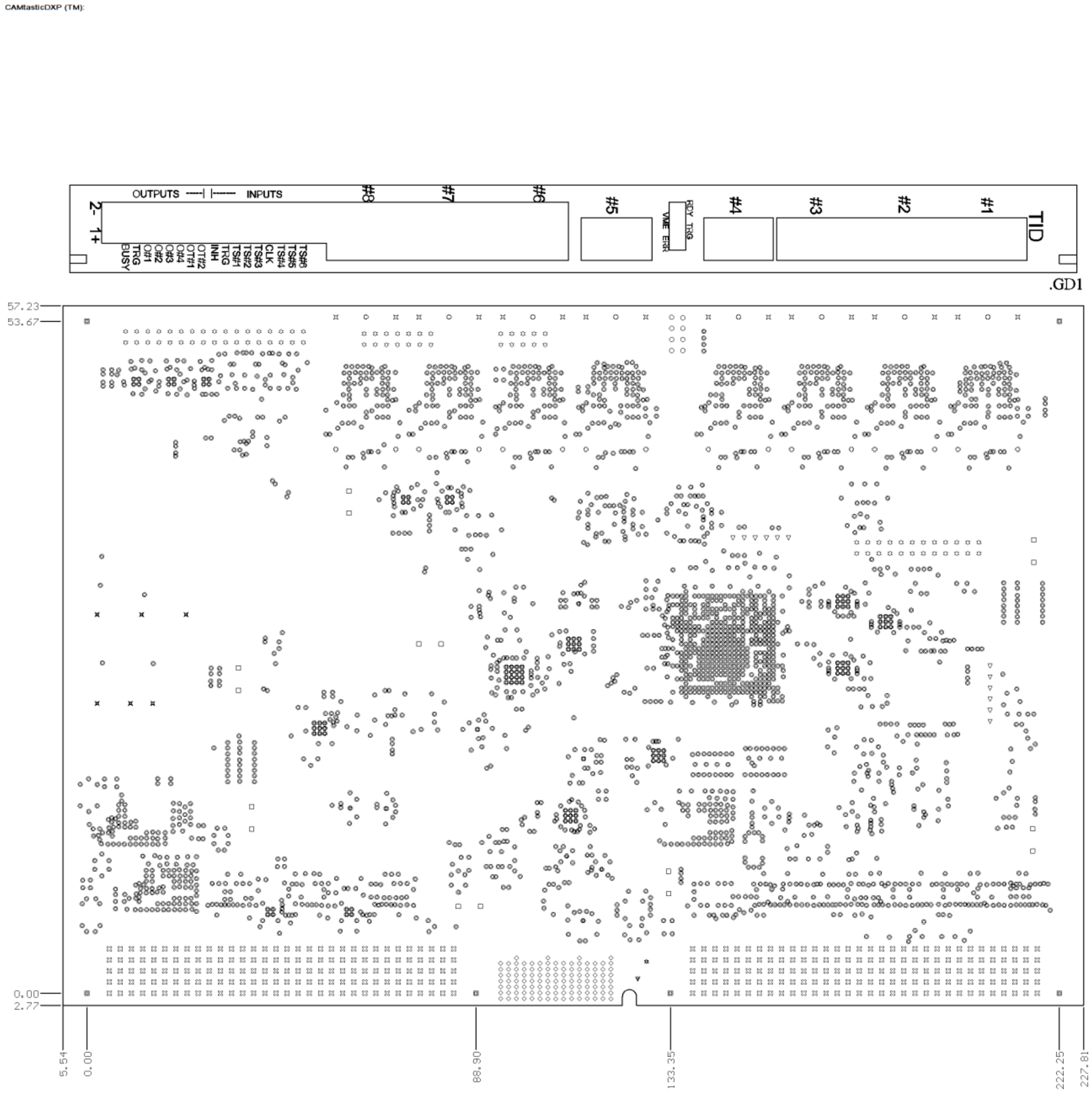
The active parts are on the TID PCB, though the +5V needs go to the mezz board for termination
The passive connectors and resistors, jumpers and the TS_rev2 cable connectors will be on the mezz. board

The above may have lower noise, but there are unnecessary power consumption if the mezz board is not used.
So, this scheme is chosen, that TS_rev2 interface are all on Mezz card.

This is placed in the middle top part of the PCB

Title: TID: TS_Rev2 Interface
Size: B
Number: 16
Revision:
Date: 5/11/2011
Sheet of
File: C:\pcb\TIDrev2\TSrev2Mezz.SchDoc
Drawn By: GU

Appendix B: TID fabrication drawing:



PCB Fabrication Notes & Stackup

1) Board - 12 Layers (8 Signal, 4Plane), Dimensions 233.35mm x 160.00mm, 2 Sided Silkscreen, 2 Sided Soldermask
2) Trace/Width Clearance: 0.127mm/0.254mm
3) 1oz Cu for all internal layers, 1.5oz Cu for outer layers
4) Finish: Electroless Nickle Immersion Gold (ENIG)
5) Impedance Requirements: See Stackup for details
6) All drill hole sizes are specified as finished size.
7) Via hole sizes 0.3mm. to be plugged or tented.
8) Board shall be 100% electrical tested.
9) Soldermask: LPI, SMOBC
10) 1.6mm +/-10% Total Board Thickness
11) Material: Tg>180 C, TD>330 C, z-CTE<15 PPM/C for leadfree FPGA assembly

PCB STACKUP

Layer#	Thickness	Description	Polarity	Filename	SingleEnded Impedance Requirement	Differential Impedance Requirement
		Solderpaste Top		TIDrev2.gtp		
		SilkScreen Top		TIDrev2.gto		
	0.01mm	SolderMask Top		TIDrev2.gts		
1	0.053mm	Top Layer	Positive	TIDrev2.gtl	0.13mm 50ohm +/- 10%	0.13mm Width, 0.254mm Gap -> 100ohm +/- 10%
	0.08mm	dielectric				
2	0.034mm	Ground 1 Plane	Negative	TIDrev2.gp1		
	0.1mm	dielectric				
3	0.034mm	Inner layer 1	Positive	TIDrev2.G1	0.13mm 50ohm +/- 10%	0.13mm Width, 0.254mm Gap -> 100ohm +/- 10%
	0.1mm					
4	0.034mm	Power Plane 1	Negative	TIDrev2.gp2		
	0.1mm					
5	0.034mm	Inner Layer 2	Positive	TIDrev2.G2	0.13mm	0.13mm Width, 0.254mm Gap -> 100ohm +/- 10%
	0.1mm					
6	0.034mm	Inner Layer 3	Positive	TIDrev2.G3	0.13mm	0.13mm Width, 0.254mm Gap -> 100ohm +/- 10%
	0.1mm					
7	0.034mm	Inner Layer 4	Positive	TIDrev2.G4		
	0.1mm					
8	0.034mm	Inner Layer 5	Positive	TIDrev2.G5	0.13mm 50ohm +/- 10%	0.13mm Width, 0.254mm Gap -> 100ohm +/- 10%
	0.1mm					
9	0.034mm	Power Plane 2	Negative	TIDrev2.gp3		
	0.1mm					
10	0.034mm	Inner Layer 6	Positive	TIDrev2.G6	0.13mm 50ohm +/- 10%	0.13mm Width, 0.254mm Gap -> 100ohm +/- 10%
	0.1mm					
11	0.034mm	Ground Plane 2	Negative	TIDrev2.gp4		
	0.08mm					
12	0.053mm	Bottom Layer	Positive	TIDrev2.GBL	0.13mm 50ohm +/- 10%	0.13mm Width, 0.254mm Gap -> 100ohm +/- 10%
	0.01mm	SolderMask Bottom		TIDrev2.gbs		
		SilkScreen Bottom		TIDrev2.gbo		
		Solderpaste Bottom		TIDrev2.gbp		

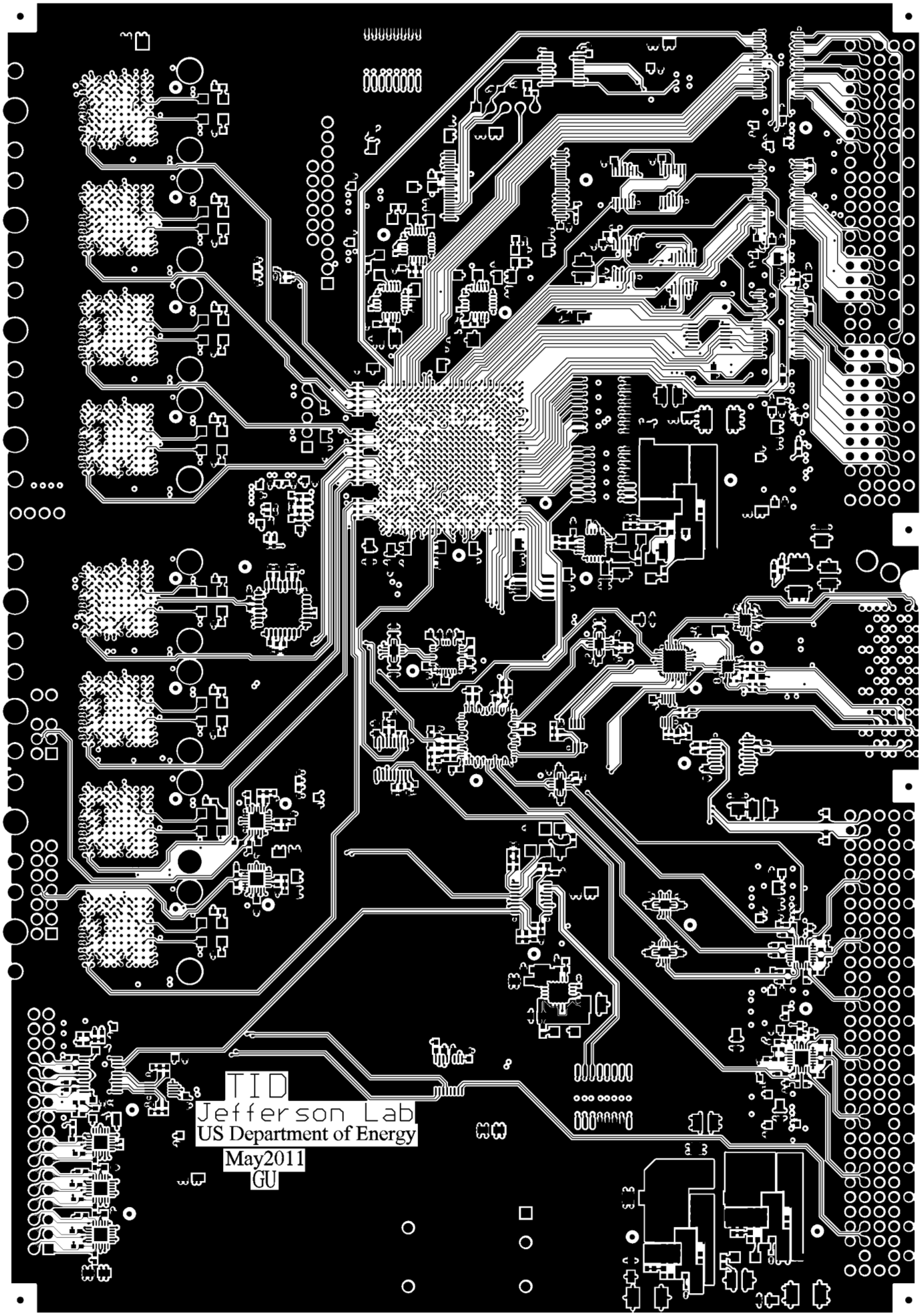
DRILL FILES

(1) TIDrev2.drr - Drill Report File
(2) TIDrev2-plated.txt - NC Drill file for PLATED holes
(3) TIDrev2-nonplated.txt - NC Drill file for NON-PLATED holes
(4) TIDrev2.gd1 - Drill Drawing/Fab Notes

Symbol	Hit Count	Tool Size	Plated	Hole Type
⊙	2903	0.3mm (11.811mil)	PTH	Round
⊕	115	0.33mm (12.992mil)	PTH	Round
◇	109	0.56mm (22.047mil)	PTH	Round
□	16	0.7mm (27.559mil)	PTH	Round
▽	12	0.9mm (35.433mil)	PTH	Round
⊠	320	0.9652mm (38mil)	PTH	Round
✡	82	1mm (39.37mil)	PTH	Round
○	8	1.016mm (40mil)	PTH	Round
⌘	6	1.27mm (50mil)	PTH	Round
⌑	16	1.7018mm (67mil)	PTH	Round
⬡	24	2.6924mm (106mil)	PTH	Round
⊡	6	2.794mm (110mil)	PTH	Round
▼	1	2.794mm (110mil)	NPTH	Round
✲	1	3.2mm (125.984mil)	NPTH	Round
	3619 Total			

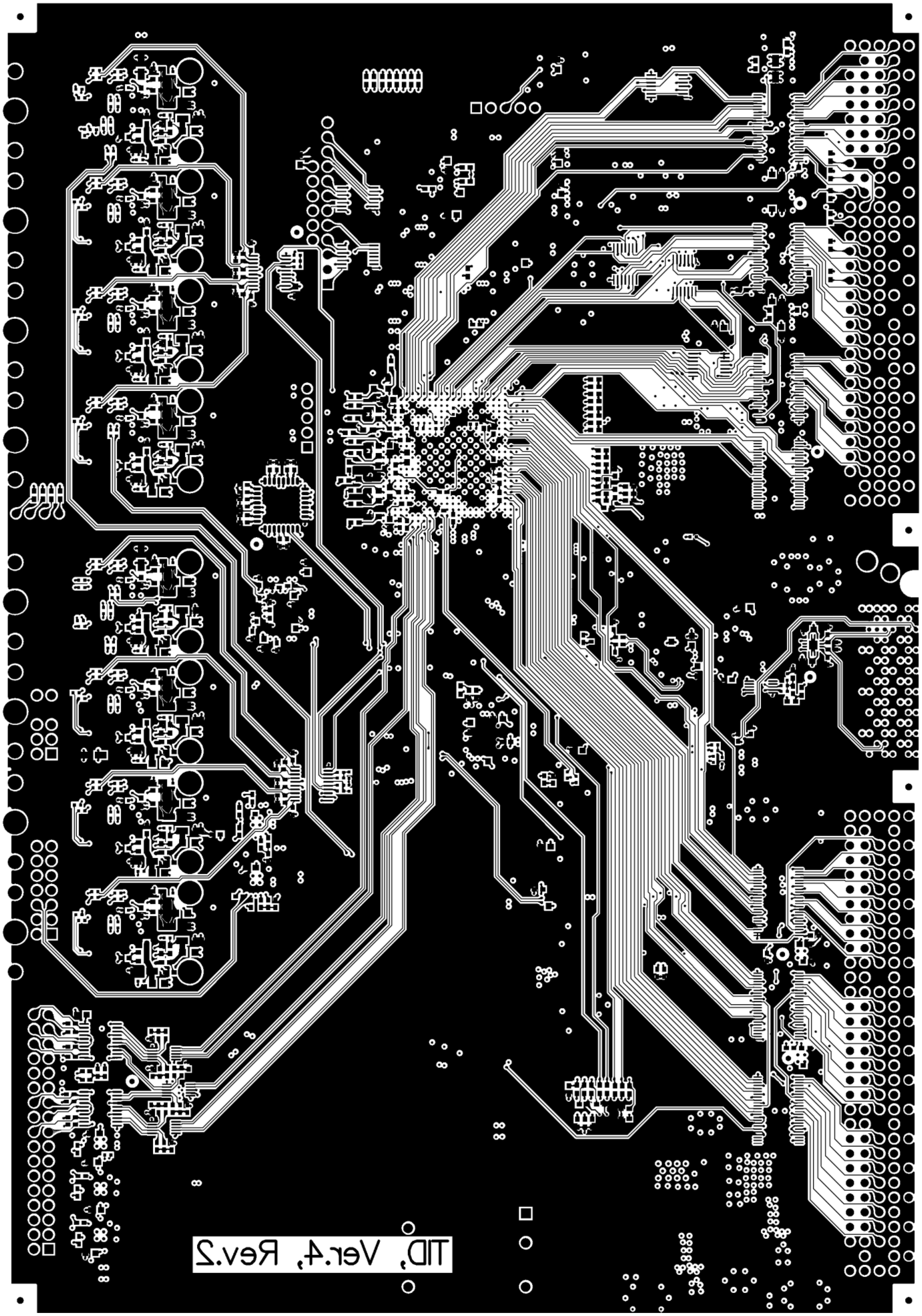
Drilling Details.

.GTL



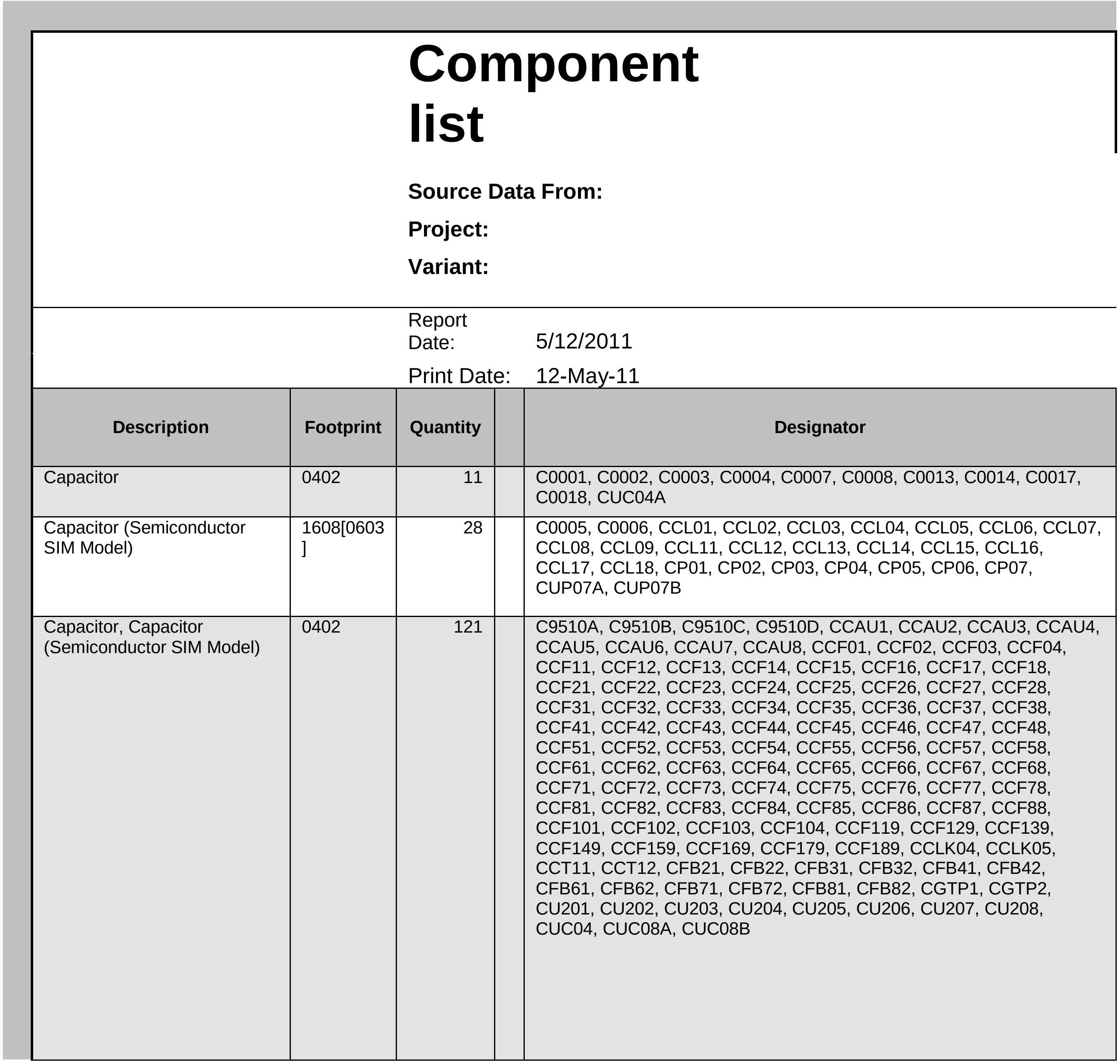
CAMtastic!DXP (TM):

.GBL



CAMtastic!DXP (TM):

Appendix C: Bill of materials:



Component list

Source Data From:

Project:

Variant:

Report Date: 5/12/2011

Print Date: 12-May-11

Description	Footprint	Quantity		Designator
Capacitor	0402	11		C0001, C0002, C0003, C0004, C0007, C0008, C0013, C0014, C0017, C0018, CUC04A
Capacitor (Semiconductor SIM Model)	1608[0603]	28		C0005, C0006, CCL01, CCL02, CCL03, CCL04, CCL05, CCL06, CCL07, CCL08, CCL09, CCL11, CCL12, CCL13, CCL14, CCL15, CCL16, CCL17, CCL18, CP01, CP02, CP03, CP04, CP05, CP06, CP07, CUP07A, CUP07B
Capacitor, Capacitor (Semiconductor SIM Model)	0402	121		C9510A, C9510B, C9510C, C9510D, CCAU1, CCAU2, CCAU3, CCAU4, CCAU5, CCAU6, CCAU7, CCAU8, CCF01, CCF02, CCF03, CCF04, CCF11, CCF12, CCF13, CCF14, CCF15, CCF16, CCF17, CCF18, CCF21, CCF22, CCF23, CCF24, CCF25, CCF26, CCF27, CCF28, CCF31, CCF32, CCF33, CCF34, CCF35, CCF36, CCF37, CCF38, CCF41, CCF42, CCF43, CCF44, CCF45, CCF46, CCF47, CCF48, CCF51, CCF52, CCF53, CCF54, CCF55, CCF56, CCF57, CCF58, CCF61, CCF62, CCF63, CCF64, CCF65, CCF66, CCF67, CCF68, CCF71, CCF72, CCF73, CCF74, CCF75, CCF76, CCF77, CCF78, CCF81, CCF82, CCF83, CCF84, CCF85, CCF86, CCF87, CCF88, CCF101, CCF102, CCF103, CCF104, CCF119, CCF129, CCF139, CCF149, CCF159, CCF169, CCF179, CCF189, CCLK04, CCLK05, CCT11, CCT12, CFB21, CFB22, CFB31, CFB32, CFB41, CFB42, CFB61, CFB62, CFB71, CFB72, CFB81, CFB82, CGTP1, CGTP2, CU201, CU202, CU203, CU204, CU205, CU206, CU207, CU208, CUC04, CUC08A, CUC08B

Capacitor, Ceramic Chip Capacitor - Standard	0603	143		CCA01, CCA02, CCA03, CCA04, CCA05, CCA06, CCA07, CCA08, CCA09, CCA10, CCA11, CCA12, CCA13, CCA23, CCA24, CCA25, CCA26, CCE01, CCE02, CCE03, CCE04, CCE05, CCE06, CCE08, CCE09, CCE10, CCF111, CCF112, CCF114, CCF115, CCF117, CCF118, CCF121, CCF122, CCF124, CCF125, CCF127, CCF128, CCF131, CCF132, CCF134, CCF135, CCF137, CCF138, CCF141, CCF142, CCF144, CCF145, CCF147, CCF148, CCF151, CCF152, CCF154, CCF155, CCF157, CCF158, CCF161, CCF162, CCF164, CCF165, CCF167, CCF168, CCF171, CCF172, CCF174, CCF175, CCF177, CCF178, CCF181, CCF182, CCF184, CCF185, CCF187, CCF188, CCPG1, CCPG2, CCPG3, CCPG4, CCPG5, CCPG6, CCPG7, CCPG8, CCPG92, CCSE01, CCSE02, CCSE03, CCSE04, CCSE05, CCSE06, CCSE07, CCSE08, CCSE08x, CCSE09, CCSE11, CCSE12, CCSE13, CCV01, CCV02, CCV03A, CCV04, CCV05, CCV06, CCV07, CCV08, CCV09, CCV10, CCV11, CCV12, CCV13, CCV14, CCV15, CCV21, CCV22, CCV23, CCV33, CCV36, CCV37, CCV38, CCV39, CCV40, CVUC04A, CVUC04B, VCB1, VCB2, VCB3, VCB4, VCB5, VCB6, VCB7, VCB8, VCB9, VCB10, VCB11, VCB12, VCB13, VCB14, VCB15, VCB16, VCB17, VCB18, VCB19, VCB29, VCB39
Capacitor, Capacitor (Semiconductor SIM Model)	0402	18		CCCF1, CCCF2, CCCFIx, CCCFS, CCGT, CCP1, CCP1_NL, CCP2, CCP3, CCP3_6, CCP4, CCP6, CCPGTP4, CCUIO1, CCUIO2, CCUIO3, CUF12BB, CUF13BB
Solid Tantalum Chip Capacitor, Standard T491 Series - Industrial Grade	A	71		CP1, CP6, CP9, CP9A, CP9B, CP9C, CP9D, CP9E, CP10, CP11, CP95x, CPE1, CPE2, CPF11, CPF12, CPF13, CPF14, CPF22, CPF23, CPF24, CPF32, CPF33, CPF34, CPF42, CPF43, CPF44, CPF51, CPF52, CPF53, CPF54, CPF62, CPF63, CPF64, CPF71, CPF72, CPF73, CPF74, CPF82, CPF83, CPF84, CPL02, CPL03, CPL04, CPL05, CPL06, CPL07, CPL08, CPL09, CPL10, CPL11, CPL12, CPL13, CPL14, CPL15, CPV1, CPV2, CPV3, CPV4, CPV35, CPV36, CTA1, CTA2, CTA3, CTA4, CTPG1, CTPG2, CTSC1, CTSC2, CTSC3, VCA1, VCA2
Solid Tantalum Chip Capacitor, Standard T491 Series - Industrial Grade, Solid Tantalum Chip Capacitor, Standard T520 Series - Industrial Grade	B	9		CP2, CP3, CP4, CP5, CP7, CP7X, CP20, CPL01, CPL20
Solid Tantalum Chip Capacitor, Standard T491 Series - Industrial Grade	B	1		CP5_NL
Typical RED, GREEN, YELLOW, AMBER GaAs LED	3.2X1.6X1.1	24		DF11, DF12, DF21, DF22, DF31, DF32, DF41, DF42, DF51, DF52, DF61, DF62, DF71, DF72, DF81, DF82, DP1, DP2, DP3, DP3_4, DP4, DP5, DPG1, DPG5
	EC5BE17	1		EC34
FUSE 5A SLO BLO NANO 2 SMD	NANO_FUSE	3		F5, F12, F15
	fiducial	40		FID1, FID2, FID3, FID4, FID5, FID6, FID7, FID8, FID9, FID10, FID11, FID12, FID13, FID14, FID15, FID16, FID17, FID18, FID19, FID20, FID21, FID22, FID23, FID24, FID25, FID26, FID27, FID28, FID29, FID30, FID31, FID32, FID33, FID34, FID35, FID36, FID37, FID38, FID39, FID40

FUSE 5A SLO BLO NANO 2 SMD	NANO_FUSE	1		FP1
Header, 6-Pin	HDR1X6	2		FPGA_JTAG, PROM_JTAG
Jumper Wire	RAD-0.2	8		GND1, GND2, GND3, GND4, GND5, GND6, GND7, GND8
Flat Cable Connector (IDC), Low-Profile Male Header, Angled Solder Pin, 34 Contacts, Performance Level 2	918534x323	1		JC1
INDUCTOR 1.0UH 300MA 20% 0805	0805	24		LF11, LF13, LF15, LF21, LF23, LF25, LF31, LF33, LF35, LF41, LF43, LF45, LF51, LF53, LF55, LF61, LF63, LF65, LF71, LF73, LF75, LF81, LF83, LF85
INDUCTOR 6.8NH 10% 0603 SMD	0603	24		LF12, LF14, LF16, LF22, LF24, LF26, LF32, LF34, LF36, LF42, LF44, LF46, LF52, LF54, LF56, LF62, LF64, LF66, LF72, LF74, LF76, LF82, LF84, LF86
Inductor	L0603	17		LL01, LL02, LL03, LL04, LL05, LL06, LL07, LL08, LL09, LL11, LL12, LL13, LL14, LL15, LL16, LL17, LL18
Inductor	1210	9		LP1, LP2, LP3, LP4, LP5, LP10, LP11, LP20, LP33
VME160-P1	VME160	1		P1
VME160-P2	VME160	1		P2
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W, Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	2-0402	45		P2R1, P2R2, P2R3, P2R4, P2R5, P2R6, P2R7, P2R8, P2R9, P2R10, P2R11, P2R12, RAT10, RAT11, RAT12, RAT13, RAT14, RAT15, RAT18, RAT19, RAT20, RAT21, RCT41X, RIO11, RIO12, RIO13, RIO14, RIO15, RIO16, RIO17, RIO18, RIO21, RIO22, RIO23, RIO24, RIO25, RIO26, RIO27, RIO28, RP12, RP12x, RP16, RPG12, RPG12x, RST99X
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W, Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	2-0402	112		P2R21, P2R22, P2R23, P2R24, P2R25, P2R26, P2R27, P2R28, P2R29, P2R30, P2R31, P2R32, P2R33, P2R34, P2R35, P2R36, P2R37, P2R38, RAT01, RAT02, RAT03, RAT16, RAT16A, RAT16B, RAT24, RAT24A, RAT24B, RC20, RC30, RC30a, RC31, RC32, RC33, RC43, RC44, RC46, RC47, RC48, RC48a, RC49, RC101, RCT17, RCT18, RCT19, RCT30, RCT31, RCT32, RCT43, RCT44, RCT45, RCT48, RCT49, RIO1, RIO2, RIO3, RIO4, RIO5, RIO6, RIO7, RIO8, RIO9, RIO31, RIO32, RIO33, RIO34, RIO35, RIO36, RIO37, RIO38, RIO39, RIO41, RIO42, RIO43, RIO44, RIO45, RIO46, RIO47, RIO48, RIO51, RIO52, RIO53, RIO54, RIO55, RIO56, RIO57, RIO58, RIO61, RIO62, RIO63, RIO64, RIO65, RIO66, RIO67, RIO68, RST31, RST31A, RST32, RST155, RST156, RST157, RST158, RST159, RST160, RT1, RT2, RT3, RT4, RT5, RUC04, RVP0, RX02, RX02F
Flat Cable Connector (IDC), Low-Profile Male Header, Angled Solder Pin, 10 Contacts, Performance Level 2	918510x323	1		PFADC
Flat Cable Connector (IDC), Low-Profile Male Header, Angled Solder Pin, 14 Contacts, Performance Level 2	918514x323	1		PFTDC
P0-PL-VXS	P0-105_P0-	1		PP0

	PL-VXS			
Flat Cable Connector (IDC), PCB Transition Connector, 2 Rows, Kinked Solder Pin, 24 Contacts	9181249421	1		PTS1
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W, Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	2-0402	80		RAT22, RAT23, RC11, RC12, RC13, RC14, RC15, RC16, RC17, RC18, RC19, RC21, RC22, RC23, RC24, RC25, RC26, RC27, RC28, RC29, RCT46, RCT47, RCT51, RCT51A, RCT51B, RCT52, RCT52A, RCT52B, RF90, RF91, RF92, RF93, RF94, RF95, RF96, RF97, RF98, RF99, RF101, RF102, RF103, RF104, RF105, RF106, RF107, RF108, RF109, RF110, RP6y, RPG8, RST33, RST34, RST35, RST36, RST37, RST38, RST39, RST40, RST41, RST42, RST43, RST44, RST45, RST46, RST47, RST48, RST49, RST50, RST101, RST102, RST103, RST104, RST151, RST152, RST153, RST154, RUP06A, RUP06B, RUP06C, RUP06D
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W, RES 100 OHM 1/16W 1% 0402 SMD, Resistor	0603	85		RC01, RC06, RC07, RC08, RCT42X, RCTR2A, RCTR3A, RCTR3B, RCX01, RCX02, RCX03, RCX04, RCX09, RCX10, RCX11, RE01X, RE06X, RF11, RF12, RF14, RF16, RF18, RF21, RF22, RF24, RF26, RF28, RF31, RF32, RF34, RF36, RF38, RF41, RF42, RF44, RF46, RF48, RF51, RF52, RF54, RF56, RF58, RF61, RF62, RF64, RF66, RF68, RF71, RF72, RF74, RF76, RF78, RF81, RF82, RF84, RF86, RF88, RI2C1, RI2C2, RI2C3, RI2C4, RI2C5, RI2C6, RP3_14, RP4, RP6, RP6x, RP9y, RP11, RP13, RP14, RP15, RPG11, RPG13, RS16, RS17, RS18, RS21A, RS22A, RS23A, RS24A, RST99D, RV02xy, RV04X, RV12xy
Resistor	0603	88		RC02, RC03, RC04, RC05, RCT50A, RCTR1, RCTR2, RCTR3, RCX05, RCX06, RCX07, RCX08, RCX12, RCX13, RCX14, RE01, RP2, RP3, RP3_15, RP3_16, RP3NL, RP3NLA, RP3x, RP5, RP9, RP9z, RP10, RP101, RP102, RP103, RP104, RP105, RP106, RP107, RP108, RP109, RP110, RP111, RP112, RPG2, RPG3, RPG4, RPG5, RPG6, RPG7, RPG9, RPG10, RPG11A, RPGCLK3, RS1, RS2, RS3, RS4, RS5, RS6, RS7, RS8, RS11, RS12, RS13, RS14, RS15, RS21, RS22, RS23, RS24, RS25, RS26, RS27, RS28, RTS19, RU40, RU40G, RUSFM, RV01, RV01x, RV02, RV02x, RV03, RV04, RV05, RV05x, RV07, RV07A, RV08, RV12x, RV12yz, RV44
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W	0402	8		RCT09, RCT10, RCT11, RCT12, RCT13, RCT14, RCT15, RCT16
Precision Thick Film Chip Resistor, 10 Ohm to 1M Ohm Range, 1% and 0.5% Tolerance, 0402 Size, 0.063 W, RES 100 OHM 1/16W 1% 0402 SMD, Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	0402	16		RCT41, RCT42, RGT1, RGT2, RST99B, RST99C, RTD0x, RTD01, RTD02, RTD03, RTD04, RTD05, RTD05X, RTD06, RTD07, RTD08

Resistor	0603	1		RE05X
RES 100 OHM 1/16W 1% 0402 SMD, Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	0402	32		RF13, RF15, RF17, RF23, RF25, RF27, RF33, RF35, RF37, RF43, RF45, RF47, RF53, RF55, RF57, RF63, RF65, RF67, RF73, RF75, RF77, RF83, RF85, RF87, RIO19, RIO29, RST16, RST99, RST99A, RT4A, RT4B, RT4C
Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	0402	6		RID01, RID02, RID03, RID04, RPGCLK_NL, RPGD01_NL
Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	0402	8		RID11, RID12, RID13, RID14, RID15, RID16, RPGCLK2, RPGD02
Thick Film Chip Resistor, 1 Ohm to 2.2M Ohm Range, 5% Tolerance, 0402 Size, 0.063 W	2-0402	4		RIO33x, RIO33y, RIO33z, RUC04A
DIP Switch, 8 Position, SPST	SW16_L	4		S1, S2, SC01, SC1
AD9510	CP-64-1_N	1		U13
IC 11-BIT I-WS BUS TXRX 48-TSSOP	TSSOP50P810-48AL	1		U17
Xilinx Virtex-5 LXT Platform FPGA, 665-Ball FFBGA, Speed Grade 1, 360 User I/Os, Commercial Grade	FF665	1		U20
On Semiconductor, Any level positive to ECL translator	QFN50P400X400-24W4M	7		U27, U31, UIO4, UIO5, UIO6, UVP21, UVP22
4 Channel ECL/PECL/LVDS -> LVTTL	TSSOP-16	1		U40
CCPD-034	SO6-5X7	1		UC01
Any level in, LVPECL out 1:2 fanout	QFN50P300X300-16V7N	6		UC04, UC04A, UC05, UC06, UF11, UP06
4:1 Differential Multiplexer	948E-02_L	1		UC07
ON-Semi Dual 2 X 2 CrossSwitch	RHB32_N	1		UC08
2x2 crosspoint switch with LVPECL output	QFN50P300X300-16V4N	2		UC10A, UC10B
Micrel dual Anylevel to LVPECL translator	TSSOP50P490-10AN	1		UC14
Low-Voltage 1:10 Differential LVECL/LVPECL/LVEPECL/HSTL Clock Driver	873A-02_L	2		UC15, US8
Differential to CML buffer	846A-02	1		UC17

	TSSOP14	4		UE01, UE02, UE07, UE08
	TSSOP14	2		UE03, UE05
	TSSOP14	2		UE04, UE06
	TSSOP14	3		UE09, UV21, UV22
	TSSOP20	1		UE10
HFBR7934	84512-102LF	8		UF1, UF2, UF3, UF4, UF5, UF6, UF7, UF8
Low-Voltage 1:5 Differential LVECL/LVPECL/LVEPECL/HSTL Clock Driver	948E-02_N	4		UF12, UF13, US4, UT1
Triple ECL to PECL Translator	948E-02_N	3		UIO1, UIO2, UIO3
Dual LVPECL to LVDS translator	TSSOP50P490-10AN	5		UIO7, UIO8, UIO9, UIO10, US1
LUMEX, Quad pack LEDs	LED14	1		ULED
LTM4604EV	LGA-66_LTM4604EV(Primary)	3		UP1, UP1_NL, UP3
IC LDO REG 3.0A W/SS 20-VQFN	QFN-20	5		UP2, UP4, UP5, UP33, UPG5
Analog 1.25Gbps Clock and Data Recovery IC	QFN50P500X500-32W2N	1		UP07
Miniature Oscillator	CFPX-5	1		UPG1
XCF00P Series, Platform Flash In-System Programmable Configuration 1.8V PROM, 48-Pin TSSOP, 32-Megabit, Commercial Grade	VO48	1		UPG2
Atmel flash memory	8S1_N	1		USFM
IC UNIV BUS TXRX TRI-ST 48-TSSOP	TSSOP50P810-48AL	9		UV1, UV2, UV3, UV4, UV5, UV6, UV10, UV12, UV14

Appendix D: Glossory:

TID: Trigger Interface and Distribution module; a PCB design can be configured as TI, TD, TS or TM;

TI: Trigger Interface module; It seats in payload slot#18 in front end crates, interfaces the trigger and the DAQ system; It is one stuffing variation of the TID.

TD: Trigger Distribution module; It seats in payload slot#1-16 in the global trigger distribution and fans out the TRIGGER/CLOCK/SYNC to eight TIs; it is one stuffing variation of the TID.

TS: Trigger Supervisor; It seats in payload#18 in the global trigger distribution crate; It is the interface between DAQ and trigger system; A simplified (pre-prototype) TS can be stuffed from a TID;

TM: TID Master. It is used in the subsystem test or commissioning setup; It generates TRG/CLK/SYNC as a TS, sends TRG/CLK/SYNC to P0 and P2 like a TI, and fans out TRG/CLK/SYNC through fiber to other TI like a TD.

SD: Signal Distribution module; It fans out TRG/CLK/SYNC from payload slot#18 to payload slots#1-16; It has clock jitter cleanup capability.

GTP: Global Trigger Processor module.

CTP: Crate Trigger Processor module.

DAQ: Data Acquisition.

ROC: Readout Controller; A VME CPU module used to readout the front end data through VME bus.

VXS: VME Switched Serial; A VME extension with dual-star serial switch slots.

MGT: Multiple Gbps Transceiver; A builtin transceiver module in Xilinx FPGA. In XC5VLX30T FPGA, it supports up to 3.125 Gbps.

Appendix E: TID data format:

The TID data is formatted in blocks of events. Each Trigger_1 is one event. A block of data contains a predefined number (the number could be 1) of triggers. Each block has block header, block trailer, possible place holder, and event data. The data format is summarized here:

Block headers
  Event#1 data
  Event#2 data
  ……
  Event#N data
Optional data
Block trailer

```
Block Header#1:
  bit(31:28): 0001;
  Bit(27:22): CrateID, which is set by register A24 offset 0x00;
  Bit(21:16): BoardID, the VME64x geographic address;
  Bit(15:8): block number;
  Bit(7:0): block size;

Block Header#2:
  Bit(31:8): 0x0f0120;
  Bit(7:0): Block size;

Block Trailer#1:
  Bit(31:28): 0010;
  Bit(27:16): floating, I guess that they default to 0;
  Bit(15:0): Word count; as suggested by Dave, some data do not count.

Extra word:
  0xF0DA0BAD

Dummy word:
  bit(31:16): 0x965A;
  Bit(15:0): Block number

Event data word1: (event header)
  Bit(31:24): Trigger Type;
  Bit(24:2): 0000,0001,0000,0000,0000,00
  Bit(1:0): Event wordcount; as suggested by Dave, some data do not count

Event data word2:
  Bit(31:0): trigger number; counting from 0 to be consistent with wrap
around;

Event data word3:
  Bit(31:0): trigger timing; 16ns step

Event data word4:
  Bit(31:16): Current trigger data (received data from fiber trigger_link as TI);
  Bit(15:0): Current trigger data (sent data from fiber trigger_link as TS)
```

Appendix F: Document revision history:

Updated on Apr. 20th, 2010

Updated on May 13th, 2010

Updated on May 19th, 2010: add the trigger acknowledge in the status word;

Updated on July 6th, 2010: Define the TI/TD mode in section 5.2.2;

Updated on Sept. 20th, 2010: Re-define the A24 address space;

Updated on Oct. 15th, 2010: Added Busy_Input_Enable (A24, 0x0004);

Updated on Oct. 18th, 2010: updated the Emergency loading after tests;

Updated on Jan. 13th, 2011: Add examples for VME trigger word loading;

Updated on Feb. 2nd, 2011: clarify the A24 0x00-0x1C registers;

Updated on Mar. 21st, 2011: further updates on registers to match with the firmware;

Updated on Mar. 25th, 2011: Added the software setup procedure section, with some updates on the registers;

Updated on Apr. 5th, 2011: Register offset 0x14 and 0x2C update.

Updated on Apr. 18th, 2011: Enables for each GTP input bits, CLK250 source selection

Updated on Apr. 20th, 2011: added the Sync decoding, and two more A24 read registers;

Updated on May 12th, 2011: Added the PCB schematics, fab layers, and BOM as appendix A, appendix B and appendix C.

Updated on June 6th, 2011: Added A24 offsets 0x38 and 0x3C for extra readout (v10)

Updated on June 22nd, 2011: Redefined A24, 0x08 and 0x30 registers;

Updated on Aug. 18th, 2011: Overall revision to add the TM description, Glossary and data format;