VXS P0 fast link design

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I. Descriptions of the asynchronous design

The link is asynchronous and simplex. The data are serialized at 50 MHz at the transmitter, and the data are deserialized at the receiver with 250 MHz oversampling clock. There is almost no requirement on the oscillator's stability.

Two VHDL modules are developed: AsyncTx.vhd for data serialization, and AsyncRx.vhd for data deserialization. The schematic symbol for AsyncTx is shown in figure 1. The input/Output ports are listed in Table 1.
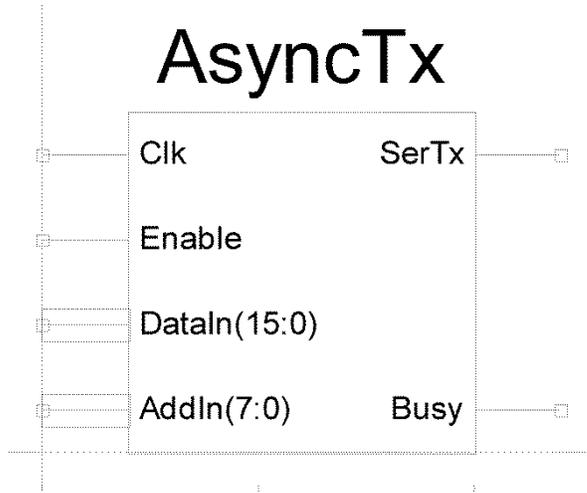

Figure 1 Schematic symbol for module AsyncTx

Table 1 Port description for AsyncTx

Port Name	In/Out	Description
Clk	In	Transmitter clock, 50 MHz nominal
Enable	In	synced with Clk, enable the data transfer if the Busy is LOW
DataIn(15:0)	In	16-bit data
AddIn(7:0)	In	8-bit address for the data

SerTx	Out	Serialized data, which is bit synced with Clk
Busy	out	indicates that the AsyncTx block can not accept new data/address

The schematic symbol for AsyncRx module is shown in figure 2, and the input/output ports for AsyncRx modules are summarized in table 2:
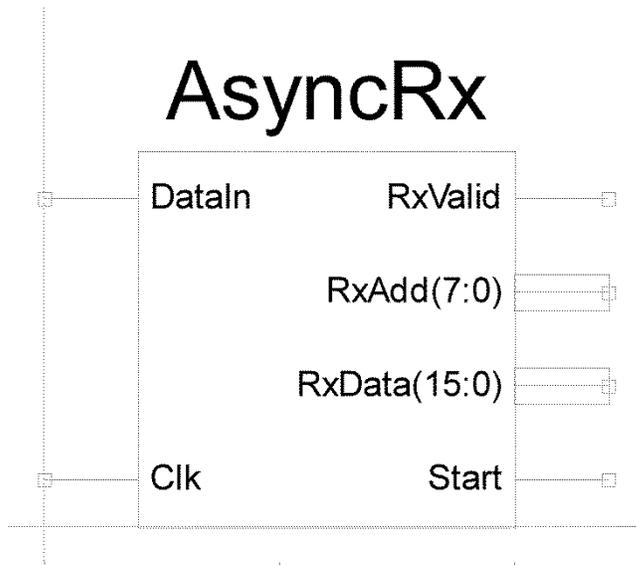

Figure 2 Schematic symbol for AsyncRx

Table 2 Ports description for AsyncRx module

Port name	In/out	Description
DataIn	In	Serial data input
Clk	In	Oversampling clock, 250 MHz nominal (five times of the Tx clock)
RxValid	Out	synced with Clk (250 MHz) to validate the received data
RxAdd(7:0)	Out	deserialized 8-bit address
RxData(15:0)	Out	Deserialized 16-bit data
Start	Out	detected START bit in the serial data stream

II. Serialized Data format

The serialized data include START bit(s), PAYLOAD (address and data), IDLES. The format is shown in figure 3. The serial data are summarized in table 3.
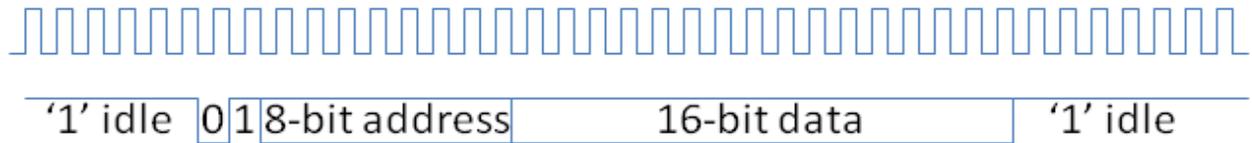

Figure 3 Serialized data format

Table 3 serialized data components

IDLE	more than 26 bits of consecutive '1' (at 50 MHz), the line stays high for more than 520ns,
START	"01", a single bit '0' is enough, but two bits are reserved for future compatibility
PAYLOAD	right now, they are 8-bit address and 16-bit data

III. Usage in VXS crate

The AsyncTx will be implemented on the transmitter (CTP/GTP/SD), and the AsyncRx will be implemented on the receiver (TI/TS) connected by one pair of the differential lines using LVDS (or BusLVDS). The receiver (TI or TS) will be readout using VME A24D32. Offsets 0x02000-0x021FC are for VXS switch slot#B (SD card), and A24 offsets 0x02800-0x029FC are for VXS switch slot#A (CTP card or GTP card).

There is no feedback on the serial data link. The Receiver updates its memory after decoding the data. The data is updated 16-bit wide. The VME reads out 32-bit wide by combining the neighboring two 16-bit data words (write address 2n and write address 2n+1).

IV. Future improvement

The current scheme, that is serial data is 50Mbps, and the effective payload (data plus address) transfer is >20Mbps, is fast enough for our need. The link can be optimized for more efficient data transfer.

➢ It is possible to change the 16-bit data into 32-bit data to increase the data payload ratio from 67% to 80%;

- The easiest way to increase further the payload efficiency (40% right now) is to decrease the idle data, which is used to separate the data packets. If the data encoding is used, the idle can be as short as one byte (8b/10b encoding), and there is no need for the start bit(s). The payload efficiency will be 80%(encoding)*75%(idle payload)=60% for 8-bit address and 16-bit data. If the 8b/10b encoding is used, the payload efficiency can be further increased by longer payload packets.
- The DDR feature can be used to further increase the data transfer speed without increasing the clock speed
- Synchronized clocks can be used on the transmitter and the receiver. The transmitter clock can easily reach 250MHz. But this is synchronous link, not asynchronous link.