Jefferson Science Associates

Thomas Jefferson National Accelerator Facility

Physics Division -- *Fast* Electronics Group

Description and Instructions
for the
Fast LED Pulser (FLP) Board

15 February 2015

Hai Dong
Jeff Wilson
Vladamir Popov
Chris Cuevas

1.0 Introduction

There is a need for a very fast Light Emitting Diode programmable pulser for the Hall B Central Time Of Flight and High Threshold Cerenkov Counter. [CTOF and HTCC respectively] These detector systems rely on photomultiplier tubes to convert photons released from scintillator material or Cerenkov light to electrical signals.

LEDs can be pulsed with precision and very fast rise times that rival expensive laser devices. One important advantage of an LED pulser system is that the personnel safety hazards are minimal compared to a high speed laser device.

Probably can fill in more details here later,,,

2.0 Requirements and Purpose of Circuit

Two completely separate pulser circuits are required and the output signals will be connected by a DB9 female connector. The outputs will have the programmable features as described below:

Outputs: [Pulser1 and Pulser2 are identical:]
- DB9 female connector; Front panel
- 3.2-5.5 VDC @ 300 mA, 16.25 mV step resolution
- 3.2-5.5 VDC @ 300 mA, 16.25 mV step resolution
- 3.2-8.0 VDC @ 300 mA, 32.55 mV step resolution
- 40 ns TTL (4.5V into 50 Ohm load) Pulse Trig1, 2 with Programmable Pulse Repetition Rate from 100 Hz to 20 KHz. Pulse signal is available at output Lemo connector

Inputs:
- TTL level, max frequency of 50MHz for pulser 1 and pulser 2 on front panel Lemo connectors.

Monitors:
- The precision DC level outputs are available for VME readback with 10 bit resolution at 188Ksps

Interfaces:
- Support VME 16. VME 64 capable if P2 is populated.
- 1 Gb Ethernet

Power Supply:
- VME 12V @ 1Amp
- Power Adapter 12-15V @ 1 Amp [Stand alone mode]

Form factor:
- Stand alone desktop chassis
- 6U x 160mm single width VME board

Please reference Figure 1 that shows the schematic for the LED configuration. The LEDs are arranged in a group of 6, and the three programmable DC voltage levels are connected to the stages of the LED driver circuit.[V1, V2, VLed] The programmable TTL pulse output drives the input to the LED drive circuit.

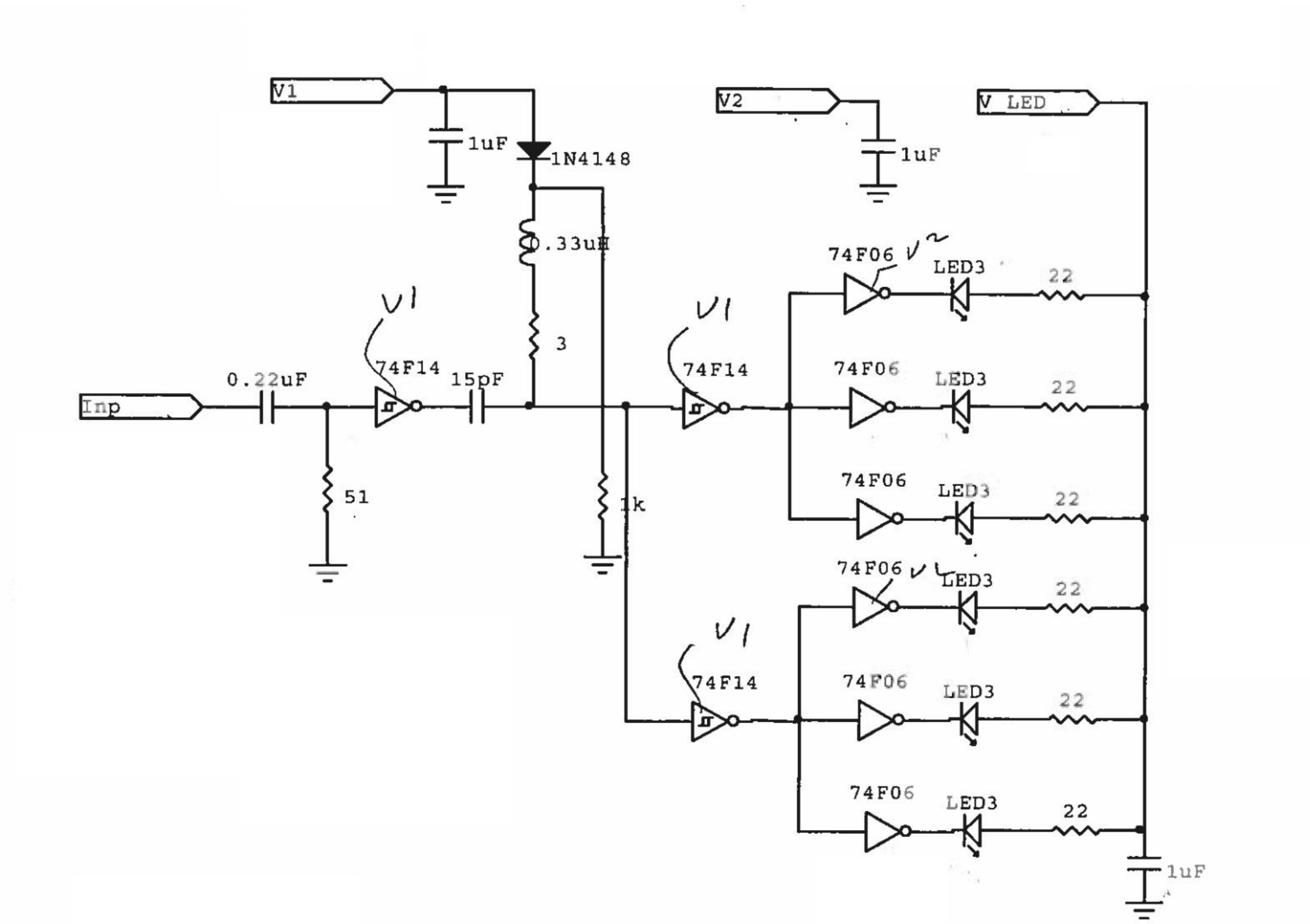


Figure 1: LED drive circuit. [V. Popov]

3.0 Detailed Functional Description

The fast LED programmable pulser circuit board is comprised of the following sections:

3.1 Power supply

The board requires +5V and +12V DC power. The +12V power the variable voltage outputs regulators (V1,V2,Vled) . The +5V power everything else on boards.

3.2 Control Circuit.

The board is controlled by Xilinx Artix

3.2 VME interface

Even though VME hardware interface fully supports VME64, firmware supports VME A24 D16 protocol.

3.3 Ethernet Interface

Ethernet interface only support 10BaseT 1Gig Ethernet connection. The firmware supports Ethernet UDP and Ping protocols. Connect Ethernet cable to J1 connector.

3.4 FPGA configuration and status registers

- All configuration and status registers are 16 bits registers.
- The address of the registers is the base address which is defined by U53 DIP switches A23 to A18 and U54 DIP switches. A17 to A12. When a switch is set toward the back of the board (toward P7) the corresponding VME address bit is a zero.

- For example:
  - U53 A23 to A19 are set toward the back (00000) and A18 is set toward the front (1).
  - U54 A17 and A14 are set toward the back (0000) and A13 to A12 are set toward the front (11).
  - The VME base address is 0x043000. The address for Config1 and Config9 are 0x043002 and 0x043012 respectively.

3.5 DC precision outputs

Voltage for V1, V2, and V LED are driven by Texas Instrument LM1117SX adjustable linear regulator as shown in Figure 2. The voltage is adjusted by setting the resistance of R3 (MCP4151 IC). VReg is connected to connector J3 and J4 to drive V1, V2, and Vled via JFET as shown in Figure 4.

- VReg voltage is equal to Vref(1+(R2+R3)/R1) + IADJ(R2+R3) where Vref = 1.25, Iadj = 60 uA9, R1=1.5K, R2=2.1K.
- Solving for R3 = (V1,2,Led – 3.126) / .00089333.
- MCP4151 (R3) for V1 and V2 are 5 KOhm digital potentiometers with 256 values (19.53125 Ohm per step). Set value for digital potentiometer for V1,V2 = R3/19.53125.
- MCP4151 (R3) for VLed is 10 KOhm digital potentiometers with 256 values (39.0525 Ohm per step). Set value for digital potentiometer for Vled = R3/39.0525.
- The Set Value for digital potentiometer for V1, V2 is limited in firmware to 0x88 correspond to 5.5V
- The Set Value for digital potentiometer for Vled is limited in firmware to 0x8B correspond to 8.0V
- V1, V2, Vled output are within 2% of the set value.
-

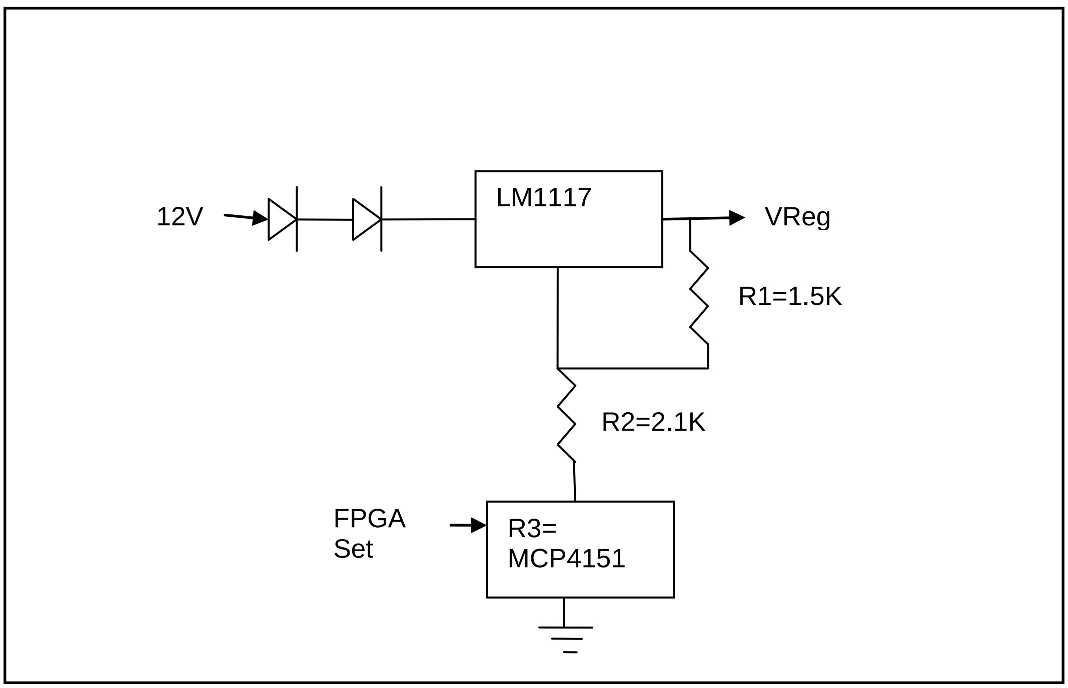


Figure 2: V1, V2, VLED Regulating Circuit

3.6 Gated and Protected V1, V2, Vled Outputs,

As shown in Figure 3, MosFET IRL6342PBF connects output of LM1117 (VReg) to J3 and J4 (V1,V2,Vled). This circuit allows turning on/off all 3 voltages simultaneously. Diode (D) protects the outputs by clamping the voltage at 6V for V1, V2 and 9.4V for Vled . Fuse prevents excessive load.

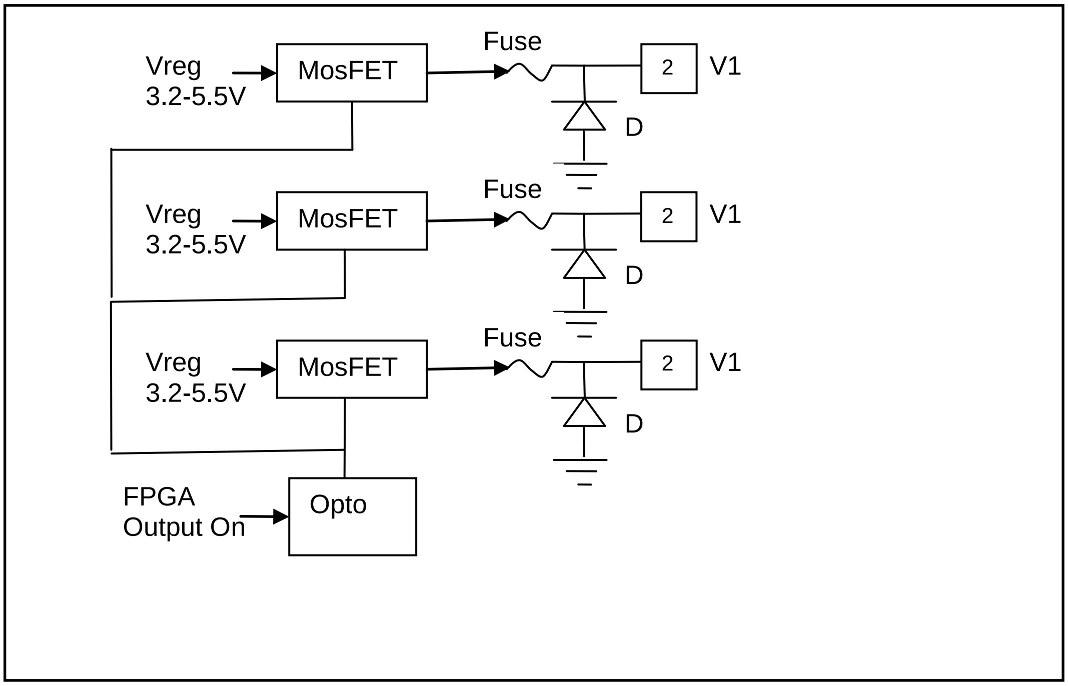


Figure 3: Gated and Protected V1,V2, Vled Outputs

3.7 V1, V2, Vled monitor

As shown in Figure 3, V1, V2, Vled are converted to digital values by AD7478 which is an 8 bit analog to digital converter with serial output. The output of AD7478 is connected to Artix FPGA.

- For V1, V2 ADC count is .02148 V/count (5.5V/256).
- For Vled ADC count is .03125 V/count (8.0V/256)
- ADC update
- The accuracy is 1%.

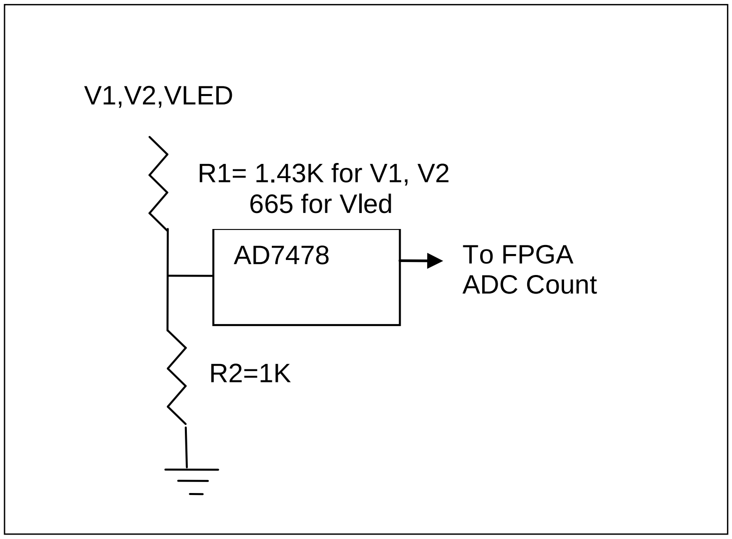


Figure 4: V1, V2, VLED Monitoring Circuit

3.7 Trig1, Trig2 Inputs and Outputs

Trig1 and Trig2 Inputs accept TTL and up to 50MHz. Trig1 and Trig2 outputs can be selected either from pulses generated inside the FPGA or from Trig1 and Trig2 Inputs respectively through FPGA. Pulses generates inside the FPGA are 40nS wide and the rate is programmable from 100Hz to 20KHz. Trig1 and Trig2 have individual pulse generator and they can be turned off individually.

4.0 Connectors Listing

- **Power Supply Requirements – Table 1**

Voltage	Current	Connector	Note:
12VDC	30 mA + Load on V1,V2, Vled	VME P6, J2	1-Amp fuse
+5VDC	1 A	VME P1, J2	2-Amp fuse

- **Indicators and Control – Table 2**

Front Panel Label	Description
LD1	Green: Heart Beat, Trig 1 Out Yellow: Trig 2 Out Red: PLL inside FPGA is locked (OK).
LD2	Green:Power Good, Yellow:Ethernet Link 100 connection, Red: Ethernet 1G
SW1	Reset FPGA
U53	VME Address switches [A23-A18]
U54	VME Address switches [A17-A12]

- **Input/Output Connections – Table 3**

Reference Designator	Description	Type	Front/Rear
J1	Ethernet Receptacle	RJ45	Front panel
P5	JTAG	Pin header	Front panel
J4	LED Pulse OUT -1	DB9	Front panel
J3	LED Pulse OUT - 2	DB9	Front panel
P2	Left: Trig1 in Right: Trig2 in	Dual Lemo female	Front panel
P1	Left: Trig1 out Right: Trig 2 out	Dual Lemo female	Front panel
P6	VME backplane	DIN 3 row [VME P1]	Rear
P7	VME backplane	DIN 3 row [VME P2]	Rear
J2	Stand Alone power	Phoenix connector	Rear

- **J3, J4 LED Pulse Out Pins function**

Pins	Description	Voltage, Current,
1,2,3,4,5	Ground	0
6	V LED	3.2-8V, 300 mA
7	V1	3.2-5.5V, 300 mA
8	V2	3.2-5.5V, 300 mA
9	Trigger Output	Hi 4.2V, Lo .55V, 32 mA, 40nS pulse width, 10Hz-20Khz

5.0 Operating Instructions

- **Prerequisites**
  - VME Crate
    - Set U53 (A23-A18) and U54 (A17-A12) to set VME base address for board
    - Plug in board. Use the injector latch to help sit the board.
    - Plug in J3, J4, P1, P2 cables.
    - Power up the crate. The top green LED should be lit to indicate voltages on boards are all OK.
    - After approximately 40 second, the bottom green LED should be blinking. The bottom Red LED should bit lit. These LED indicate the FPGA is running.

- Stand alone
  - Plug in power cable
  - Plug in Plug in J3, J4, P1, P2 cables.
  - Plug in Ethernet cable.
  - Turn on power.
    - The top green LED should be lit to indicate voltages on boards are all OK.
    - After couple second, the top red LED should be lit to indicate a link at 1G to the host computer.
  - After approximately 40 second, the bottom green LED should be blinking. The bottom Red LED should bit lit. These LED indicate the FPGA is running.

6.0 Programming

- Programmable feature description
  - When powers up, the board is default to stand-alone mode; all the configuration registers except Config 0 bit 15 are accessible through Ethernet. To access these registers through VME, VME host computer set Config 0 bit 15.
  - For VME, the address of the registers are base address determined by U53 and U54 plus VME Address Offset as shown in Table 4. All registers are 16 bits and only response to VME D16 A24 protocol.
  - All functions such as setting V1, V2, VLED are done through setting the appropriate Config registers.
  - All Config registers are write and read registers. All status registers are read only registers.
  - Ethernet Programming sections describes the Ethernet protocol and data format

- Table 4: VME Programming register map

  VME Address = Base Address + VME Address Offset

VME Address Offset	Register Name	Bits Functions	Descriptions
0	Config 0	0-8 :J4 V1 Volt 9: 0 Write to MCP4151 1 Read from 4151. Result is at Status 0 15: 0 Stand alone mode 1 VME mode	V1=1.25(1+(2.1K+R3)/1.5K)+60uA(2.1K+R3) R3= Bit0-8 * 19.53125 R3 is MCP4151 Only VME can write to Bit 15
2	Config 1	0-8 :J4 V2 Volt 9: 0 Write to MCP4151 1 Read from 4151. Result is at Status 1	V2=1.25(1+(2.1K+R3)/1.5K)+60uA(2.1K+R3) R3= Bit0-8 * 19.53125 R3 is MCP4151
4	Config 2	0-8 :J4 Vled Volt 9: 0 Write to MCP4151 1 Read from 4151. Result is at Status 2	V2=1.25(1+(2.1K+R3)/1.5K)+60uA(2.1K+R3) R3= Bit0-8 * 39.0625 R3 is MCP4151
6	Config 3	0-8 :J3 V1 Volt 9: 0 Write to MCP4151 1 Read from 4151.	V1=1.25(1+(2.1K+R3)/1.5K)+60uA(2.1K+R3) R3= Bit0-8 * 19.53125 R3 is MCP4151

		Result is at Status 3	
8	Config 4	0-8 :J3 Vled Volt 9: 0 Write to MCP4151 1 Read from 4151. Result is at Status 4	V2=1.25(1+(2.1K+R3)/1.5K)+60uA(2.1K+R3) R3= Bit0-8 * 39.0625 R3 is MCP4151
10	Config 5	0-8 :J3 V2 Volt 9: 0 Write to MCP4151 1 Read from 4151 Result is at Status 5	V1=1.25(1+(2.1K+R3)/1.5K)+60uA(2.1K+R3) R3= Bit0-8 * 19.53125 R3 is MCP4151
12	Config 6	0-15 : Trig1 Rate	Bit 15 to 0 of J4 Trig1 Timer
14	Config 7	13-11: Trig1 Rate 14: 1 Enable Trig1 Rate 15: 0 Select Trig1 Rate to J4 Trig1 out 1 Select P1 trig1 in to J4 Trig1 out.	Bits 13-11 are bits 18-16 of P2 Trig1 Timer Trig Rate = 1/(Timer * 20 ns)
16	Config 8	0-15 : Trig2 Rate	Bit 15 to 0 of J3 Trig2 Timer
18	Config 9	13-11: Trig2 Rate 14: 1 Enable Trig2 Rate 15: 0 Select Trig2 Rate to J3 Trig2 out 1 Select P1 trig2 in to J3 Trig2 out.	Bits 13-11 are bits 18-16 of P2 Trig1 Timer Trig Rate = 1/(Timer * 20 ns)
20	Config 10	0:1 Turn on J4 V1,V2,Vle 0 Turn off J4 V1,V2,Vle 1:1 Turn on J3 V1,V2,Vle 0 Turn off J3 V1,V2,Vle 2:0 Heart beat to bottom green LED 1 Trig1 Rate to bottom green LED	Connect Vreg to J4 V1, V2, Vled Connect Vreg to J3 V1, V2, Vled Selecteither to blink LED at 1 per second or at Trig 1 rate
	Config 11-20		Reserved for future
22	Status 0	0-8 J4 V1 MCP4151 14: MCP data is valid 15: MCP is ready for command	Data read back from MCP4151. After writing to MCP, data can be read back for verification
24	Status 1	0-8 J4 V2 MCP4151 14: MCP data is valid 15: MCP is ready for command	
26	Status 2	0-8 J4 VLED MCP4151 14: MCP data is valid 15: MCP is ready for command	
28	Status 3	0-8 J3 V1 MCP4151 14: MCP data is valid 15: MCP is ready for command	

30	Status 4	0-8 J3 Vled MCP4151 14: MCP data is valid 15: MCP is ready for command	
32	Status 5	0-8 J3 V2 MCP4151 14: MCP data is valid 15: MCP is ready for command	
34	Status 6	0-7: J4 V2 Adc count 15-8: J4 V1 Adc count	V1,V2= Adc count * (5.5/256)
36	Status 7	0-7: J3 V1 Adc count 15-8: J4 Vled Adc count	Vled= Adc count * (8/256)
38	Status 8	0-7: J3 V2 Adc count 15-8: J3 Vled Adc count	
40	Status 9	0-5: Firmware version	
42	Status 10	0-15: Trig 1 In Frequency in 10 of Hz.	Multiply this value by 10 to get Hz.
44	Status 11	0-15: Trig 2 In Frequency in 10 of Hz.	Multiply this value by 10 to get Hz.
46	Status 12	0: Ethernet Link 100 1: Ethernet Link 1000	
48,50	Status 13,14		

- **<u>Ethernet programming</u>**
  - FLP supports PING, ARP, and UDP Ethernet Protocols.
  - All Config Registers setting are sent as one Ethernet packets.
  - All Config and Status Registers are received as one packe
  - **<u>UDP Data Format</u>**
    - 5A5A (2 bytes)
    - Opcode (1 byte)
    - Type of data (1 or 2 bytes)
    - Data

Table 5: OpCode for UDP Data Format

OP-CODE	Function	Type Of Data
01	Set Registers, LCD from Host	0x0002, the bytes followed are to be displayed on LCD of FLP (must be 64 bytes). **0x0003, the bytes followed are Config registers data (see Table 4).**
02	Activate Command from host	03: Read Back Config and Status Registers (only one time) . **Wait 25 ms** before issue another Read Back Register Command
03	Data to Host	**03: Config and Status Registers (See Table 4)**

<u>UDP Data Format From Host Examples:</u>

Set Registers (See Table 4 for Registers' Definition) From Host

5A --- header
5A
01 -- Opcode to set Register, PLayBack, LCD
00 -- 0003 indicates data is for registers.
00
00 -- Register 0 Hi Byte
01 -- Register 0 Lo Byte
00 -- Register 1 Hi Byte
02 -- Register 1 Lo Byte
00 -- Register 2 Hi Byte
03 -- Register 2 Lo Byte
00 -- Register 3 Hi Byte
04 -- Register 3 Lo Byte
00 -- Register 4 Hi Byte
05 -- Register 4 Lo Byte
00 -- Register 5 Hi Byte
06 -- Register 5 Lo Byte
00 -- Register 6 Hi Byte
07 -- Register 6 Lo Byte
00 -- Register 7 Hi Byte
08 -- Register 7 Lo Byte
00 -- Register 8 Hi Byte
09 -- Register 8 Lo Byte
00 -- Register 9 Hi Byte
0A -- Register 9 Lo Byte
00 -- Register 10 Hi Byte
0B -- Register 10 Lo Byte
00 -- Register 11 Hi Byte
0C -- Register 11 Lo Byte
00 -- Register 12 Hi Byte
0D -- Register 12 Lo Byte
00 -- Register 13 Hi Byte
0E -- Register 13 Lo Byte
00 -- Register 14 Hi Byte
0F -- Register 14 Lo Byte
00 -- Register 15 Hi Byte
10 -- Register 15 Lo Byte
00 -- Register 16 Hi Byte
11 -- Register 16 Lo Byte
00 -- Register 17 Hi Byte
12 -- Register 17 Lo Byte
00 -- Register 18 Hi Byte
13 -- Register 18 Lo Byte
00 -- Register 19 Hi Byte
14 -- Register 19 Lo Byte
00 -- Register 20 Hi Byte
15 -- Register 20 Lo Byte

Set LCD Data 1St Line From Host

5A --- header

5A
01 -- Opcode to set Register,LCD
00 -- 0002 indicated data is for LCD data
02
02 -- LCD CMD
01 -- Return Home, 1st CHAR
03 -- LCD Char
01 -- LCD Char 1 ASCII
03 -- LCD Char
01 -- LCD Char 2 ASCII
03 -- LCD Char
01 -- LCD Char 3 Lo Byte
03 -- LCD Char
01 -- LCD Char 4 Lo Byte
03 -- LCD Char
01 -- LCD Char 5 Lo Byte
03 -- LCD Char
01 -- LCD Char 6 Lo Byte
03 -- LCD Char
01 -- LCD Char 7 Lo Byte
03 -- LCD Char
01 -- LCD Char 8 Lo Byte
03 -- LCD Char
01 -- LCD Char 9 Lo Byte
03 -- LCD Char
01 -- LCD Char 10 Lo Byte
03 -- LCD Char
01 -- LCD Char 11 Lo Byte
03 -- LCD Char
01 -- LCD Char 12 Lo Byte
00 -- LCD Char
03 -- LCD Char 13 Lo Byte
00 -- LCD Char
01 -- LCD Char 14 Lo Byte
03 -- LCD Char
01 -- LCD Char 15 Lo Byte
03 -- LCD Char
01 -- LCD Char 16 Lo Byte

Set LCD Data 2nd Line From Host

5A --- header
5A
01 -- Opcode to set Register, PLayBack, LCD
00 -- 0002 indicated data is for LCD data
02
02 -- LCD CMD
01 -- Go to 2nd line 1st CHAR
03 -- LCD Char
01 -- LCD Char 1 ASCII

03 -- LCD Char
01 -- LCD Char 2 ASCII
03 -- LCD Char
01 -- LCD Char 3 Lo Byte
03 -- LCD Char
01 -- LCD Char 4 Lo Byte
03 -- LCD Char
01 -- LCD Char 5 Lo Byte
03 -- LCD Char
01 -- LCD Char 6 Lo Byte
03 -- LCD Char
01 -- LCD Char 7 Lo Byte
03 -- LCD Char
01 -- LCD Char 8 Lo Byte
03 -- LCD Char
01 -- LCD Char 9 Lo Byte
03 -- LCD Char
01 -- LCD Char 10 Lo Byte
03 -- LCD Char
01 -- LCD Char 11 Lo Byte
03 -- LCD Char
01 -- LCD Char 12 Lo Byte
00 -- LCD Char
03 -- LCD Char 13 Lo Byte
00 -- LCD Char
01 -- LCD Char 14 Lo Byte
03 -- LCD Char
01 -- LCD Char 15 Lo Byte
03 -- LCD Char
01 -- LCD Char 16 Lo Byte

Registers and Status (See Table 4 for definition) From FLP

5A --- header
5A
03 -- Opcode
03 -- 03 indicates data is for registers.
00 -- Register 0 Hi Byte
01 -- Register 0 Lo Byte
00 -- Register 1 Hi Byte
02 -- Register 1 Lo Byte
00 -- Register 2 Hi Byte
03 -- Register 2 Lo Byte
00 -- Register 3 Hi Byte
04 -- Register 3 Lo Byte
00 -- Register 4 Hi Byte
05 -- Register 4 Lo Byte
00 -- Register 5 Hi Byte
06 -- Register 5 Lo Byte
00 -- Register 6 Hi Byte
07 -- Register 6 Lo Byte

00 -- Register 7 Hi Byte
08 -- Register 7 Lo Byte
00 -- Register 8 Hi Byte
09 -- Register 8 Lo Byte
00 -- Register 9 Hi Byte
0A -- Register 9 Lo Byte
00 -- Register 10 Hi Byte
0B -- Register 10 Lo Byte
00 -- Register 11 Hi Byte
0C -- Register 11 Lo Byte
00 -- Register 12 Hi Byte
0D -- Register 12 Lo Byte
00 -- Register 13 Hi Byte
0E -- Register 13 Lo Byte
00 -- Register 14 Hi Byte
0F -- Register 14 Lo Byte
00 -- Register 15 Hi Byte
10 -- Register 15 Lo Byte
00 -- Register 16 Hi Byte
11 -- Register 16 Lo Byte
00 -- Register 17 Hi Byte
12 -- Register 17 Lo Byte
00 -- Register 18 Hi Byte
13 -- Register 18 Lo Byte
00 -- Register 19 Hi Byte
14 -- Register 19 Lo Byte
00 -- Register 20 Hi Byte
15 -- Register 20 Lo Byte
01 -- Status 0 Hi Byte
01 -- Status 0 Lo Byte
01 -- Status 1 Hi Byte
01 -- Status 1 Lo Byte
01 -- Status 2 Hi Byte
01 -- Status 2 Lo Byte
01 -- Status 3 Hi Byte
01 -- Status 3 Lo Byte
01 -- Status 4 Hi Byte
01 -- Status 4 Lo Byte
01 -- Status 5 Hi Byte
01 -- Status 5 Lo Byte
01 -- Status 6 Hi Byte
01 -- Status 6 Lo Byte
01 -- Status 7 Hi Byte
01 -- Status 7 Lo Byte
01 -- Status 8 Hi Byte
01 -- Status 8 Lo Byte
01 -- Status 9 Hi Byte
01 -- Status 9 Lo Byte
01 -- Status 10 Hi Byte
01 -- Status 10 Lo Byte

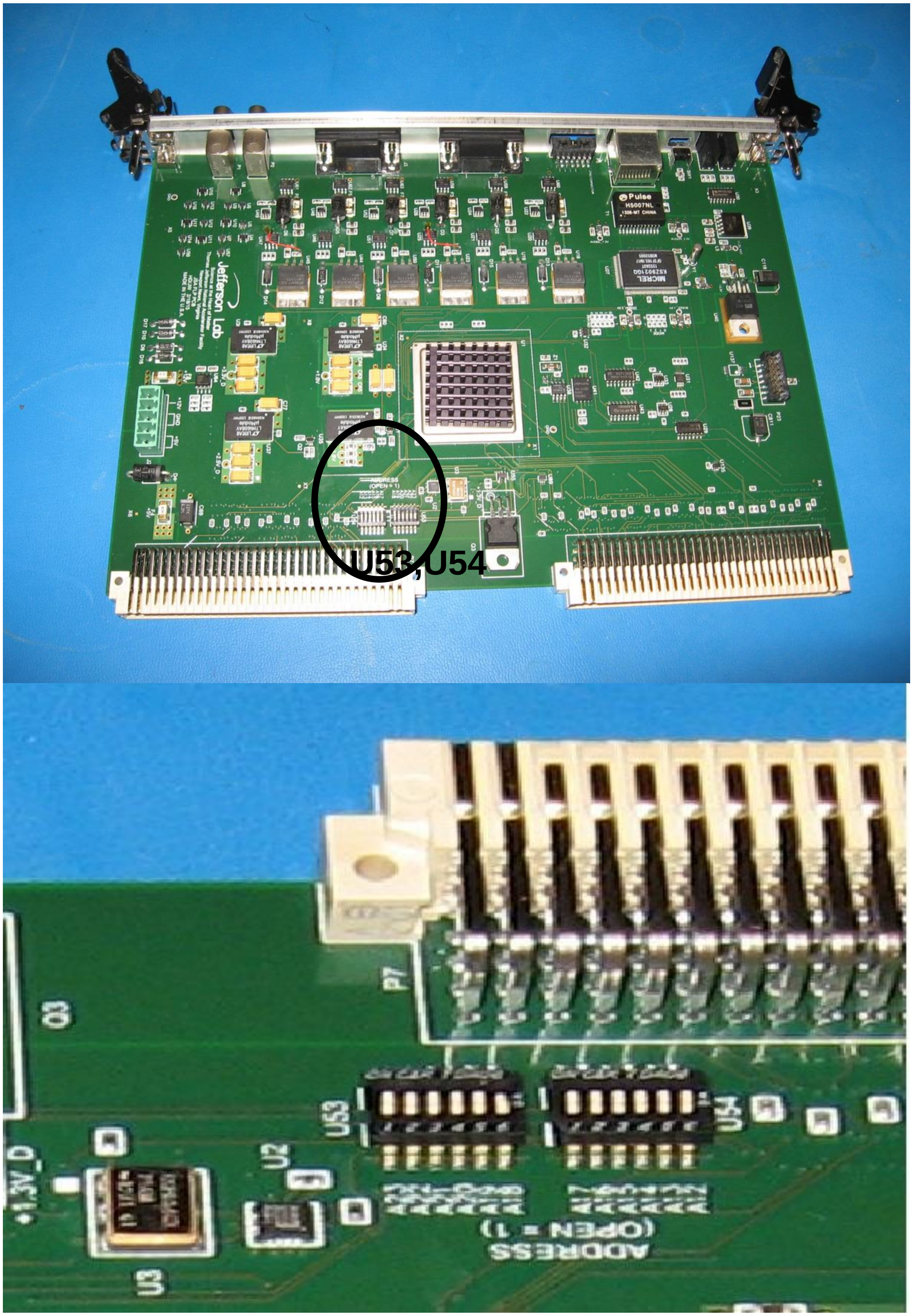
01 -- Status 11 Hi Byte
01 -- Status 11 Lo Byte
01 -- Status 12 Hi Byte
01 -- Status 12 Lo Byte
01 -- Status 13 Hi Byte
01 -- Status 13 Lo Byte
01 -- Status 14 Hi Byte
01 -- Status 14 Lo Byte

- Programming instruction examples
  - To set J4 V1 = 3.3V, J4 V2 = 5.5V, J4 Vled = 7.5V
    - R3 = (V1,2,Led – 3.126) / .00089333
      - V1 R3 = (3.3– 3.126) / .00089333 = 194.7=195
      - V2 R3 = (5.5– 3.126) / .00089333 = 2657.4=2657
      - Vled R3 = (7.5– 3.126) / .00089333 = 4896.3=4896
    - Set value for digital potentiometer for V1,V2 = R3/19.53125
      - SetValueV1 = 195/19.53125 = 5
      - SetValueV2 = 2657/19.53125 = 136
    - Set value for digital potentiometer for Vled = R3/39.0525
      - SetValueVled = 4896/39.0525=125
    - Write Config 0:
      - bit 0-8 = 5
      - bit 9 = 0
      - bit 15= 1
    - Write Config 1:
      - bit 0-8 = 136
      - bit 9 = 0
    - Write Config 2:
      - bit 0-8 = 125
      - bit 9 = 0
    - Wait 2 ms
    - Set bit 0 of Config 10
  - To read J3 Vled Volt
    - Read Status 8 bit 15 to 8 = AdcCount
    - Vled= AdcCount * (8/256)
  - To read J4 V2 Volt
    - Read Status 6 bit 16 to 8 = AdcCount
    - J4 V2 Volt = AdcCount * (5.5/256)

7.0 Demo GUI Program

A GUI Program demonstrates all the board's functions. This program running on Window OS provides all the functions of the board. A Weiner USB VME Controller is needed. To use this program:

- Installs MS Visual C++
- Installs Weiner USB VME driver
- Plug in Weiner USB VME Controller to VME crate
- Set U53, U54 on as shown in Figure 5
- Plug in Fast LED Pulser Board.
- Connect USB cable from PC to Weiner USB VME Controller
- Figure 6 shows the setup.
- Run FastLightPulser.exe
- GUI is shown in Figure 7.
- Type in values for all set boxes
- Click on Push to Set Button.



- Figure 5. U53,U54 Swiches Setting For FastLightPulser.exe Demo GUI Program. All switches except A10 are toward P7

- Figure 6. Weiner VME USB anh Fast Light Pulser Board Setup for FastLightPulser.exe Demo GUI Program

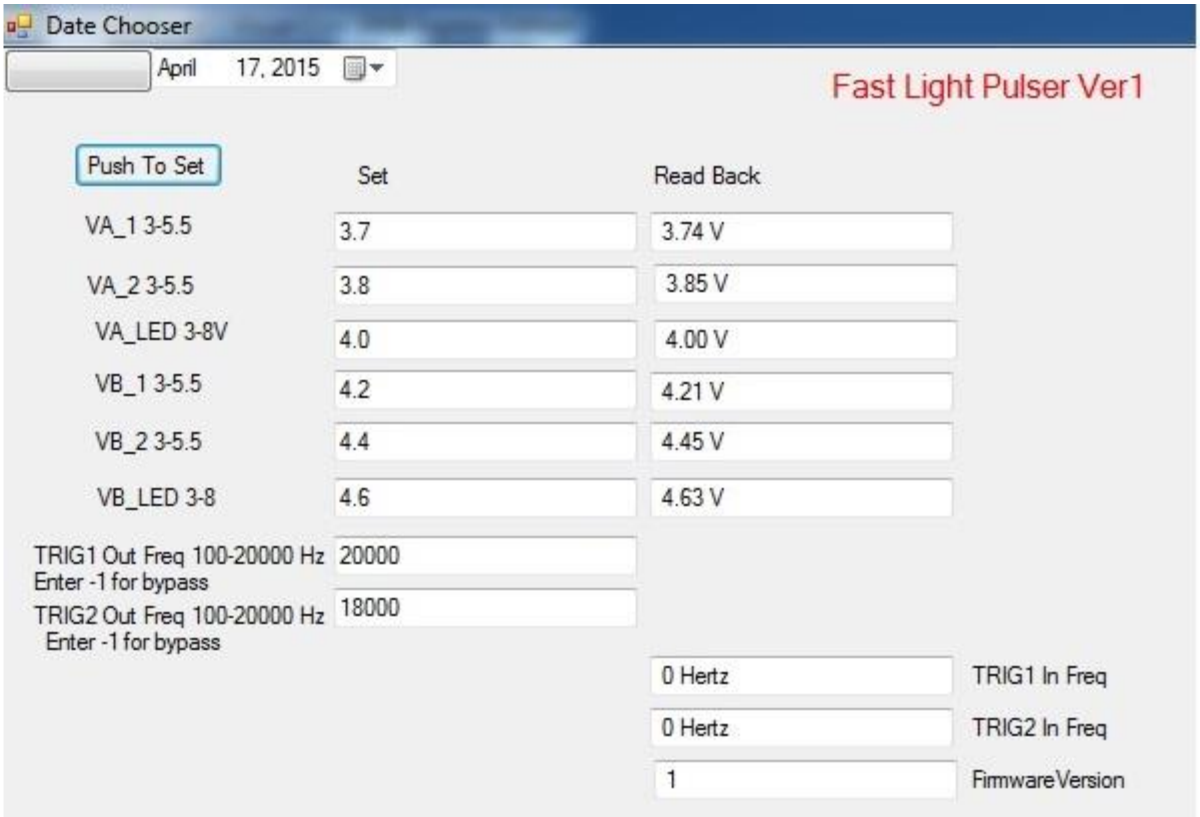


Figure 7. FastLightPulser.exe GUI