TI production test procedure

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1. Multimeter check:
* Check the resistance between the powers (+12 V, -12 V, +5 V, -5 V, three +3.3 V, two +1 V, +1.2 V, +2.5 V, +1.8 V) and ground. The resistances should be greater than 100 Ohm.
1. Hardware setup
* Put on the alignment pin (for TI with P0). Make sure that the alignment pin is tight on PCB;
* Put on the very top optic transceiver (HFBR-7924), three screws are used;
* Put on the heat sink for the FPGA;
* Put on the front panel;
* Set switch: SC01: to 11111100, S1: 00011111, S2: 11111111, SC1: 00000001 (default is 1)
1. Power up
* Plug the TI board into VXS crate payload slot #18. It is ok to be in any payload slot if no SD is present in the crate. All the power good LED near the power regulators should be OFF.
* Check the Voltage on the board (+12 V, -12 V, +5 V, -5 V, three +3.3 V, two +1.0 V, +1.2 V, +2.5 V, +1.8 V), the voltage should be within 3% of the nominal value;
* The front panel LED should be OFF, the Program Done LED (near the PROM) should be ON
1. FPGA firmware loading
* From ‘phecda’ X-terminal, telnet to the VME6100 controller. No username or password is required to login. After login:
* >ld < usrTempeDma\_AM.o; //user defined AM code 0x19 can be used
* >ld < trigger.o; // Gu’s test software package
* >EMload(TI’s VME slot number); // load the firmware to the TI. The board type is TI, and the serial number can be read from the sticker on the PCB. This information will be saved in the PROM on the PCB. The firmware loading takes about five minutes. After the above command, the Program Done LED should be off, the left LED on the front panel should be ON, the other three LED on front panel should be OFF.
* >FPGAusercode(slot); //FPGA user-code shows the firmware version, and firmware type
* >PROMusercode(slot); //PROM user-code shows the board type and serial number

>TItest4(TI’s slot) this is the combination of EMload, FPGAusercode and PROMusercode. Either “pass” or “fail” will be displayed at the end of the test.

1. FPGA/VME test, continue from step 4 X-terminal:
* >TImasterSet(slot, Block-level, crate-ID); //set the TI to internal loopback mode
* >TrgStart(slot); // VME trigger, The third LED should be flashing to indicate trigger
* >tidsBERead(slot); //Data readout, data file tidsBE.dat should be reasonable

> TItest5(TI’s slot) this is the combination of TImasterSet, TrgStart and tidsBERead. Either “pass” or “fail” will be displayed at the end of the test.

1. Copper front panel IO test: Continue from step #6, with TI X-terminal:
* >TImasterSet(slot, Block\_level, crate\_ID); //set the TI to internal loopback mode
* >TrgStart(slot); //Start trigger link
* Connect the “O#1” to “TS#1” (or the special 34-pin connector);
* >TrgTblLoad(slot); // load the event type look up table
* >\*(0x90a80020)=0x24; // enable the TS code input
* >\*(0x90a80028)=0x0; //disable the backpressure
* >\*(0x90a80048)=0x1; //enable TS code bit#1
* >\*(0x90a8004c)=0xff; \*(0x90a8004c)=0x00; //every pair should generate one trigger

Connect the custom connector specially made for TI test, to the 34-pin connector on TI;

> TItest6(TI’s slot) this is the combination of the above commands for copper front panel IO test. Either “pass” or “fail” will be displayed at the end of the test.

1. TI fiber input test, when the optional HFBR optic transceiver is loaded, not TS crate available:
* Connect a fiber between the TI optic transceivers (external loopback);
* >TImasterFLB(slot, block, crate-ID); // set the TI to Fiber loopback;
* >TrgStart(slot); // TI generates trigger and loopback to HFBR#1. This can test the trigger link and the SYNC link, but it can not test the clock link on the HFBR#1 input. This is a easier setup than step #7.
1. TI fiber input test, when there is a Trigger distribution crate ready:
* Connect a fiber between the TI optic transceiver and the TD (or TS, or TImaster);
* >TIsetup(slot); // set the TI as a slave board
* From the X-terminal that controls the TImaster or the TS: >TrgStart(slot); //VME trigger. This slot is the slot number of the TImaster or TS. The TI board trigger LED should be flashing.
* On TImaster/TS crate, do >\*(0x90a8008c)=0xffffffff (slot21 for example), the TI board should trigger, and after a while the trigger LED should stop. After the LED stop, do >\*(0x90a80100)=0x80 on the TI X-terminal window, the trigger LED should flash again, and stop after few triggers. This means that the busy backpressure is working

Connect the optic fiber between two TI boards;

> TItest7(TI\_A, TI\_B) this is to test the optic transceiver. Both TI boards are tested in TImaster mode and standard mode. Either “pass” or “fail” will be displayed at the end of the test.

1. P0 output, front panel 10-pin, 14-pin connector test: continue from step #7, with TI X-terminal:
* Connect the SD Trigger output, sync output, clock outputs to the scope
* Or connect the 10-pin (14-pin) connector outputs to the scope
* >TItest9(slot) //looping over pulse and reset
* The trigger should be seen on the scope;
* Two 250 MHz clocks should be seen on the scope;
* The sync reset should be seen on the scope.

If the test fails at any step, stop and record the failure in the test summary file. Some of the steps will be automated for less user interactions.

The purple procedure can be used for automatic test of steps 4 ( TItest4(slot) ), 5 ( TItest5(slot) ), 6 ( TItest6(slot) ), 7 and 8 ( TItest7(slotA, slotB) ).