

Nuclear Physics Division

*Data Acquisition Group*

# FANIO, TI to CAEN\_TDC interface board

J. William Gu ([jgu@jlab.org](mailto:jgu@jlab.org))

Nov. 5, 2018

# Table of Contents

# Section Title Page

|  |  |  |
| --- | --- | --- |
| 1 | Introduction | 3 |
| 2 | Purpose of FanioDC Module | 4 |
| 3 | Function Description | 4 |
| 4 | Specifications | 5 |
| 5 | FanioDC operation | 6 |
| 6 | Front connector and VME P2 user pin out | 6 |
| 7 | Citation | 7 |
| Appendix A | Schematics | 8 |
| Appendix B | Fabrication Drawing | 12 |
| Appendix C | Bill of Materials | 13 |

# 1 Introduction

The FANIO board is being designed for Hall-B (Collaboration, 2009) upgrade. This module is responsible for connecting the trigger/clock/reset/busy signals between the TI (GU, TID design, 2009) and the FANIO (GU, FANIO, 2010) boards. Some extra functions are added to the board in case that the TI and/or the FANIO boards are not available when testing the CAEN TDC (1290). Figure 1 shows the diagram of the FanioDC in the setup.

FanioLocation.tif

Figure 1 FanioDC board is located in the rear of VME64(x) crate

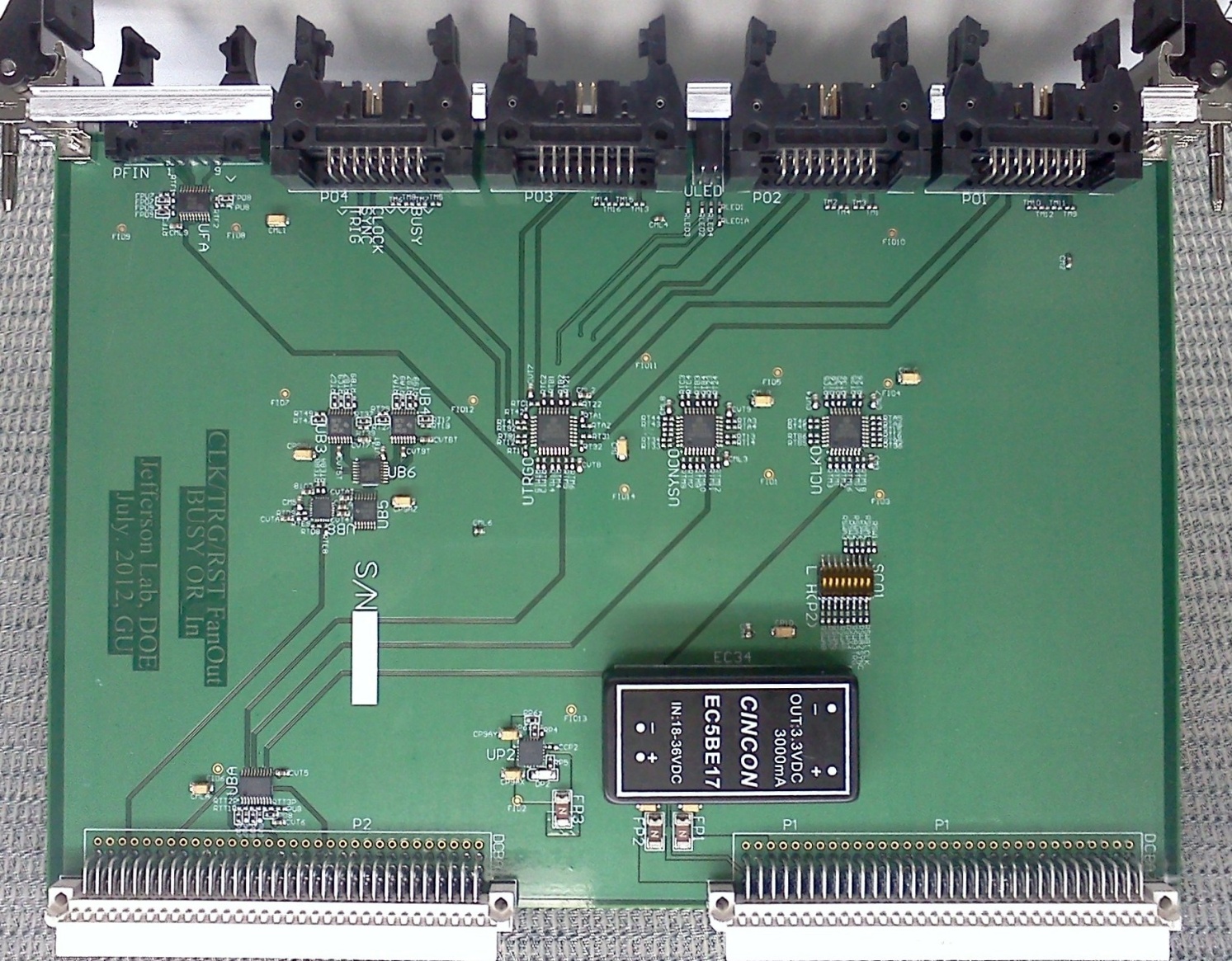


Figure 2 FANIODC board

# 2 Purpose of the module

The main purpose is to fan out the Trigger/Clock/Sync from Trigger Interface (TI) to CAEN TDC boards, and merge the BUSY signals from CAEN TDC boards to TI board.

Each FANIO board has four 3M 2x2x8 condo connectors, which can connect to eight CAEN TDC boards. The FANIO can connect to the TI front panel via a 10-pin twist-pair cable, or two FANIODC cards through the VME P2 connector. The front connection is easier, while the P2 connection is more versatile where the FANIODC has the option of built in signal generator.

# 3 Functional Descriptions

Figure 3 shows the block diagram of the FanioDC module.

FanioBlock.tif

Figure 3: FanioDC functional diagram

The FANIO gets its power from the P1 connector, which has +5V, +12V and -12V. It uses a TI TPS74401 to get the +3.3V, which supply power for the LVTTL BUSY “OR” logic. It uses CINCON EC5BE17 to get -3.3V, which is the main supply for ECL logic.

The inputs are received near the connectors. On semi MC100LVEP111, which is 2:1:10 clock buffer, is used to multiplex the inputs and to fan out.

The BUSY signals from CAEN TDC boards are translated into LVTTL first, then logically ORed together. The result is output to the connector in ECL level to match with TI board.

# 4. Specification Sheet

**4.1 Mechanical**

* Single width VME board. Size: 6Ux160mm (or 233mmX160mm).

**4.2 P2 inputs/outputs:**

* 41.67 MHz clock ECL 100 Ohm differential;
* Trigger, ECL 100 Ohm differential;
* Reset, ECL 100 Ohm differential;
* Status (busy), ECL 100 Ohm differential.

**4.3 Front panel inputs and outputs: (10 pin to TI, 16 pin to TDC)**

* 41.67 MHz clock ECL 100 Ohm differential;
* Trigger, ECL 100 Ohm differential;
* Reset, ECL 100 Ohm differential;
* Status (Busy), ECL 100 Ohm differential

**4.4 Power requirements:**

* +5v @ 0.5 Amps;
* +12V @ 0.3 Amps;
* -12V @ 0.3 Amps;

4.5 Environment:

* Forced air cooling;
* Commercial grade components ( 0-75 Celsius)

# 5 FANIO operation procedure:

The FANIO needs be properly set, and plugged into the proper crate and slot. Damage may happen to the FANIO, the crate, or other PCBs in the crate if the right procedure is not followed.

5.1 Power supply:

The board uses DC-DC converter to generate the -3.3V from +12V and -12V supply. It uses LDO to generate the +3.3V from +5V. This board can fit in standard VME64 crate, or VME64x crate, or VXS crate.

5.2 Hardware setting (jumper etc.):

5.2.1: Clock source selection (Switch Bit#1)

|  |  |  |
| --- | --- | --- |
| ON (low) | Front panel 10pin connector input | Switch position: RIGHT |
| OFF (high) | VME P2 connector input | Switch position: LEFT |

5.2.2: RESET source selection (Switch Bit#2)

|  |  |  |
| --- | --- | --- |
| ON (low) | Front panel 10pin connector input | Switch position: RIGHT |
| OFF (high) | VME P2 connector input | Switch position: LEFT |

5.2.3: TRIGGER source selection (Switch Bit#3)

|  |  |  |
| --- | --- | --- |
| ON (low) | Front panel 10pin connector input | Switch position: RIGHT |
| OFF (high) | VME P2 connector input | Switch position: LEFT |

6 pin out tables:

6.1 VME P2 User-defined pin table

|  |  |  |
| --- | --- | --- |
| Pin name | Signal Name | Signal Level |
| C13 | CLK+ | ECL |
| C14 | CLK- | ECL |
| C17 | TRIG1+ | ECL |
| C18 | TRIG1- | ECL |
| C25 | SYNC+ | ECL |
| C26 | SYNC- | ECL |
| C29 | BUSY+ | ECL |
| C30 | BUSY- | ECL |

6.2 Front panel 16-pin connector pin table

The definition is compatible with the CAEN TDC V1290.

|  |  |  |
| --- | --- | --- |
| Pin name | Signal Name | Signal Level |
| 1, 2 | Not used | N/A |
| 3, 4 | Trigger+, Trigger- | ECL, 100 ohm |
| 5, 6 | Reset+, Reset- | ECL, 100 ohm |
| 7, 8 | Clock+, Clock- | ECL, 100 Ohm |
| 9, 10 | Not Used | 100 ohm |
| 11,12 | Not used | 100 ohm |
| 13, 14 | Status+, Status- | ECL, 100 ohm |
| 15,16 | Not used | 100 ohm |

6.3 Front panel 10-pin connector pin table

The definition is compatible with the TI 10-pin connector.

|  |  |  |
| --- | --- | --- |
| Pin name | Signal Name | Signal Level |
| 1, 2 | BUSY+, BUSY- | ECL, 100 Ohm |
| 3, 4 | Trigger+, Trigger- | ECL, 100 ohm |
| 5, 6 | Reset+, Reset- | ECL, 100 ohm |
| 7, 8 | Not Used |  |
| 9, 10 | Clock+, Clock- | ECL, 100 ohm |

6.4 Front Panel LED indicator

#1 (left most): +5V from VME (normally ON)

#2 (mid-left): +3V on board (normally ON)

#3 (mid-right): -3V on board (normally ON)

#4 (right most): BUSY (normally OFF)

7. Citations:

# Works Cited

Collaboration, C. (2009). CLAS12 experiment. *Journal* , 1-25.

GU. (2010). *FANIO.* Retrieved from http://www.jlab.org/~gujh

GU. (2009). *TID design.*

##### Appendix A: design schematics

FanioP1.tif

FANIOP2.tif

FANIOP3.tif

FANIOP4.tif

##### Appendix B: PCB layout

FAIOTop.tif

##### Appendix C: Bill of Material

FanIO_BOM.tif