

Jefferson Science Associates, LLC

# Helicity Control Board User's Guide (Draft 2)

Programming and Hardware

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10

# Table of Contents

- Introduction ..... 3
- Why a New Helicity Board?..... 4
- Helicity Board Modes..... 4
  - Beam Sync Mode ..... 4
  - Free Clock Mode ..... 4
- Helicity Board Registers ..... 5
  - T\_Settle Register ..... 5
  - T\_Stable Register ..... 5
  - Helicity Pattern Register ..... 5
  - Reporting Delay Register ..... 5
- Software ..... 6
  - EPICS Channels..... 6
  - Programming ..... 8
  - Pseudo-random Helicity Generator ..... 9
- Hardware Description ..... 10
- Helicity Board Inputs and Outputs..... 11
  - LED Signals ..... 12
  - LEMO Signals..... 12
  - Fiber-Optic Inputs ..... 12
  - Fiber-Optic Outputs ..... 12
  - Relative Timing of Helicity Board Outputs..... 22
  - Helicity Flip and Pockels Cell High Voltage ..... 23
  - IA Control Signals ..... 24
- Fibers Distribution in Injector ..... 26
- Fibers Distribution to the Halls ..... 27
- How to Reduce 60 Hz Line Noise? ..... 28
- Helicity Board Tentative Configuration for PREx and Qweak..... 29
- Sign of Physics Asymmetry ..... 30
- Helicity Board Circuit Diagram and Description..... 30

## Introduction

A new Helicity Control Board was installed in November 2009. The new board provides more outputs and easier to re-program than the old one. The initial programming was chosen to meet the requirements of the current experiments. Changes are very easy to make and there is no limitation on the outputs. However, there are two main issues to keep in mind when selecting the outputs: first, the Pockels Cell response to the high voltage (HV) switching and, second, the Data Acquisition systems (DAQ) of the Halls. In specific, the choice of the T\_Settle has to be long enough to allow for the Pockels Cell to “settle” and the choice of the helicity reversal frequency has to be matched with the speed of the DAQ.

The Helicity Board is an “Advanced Programmable Logic Generator”. One of its outputs is used to control the high voltage (+3 kV or -3 kV) of the Pockels Cell on the Laser Table in CEBAF Injector. This change in Pockels Cell HV changes the circular polarization (left-handed or right-handed) of the laser light which in turn changes the direction of spin of the photo-emitted electrons relative to its momentum. The electron spin is either aligned parallel or anti parallel to the electron momentum; this is called electron helicity. Thus one signal from this logic generator changes the helicity of the electron beam and hence this board is called the Helicity Board.


The Helicity Board will operate at one of four timing selections. Three are fixed-frequencies of 30 Hz, 120 Hz, and 240 Hz triggered by "Beam Sync". The phase locking is forced during the last T\_Stable period. The T\_Settle time period may be chosen from the T\_Settle Register values. The T\_Stable selection is disabled in this mode.

The fourth mode of operation allows the module to operate in free-running mode, where the T\_Settle and T\_Stable values are selected from the values in the registers.

The Reporting Delay is selected from a register and determines how many windows there are between the real time Helicity Flip signal and the Delayed Helicity signal.

The Helicity Pattern may be selected to provide three pseudo-random patterns: Pair, Quartet, and Octal. In these patterns, the first window is chosen using the pseudo-random bit Shift Register. The forth pattern is pair Toggle.

When talking about frequency: it is the frequency of the T\_Settle signal ( $f$ ) and this will be labeled as the Helicity Board Frequency. Note that the Pair Sync signal will have  $f/2$  frequency. The Pattern Sync signal will have  $f/4$  when the Helicity Pattern is Quartet. The Delayed Helicity will have  $f/2, f/4, f/8$ .

There are three ways to indicate a helicity state: either 0,1 ( +, - ) or . Each helicity state is called a window.

## Why a New Helicity Board?

It was time to upgrade the Helicity Board for the following reasons:

- I. Clean up leftovers from G0. Drop the "MPS" label,
- II. Make it easy to program and easy to choose any reversal rate and any T\_Settle time,
- III. Change the Shift Register to 30-Bit. The old one is 24-Bit and would repeat in a shorter time (1 day compared to 50 days),
- IV. Add another pattern: Octet (+ - - + - + + - or - + + - + - - +),
- V. New fiber output signals:
  1. 2 additional outputs for 4-way IA feedback scheme where the applied IA voltage is determined not only from the current helicity state but also from the previous helicity state.
  2. Output of the Helicity Board 20 MHz Clock signal.

## Helicity Board Modes

There are two modes of the Helicity Board.

### Beam Sync Mode

There are three line synced fixed-frequencies of 30 Hz, 120 Hz, and 240 Hz triggered by "Beam Sync". The phase locking is forced during the last T\_Stable period. The T\_Settle time period may be chosen from the T\_Settle Register. You cannot choose T\_Stable in this mode only T\_Settle. Once you select Beam Sync Mode, the T\_Stable menu bar is disabled.

### Free Clock Mode

This mode of operation allows the module to operate in free-running mode, where the T\_Settle and T\_Stable values are selected from the tables below. In this mode, you can select any T\_Settle and any T\_Stable.

## Helicity Board Registers

These registers have the listed values. We can choose whatever we want to fill them.

### T\_Settle Register

There is a Five-bit R/W register that determines the "T\_Settle" portion of the helicity period. The settle time selections are as follows:

10  $\mu$ s, 20  $\mu$ s, 30  $\mu$ s, 40  $\mu$ s, 50  $\mu$ s, 60  $\mu$ s, 70  $\mu$ s, 80  $\mu$ s, 90  $\mu$ s, 100  $\mu$ s, 110  $\mu$ s, 120  $\mu$ s, 130  $\mu$ s, 140  $\mu$ s, 150  $\mu$ s, 160  $\mu$ s, 170  $\mu$ s, 180  $\mu$ s, 190  $\mu$ s, 200  $\mu$ s, 250  $\mu$ s, 300  $\mu$ s, 350  $\mu$ s, 400  $\mu$ s, 450  $\mu$ s, 500  $\mu$ s (DEFAULT), 550  $\mu$ s, 600  $\mu$ s, 700  $\mu$ s, 800  $\mu$ s, 900  $\mu$ s, 1000  $\mu$ s.

### T\_Stable Register

There is a Five-bit R/W register that determines the "T\_Stable" portion of the helicity period. The stable time selections are as follows:

400  $\mu$ s, 500  $\mu$ s, 600  $\mu$ s, 700  $\mu$ s, 800  $\mu$ s, 900  $\mu$ s, 1000  $\mu$ s, 1500  $\mu$ s, 2000  $\mu$ s, 2500  $\mu$ s, 3000  $\mu$ s, 3500  $\mu$ s, 4000  $\mu$ s, 4500  $\mu$ s, 5000  $\mu$ s, 5500  $\mu$ s, 6000  $\mu$ s, 6500  $\mu$ s, 7000  $\mu$ s, 7500  $\mu$ s, 8000  $\mu$ s, 8500  $\mu$ s, 9000  $\mu$ s, 10000  $\mu$ s, 33330  $\mu$ s (DEFAULT), 50000  $\mu$ s, 75000  $\mu$ s, 100000  $\mu$ s, 250000  $\mu$ s, 500000  $\mu$ s, 750000  $\mu$ s, 1000000  $\mu$ s.

### Helicity Pattern Register

There is a Two-bit R/W register that determines the Helicity Pattern. The pattern selections are as follow:

Pair (+ - or - +), Quartet (- + + - or + - - +) (DEFAULT),

Octet (+ - - + - + + - or - + + - + - - +), Toggle (+ - + - + - + - + -)

### Reporting Delay Register

There is a three-bit R/W register that determines the delay of the Delayed Helicity signal relative to the real time Helicity Flip signal. The delay time in units of helicity windows is selected as follows:

No Delay, 1 window, 2 windows, 4 windows, 8 windows (DEFAULT), 12 windows, 16 windows, 24 windows, 32 windows, 40 windows, 48 windows, 64 windows, 72 windows, 96 windows, 112 windows, 128 windows.

For example a Quartet has 4 helicity windows.

## Software

### EPICS Channels

These are the old channels:

**Table 1: EPICS Channels used with the old Helicity Board.**

Channel	Name	Value
G0 Helicity Settle Set	HELG0TSETTLEs	500 $\mu$ s
G0 Helicity Delay Set	HELG0DELAYs	8 windows
G0 Helicity Pattern Set	HELG0PATTERNs	Quartet
G0 Helicity Random/Toggle Set	HELG0ORDERs	Random
G0 Helicity Settle Read	HELG0TSETTLEd	500 $\mu$ s
G0 Helicity Delay Read	HELG0DELAYd	8 windows
G0 Helicity Pattern Read	HELG0PATTERNd	Quartet
G0 Helicity Random/Toggle Read	HELG0ORDERd	Random

These are the new channels:

**Table 2: EPICS Channels used with the new Helicity Board. These are the settings used during the PVDIS experiment.**

Channel	Name	Default Value
Helicity Clock Set	HELCLOCKs	Free Clock
Helicity Reporting Delay Set	HELDELAYS	8 windows
Helicity Pattern Set	HELPPATTERNs	Quartet
Helicity Clock Read	HELCLOCKd	Free Clock
Helicity T_Settle Read	HELTSETTLEd	500 $\mu$ s
Helicity T_Stable Read	HELTSTABLEd	33330 $\mu$ s
Helicity Reporting Delay Read	HELDELAYd	8 windows
Helicity Pattern Read	HELPPATTERNd	Quartet
Helicity Board Frequency	HELFREQ	(calculated frequency, not a readback) 29.5596 Hz

Below is the relation between the Numeric Value and Text for the Mode (**HELCLOCKd**). Type "caget -n" to get the numeric value instead of the string:

0 = 30 Hz Line Sync

1 = 120 Hz Line Sync

2 = 240 Hz Line Sync

3 = Free Clock

Below is the relation between the Numeric Value and Text for the Helicity Pattern (**HELPATTERNd**). Type "caget -n" to get the numeric value instead of the string:

0 = Pair

1 = Quartet

2 = Octet

3 = Toggle

Below is the relation between Numeric Value and Text for the Reporting Delay (**HELDELAYd**). Type "caget -n" to get the numeric value instead of the string:

0 = No delay

1 = 1 window

2 = 2 windows

3 = 4 windows

4 = 8 windows

5 = 12 windows

6 = 16 windows

7 = 24 windows

8 = 32 windows

9 = 40 windows

10 = 48 windows

11 = 64 windows

12 = 72 windows

13 = 96 windows

14 = 112 windows

15 = 128 windows

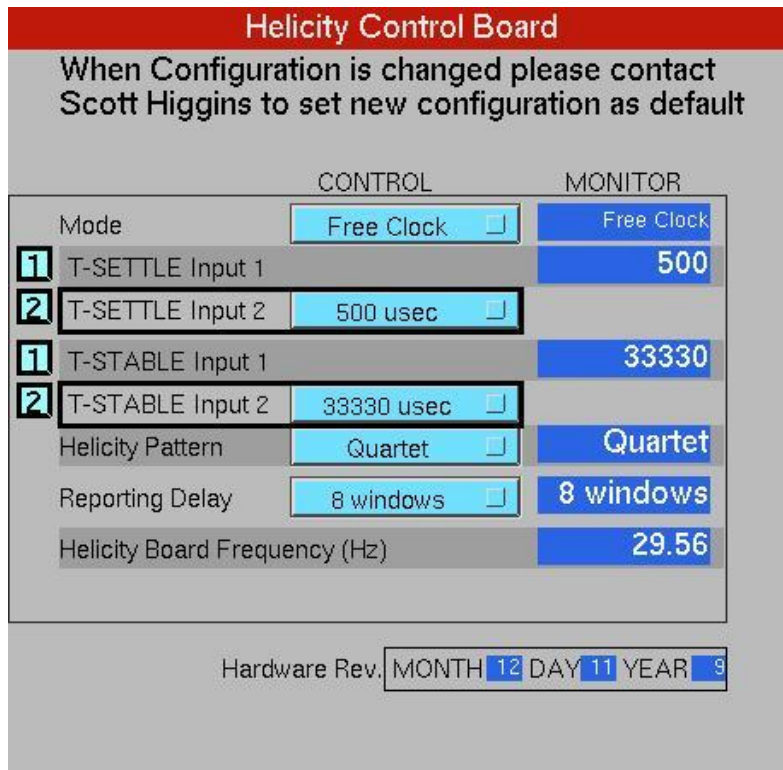


Figure 1: Helicity Board Control Screen. There are two pull-down menus for T\_Settle and two menus for T\_Stable. In Free Clock Mode, all menus are available. In Line Synced Mode, only the menus of T\_Settle are active; T\_Stable menus are inactive.

## Programming

Figure 1 shows the control screen for the new Helicity Board. The following shows how to use the board.

1. Select Mode:
  - I. Beam Sync (Force phase-lock during last T\_Stable):
    - Select Helicity Board Frequency  $f$ : 30 , 120, or 240 Hz Line Sync
    - Select T\_Settle value between 10  $\mu$ s - 1000  $\mu$ s
    - Display T\_Stable (T\_Stable selection is disabled):

$$T_{Stable} = \frac{1}{f} - T_{Settle}$$

- II. Free Clock:
  - Select T\_Settle value between 10  $\mu$ s – 1,000  $\mu$ s



- Select T\_Stable value between 400 μs – 1,000,000 μs
- Display Helicity Frequency (Reversal Rate):

$$f = \frac{1}{T_{Settle} + T_{Stable}}$$

2. Select Helicity Pattern:

Pair (+ – or – +), Quartet (– + + – or + – – +),

Octet (+ – – + – + + – or – + + – + – – +), Toggle (+ – + – + – + – + –).

3. Select Reporting Delay: n Windows, n = 0 ... 128 windows

## Pseudo-random Helicity Generator

30-Bit Shift Register is used to generate the pseudo-random bits: 0,1 (or +, –) which determines the first window of a pattern. This removes any correlation between the helicity of the beam and any other device in the accelerator or in the Hall. It is Pseudorandom, not “random” because it is deterministic, once a sequence of 30 bits is known, the next bits can be predicted, and it repeats after the maximal length. For any initial register value, there are  $2^{30} - 1 = 1,073,741,823$  (maximal length) random bits before the sequence repeats, 50 days for 1000 Hz helicity reversal rate and a Quartet pattern. Figure 2 shows the 30-Bit shift register.

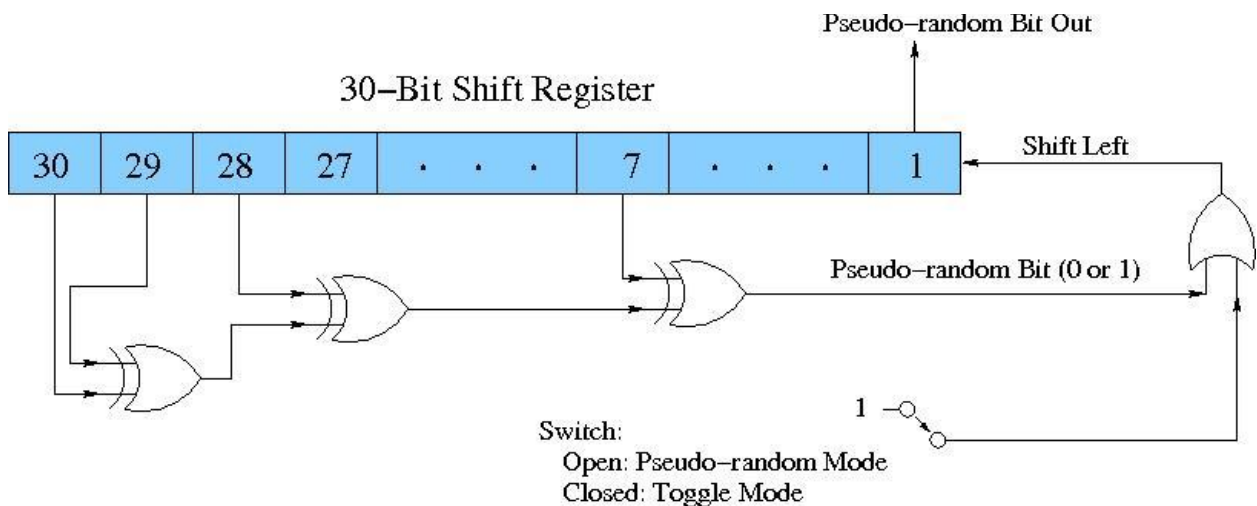


Figure 2: 30 Bit Shift Register.

The following C++ code can be used to fill the Shift Register or to predict the helicity bit:

```
UInt_t RanBit(UInt_t hRead)
{
    UInt_t bit7  = (fgShreg & 0x00000040) != 0;
    UInt_t bit28 = (fgShreg & 0x08000000) != 0;
    UInt_t bit29 = (fgShreg & 0x10000000) != 0;
    UInt_t bit30 = (fgShreg & 0x20000000) != 0;
    UInt_t newbit = (bit30 ^ bit29 ^ bit28 ^ bit7) & 0x1;
    fgShreg = ( hRead == 2 ? newbit : hRead) | (fgShreg << 1) & 0x3FFFFFFF;
    return newbit;
}
```

During analysis of the parity data, the first 30 patterns of each typically 1 hour long runs are used to initialize the Shift Register (these patterns are thrown away). After that the analysis can predict what the next pseudo-random bit will be. This prediction is compared to the actual helicity of the first window of each pattern in the data to make sure things are fine. Polarimeters and non-parity experiments usually do not perform this check.

## Hardware Description

The Helicity Control Board is located in an isolated crate in the Injector Service Building, see Figure 3. This rack is powered by an Isolation Transformer and is floating at 65 VAC. Follow instruction posted on the rack when working there.



Fiber Cable

Isolation Transformer

Power Cable with ground pin removed

Ground Rod

Figure 3: Rack that houses the Helicity Control Board. This crate is powered by an Isolation Transformer and is floating at 65 VAC. Please follow safety procedure when working in this rack. The ground pin of the Isolation Transformer power cable is removed.



Figure 4: Helicity Control Board and its Crate. This is IOC "iochelgen". (Remove the two un-used modules in this crate. Add a front panel to the Board).

## Helicity Board Inputs and Outputs

Figure 4 shows the new Helicity Control Board. The following describes the new board front panel.

## LED Signals

1. HEL REQ BIT/8 (Left): (?)
2. HEL REQ BIT (Right): (?)

## LEMO Signals

Upper left to lower right:

3. NC (Input): (?)
1. Hel REQ Bit (Output): (?)
2. Pattern Sync (Output): TTL signal
3. T\_Settle (Output): TTL signal

## Fiber-Optic Inputs

1. Beam Sync: This is the standard accelerator 30 Hz Beam sync signal it is generated from the 60 Hz line signal with (?). It is commonly used in the accelerator to ....

## Fiber-Optic Outputs

1. Patter Sync (old name QRT): Indicates the start of each pattern. If the pattern is Pair, then it is identical to Pair Sync, see Figure 6. This signal goes to the users.

This signal can also be called T\_Stable since when it is not true the Pockels Cell is table.

2. T\_Settle (old name MPS): Indicates the time the DAQs will not collect data allowing for the Pockels Cell to settle. This signal goes to the users.
3. Helicity Flip: This is the signal that goes to the Pockels Cell and IAs. The Pockels Cell changes its voltage with this signal thus changes the circular polarization of the laser light, see Figure . Its length is T\_Settle + T\_Stable. This is the real time helicity and goes only to the Laser Table in CEBAF Injector.

4. nHelicity Flip: Complementary to the Helicity Flip signal. This way the board always draws the same current regardless of the helicity being 0 or 1 and further protects against any electrical pickup from the Helicity Board. This signal goes to the crate that controls the Helicity Magnets. This is a floating crate located in the 5 MeV region in CEBAF Injector and powered by an isolation transformer with its cord ground wire cut-off.
5. Delayed Helicity: This signal is delayed by n windows, where n is chosen from Reporting Delay Register. It tells what the helicity was n windows before. This way no devices on the beamline or in the hall know what the current helicity is. In analysis, the data is shifted to match it with its helicity. This signal goes to the users, iocse9 and iocse14.

Note that the last n windows of data in each DAQ run are thrown away because the DAQ does not receive the actual helicity of these data (although it is known from helicity prediction).

6. Pair Sync: This signal toggle between 0 and 1, other wise it looks like the helicity signal. It is used to make T\_Stable (the integration window). It goes to the users.
7. IA0: This is an IA Control signal that indicates the current pattern. It goes to the Laser Table in CEBAF Injector.
8. IA1: This is an IA Control signal that indicates the previous pattern. It goes to the Laser Table in CEBAF Injector.
9. 20 MHz Clock: This is the internal Helicity Control Board clock. It goes to the Qweak ADCs in Injector and Hall C as external clock. It will be used as the reference clock for the ADCs. It will ensure that all the crates are sampling the same times.

The Halls only receive the following signals: T\_Settle, Pair Sync, Pattern Sync, and Delayed Helicity. Only the Parity DAQs make use of the four signals and data is analyzed according to the pattern generated by the Helicity Board. Other DAQs use some of them. For example:

- I. Accelerator FFB Measurement of Charge Asymmetry and Position Differences: This measurement uses the BPMs in Hall A Arc (iocse9) and the BPMs in Hall C Arc (iocse14). The only signal these iocs receive is the Delayed Helicity. The analysis software is coded to drop the first part of each helicity window that corresponds to T\_Settle (assumes T\_Settle is 500  $\mu$ s). Also a Reporting Delay of 8 windows is hard coded. The data is analyzed in pairs.
- II. 100 keV/500 keV and 5 MeV Injector Mott Polarimeter DAQ: Uses only T\_Settle and Delayed Helicity with Reporting Delay set to No Delay and the data are analyzed in pairs regardless of the Helicity Pattern.
- III. Hall A Spectrometer DAQ, Parity DAQ, Moller Polarimeter DAQ, and Compton Polarimeter DAQ: All use the four signals and analyze the data according to the pattern generated by the Helicity Board.
- IV. (?) Hall B CLAS DAQ and Moller Polarimeter DAQ: Only uses Delayed Helicity and T\_Settle. Data are analyzed in pairs.

- V. (?) Hall C Qweak Parity DAQ and Moller Polarimeter DAQ: Both use the four signals and analyze the data according to the pattern generated by the Helicity Board.

Figure 5 - Figure show the outputs of the helicity board using a scope.

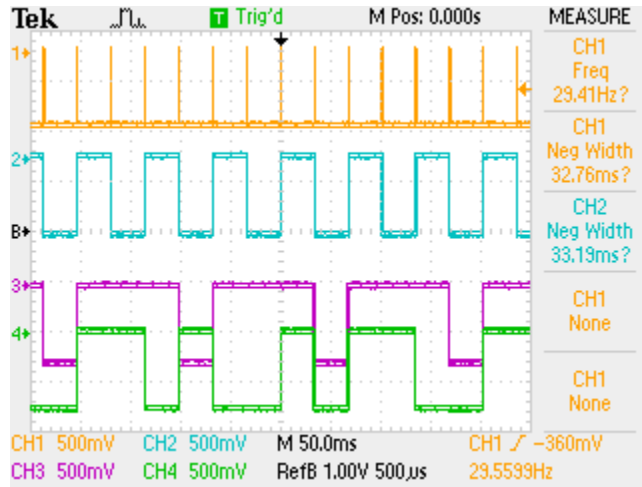


Figure 5: CH1: T\_Settle, CH2: Pair Sync, CH3: Pattern Sync, CH4: Delayed Helicity. This was the configuration for Hall A PVDIS experiment.

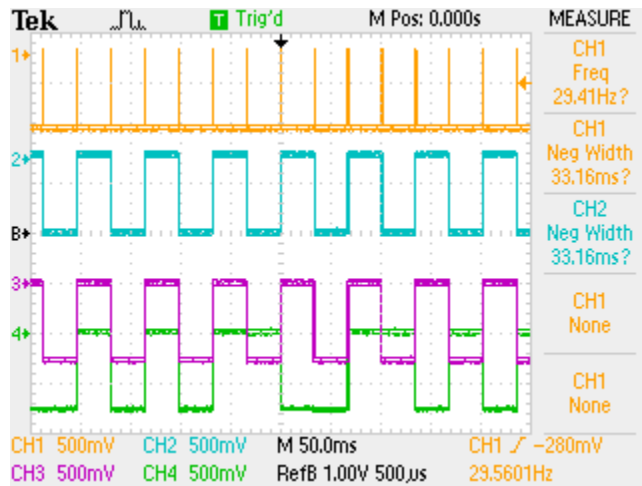


Figure 6: CH1: T\_Settle, CH2: Pair Sync, CH3: Pattern Sync, CH4: Delayed Helicity. Helicity Pattern is Pair.

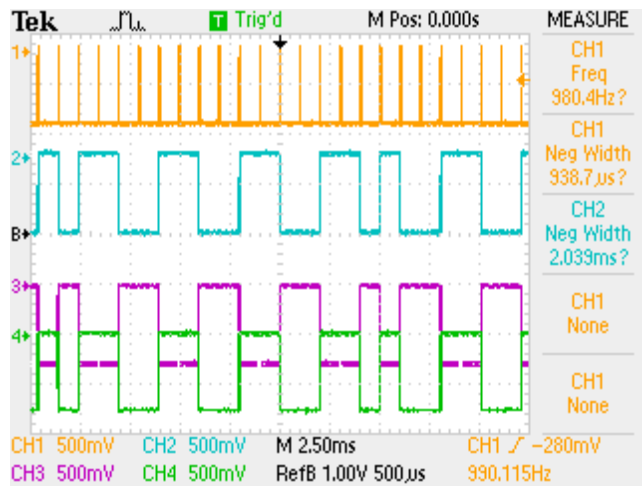


Figure 7: CH1: T\_Settle, CH2: Helicity Flip, CH3: nHelicity Flip, CH4: Delayed Helicity. No Delay.

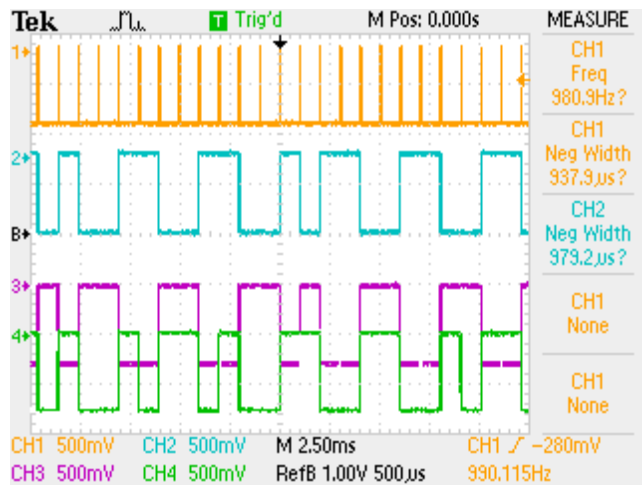


Figure 8: CH1: T\_Settle, CH2: Helicity Flip, CH3: nHelicity Flip, CH4: Delayed Helicity. The Delay is 8 windows.

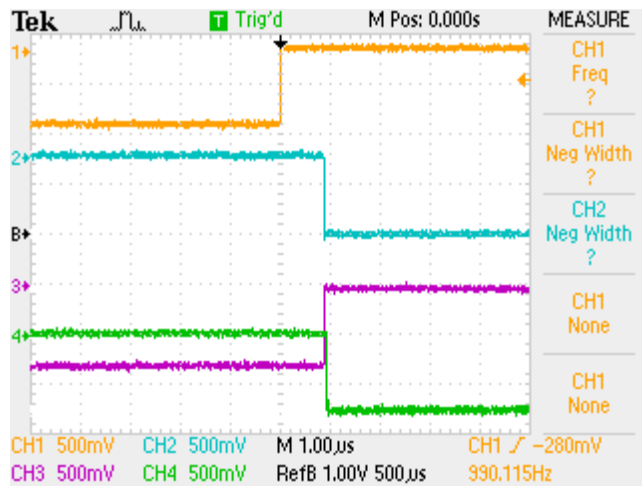


Figure 9: CH1: T\_Settle, CH2: Helicity Flip, CH3: nHelicity Flip, CH4: Delayed Helicity. The delay is 8 windows.

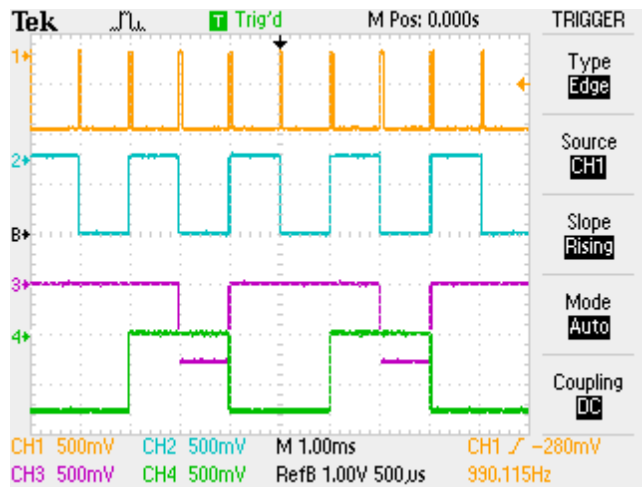


Figure 10: CH1: T\_Settle, CH2: Pair Sync, CH3: Pattern Sync, CH4: Delayed Helicity. T\_Settle = 60 µs, T\_Stable = 900 µs.



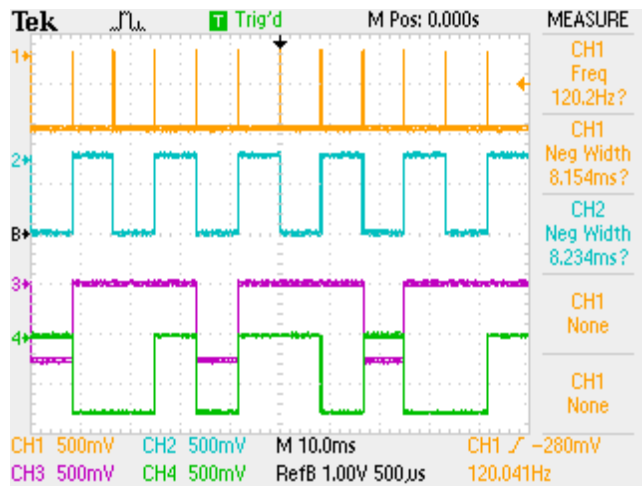


Figure 8: CH1: T\_Settle, CH2: Pair Sync, CH3: Pattern Sync, CH4: Delayed Helicity. Quartet Pattern, 120 Hz Line Sync Mode. T\_Settle + T\_Stable = 8.300 ms.

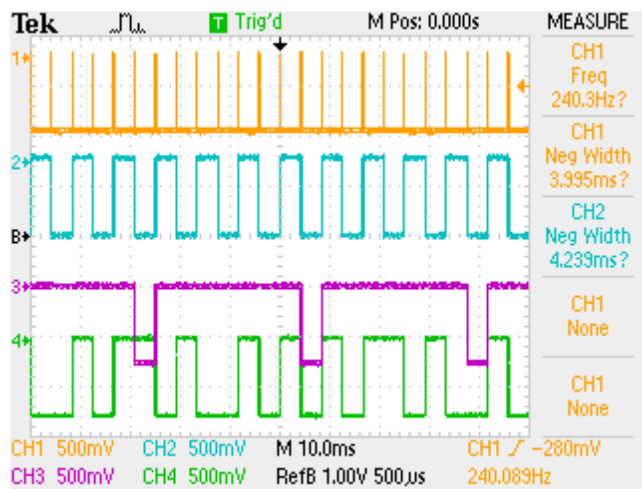


Figure 9: CH1: T\_Settle, CH2: Pair Sync, CH3: Pattern Sync, CH4: Delayed Helicity. Octet Pattern. 240 Hz Line Sync Mode. T\_Settle + T\_Stable = 4.150 ms.

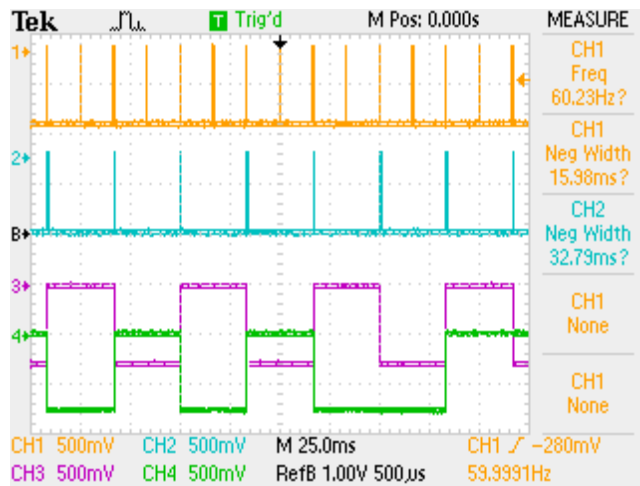


Figure 13: CH1: Beam Sync, CH2: T\_Settle, CH3: Pair Sync, CH4: Delayed Helicity. Pair Pattern, 30 Hz Line Sync Mode.

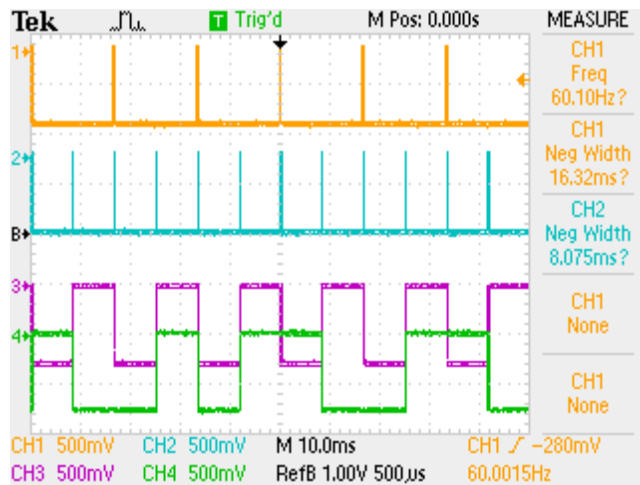


Figure 14: CH1: Beam Sync, CH2: T\_Settle, CH3: Pattern Sync, CH4: Delayed Helicity. Quartet Pattern, 120 Hz Line Sync Mode. T\_Settle + T\_Stable = 8.300 ms.

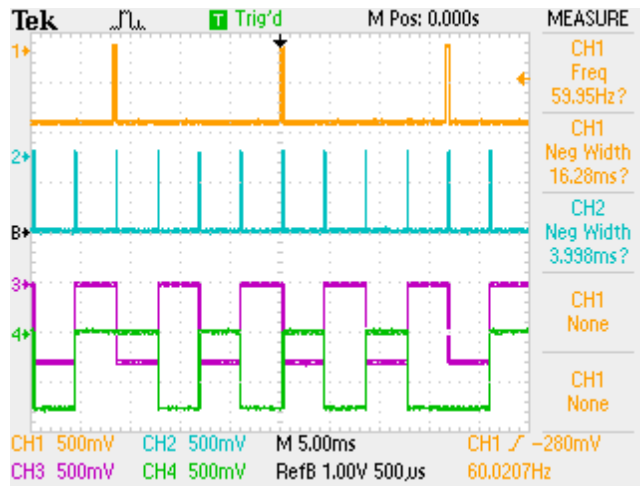


Figure 15: CH1: Beam Sync, CH2: T\_Settle, CH3: Pattern Sync, CH4: Delayed Helicity. Octet Pattern. 240 Hz Line Sync Mode. T\_Settle + T\_Stable = 4.150 ms.

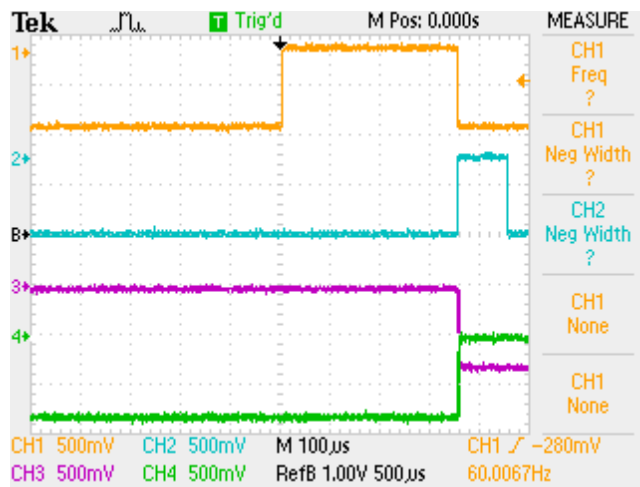


Figure 16: CH1: Beam Sync, CH2: T\_Settle, CH3: Pattern Sync, CH4: Delayed Helicity. Octet Pattern. 240 Hz Line Sync Mode. T\_Settle + T\_Stable = 4.150 ms.

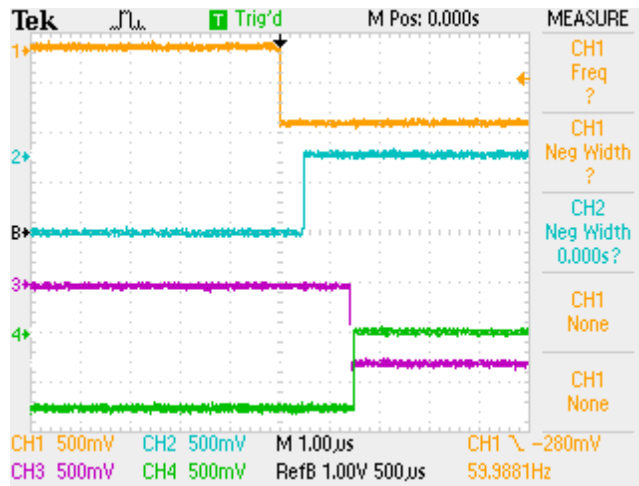


Figure 17: CH1: Beam Sync, CH2: T\_Settle, CH3: Pattern Sync, CH4: Delayed Helicity. Octet Pattern. 240 Hz Line Sync Mode.  $T_{Settle} + T_{Stable} = 4.150$  ms.

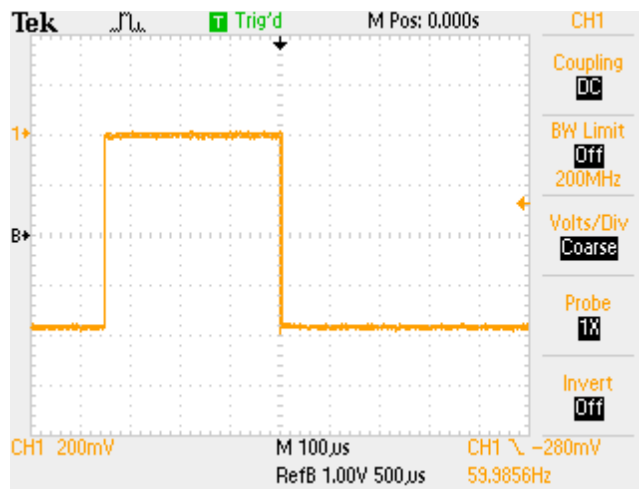


Figure 18: CH1: Beam Sync.

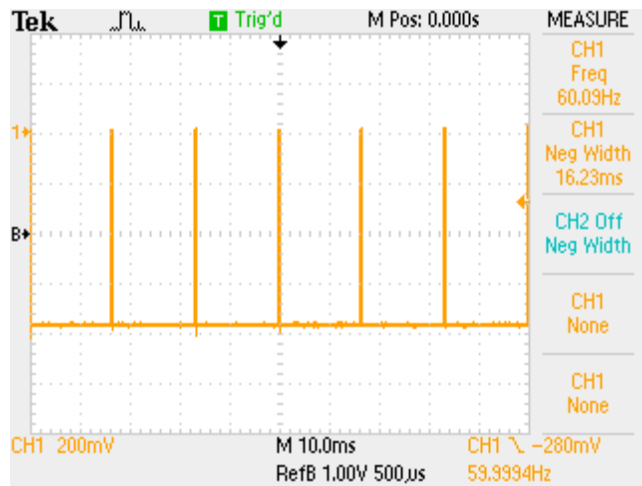


Figure 19: CH1: Beam Sync.



Figure 20: CH1: 20 MHz Clock.

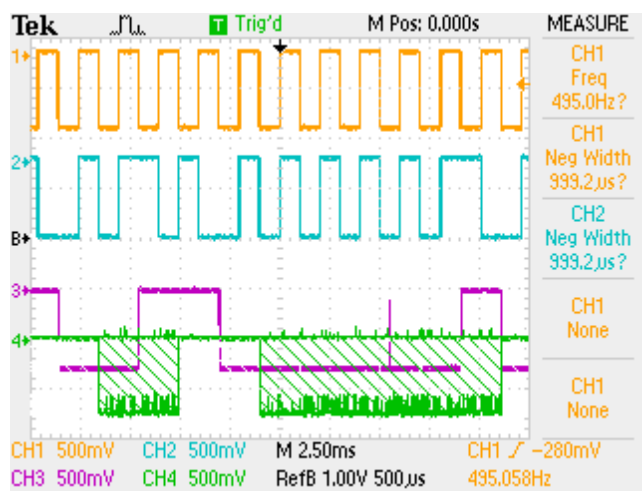


Figure 21: CH1: Pattern Sync, CH2: Helicity Flip, CH3: IA0, CH4: IA1. Pair Pattern.

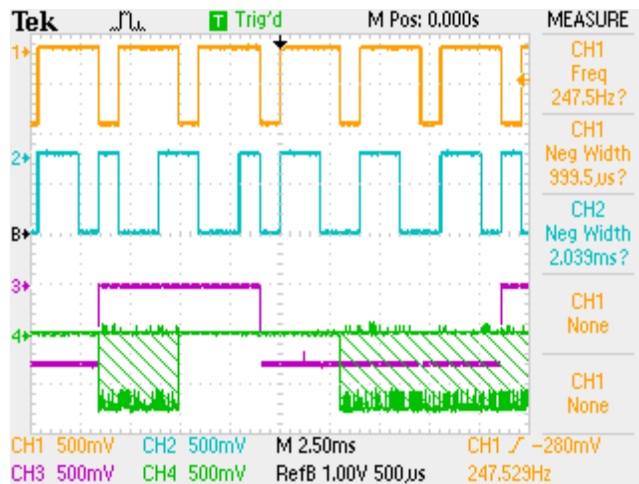


Figure 22: CH1: Pattern Sync, CH2: Helicity Flip, CH3: IA0, CH4: IA1. Quartet Pattern.

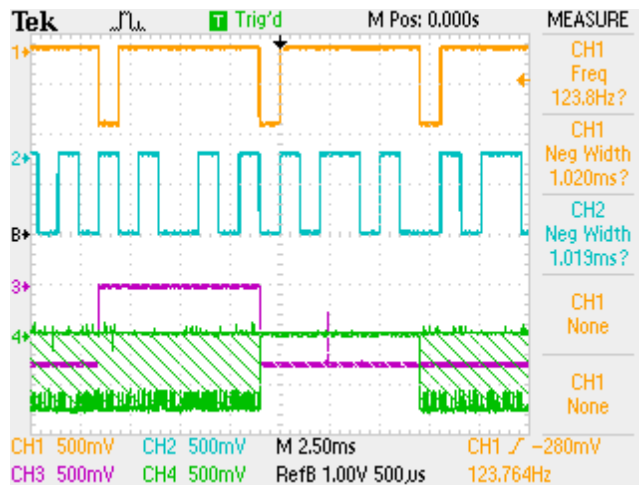


Figure 23: CH1: Pattern Sync, CH2: Helicity Flip, CH3: IA0, CH4: IA1. Octet Pattern.

## Relative Timing of Helicity Board Outputs

With the old helicity board, all the signals were in time. Looking at these signals in the injector or hall would show roughly 100 ns delays between them. This is mainly due to the Fiber FAN IN/OUT and to the Fiber Transducer and NIM FAN IN/OUT internal delays. For the new board, the transition to T\_Settle starts 1.0 μs before all other signals, see Figure and Figure . This is long enough to make sure the Halls know that the helicity is going to change beforehand. Actually this is not absolutely required because it takes the beam about 4.3 μs (?) per pass to reach the Hall.

If  $T_{Settle}$  is of order of  $10\text{ }\mu\text{s}$ , then we should account for the time the beam reaches the hall and for the time it takes for the helicity board signals to propagate to the Laser Table and to the Halls.

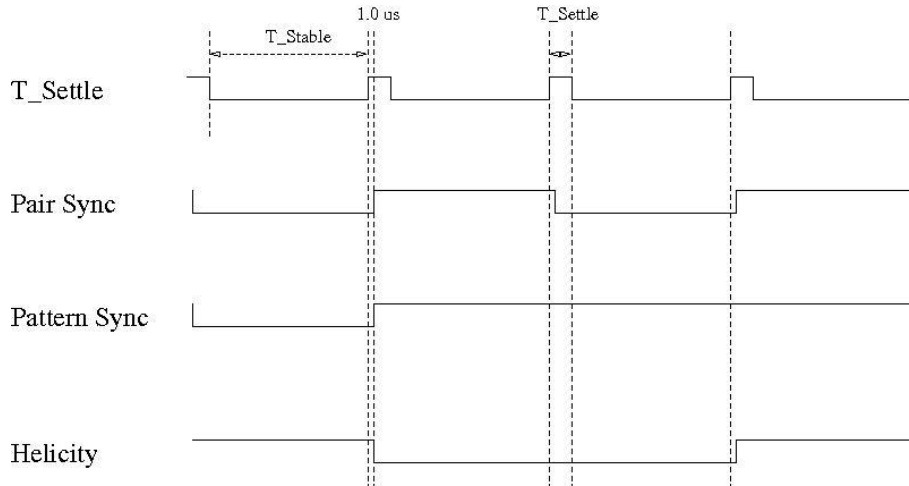


Figure 24: Helicity Board output signals timing relative to  $T_{Settle}$ . All the signals:  $Pair\ Sync$ ,  $Pattern\ Sync$ ,  $Helicity\ Flip$ ,  $nHelicity\ Flip$ ,  $Delayed\ Helicity$ ,  $IA0$ , and  $IA1$  start  $1.0\ \mu\text{s}$  after  $T_{Settle}$ .

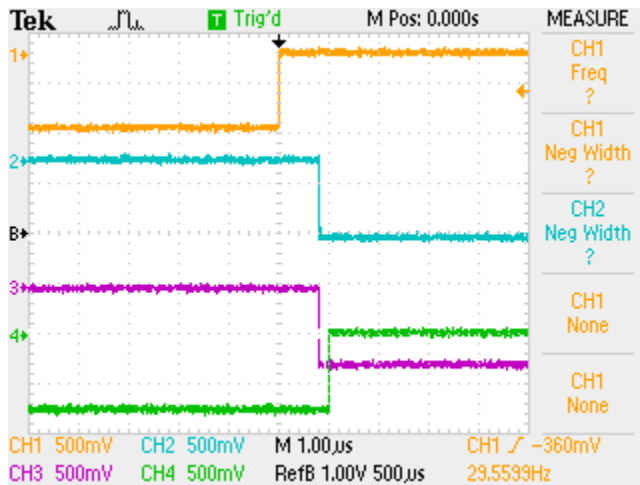


Figure 25: CH1:  $T_{Settle}$ , CH2:  $Pair\ Sync$ , CH3:  $Pattern\ Sync$ , CH4:  $Delayed\ Helicity$ .  $T_{Settle}$  starts  $1.0\ \mu\text{s}$  earlier than all other signals.

## Helicity Flip and Pockels Cell High Voltage

Figure shows the Pockels Cell (PC) high voltage (HV) while the helicity is flipping. The Pockels Cell HV changes between  $+3\ \text{kV}$  to  $-3\ \text{kV}$ .

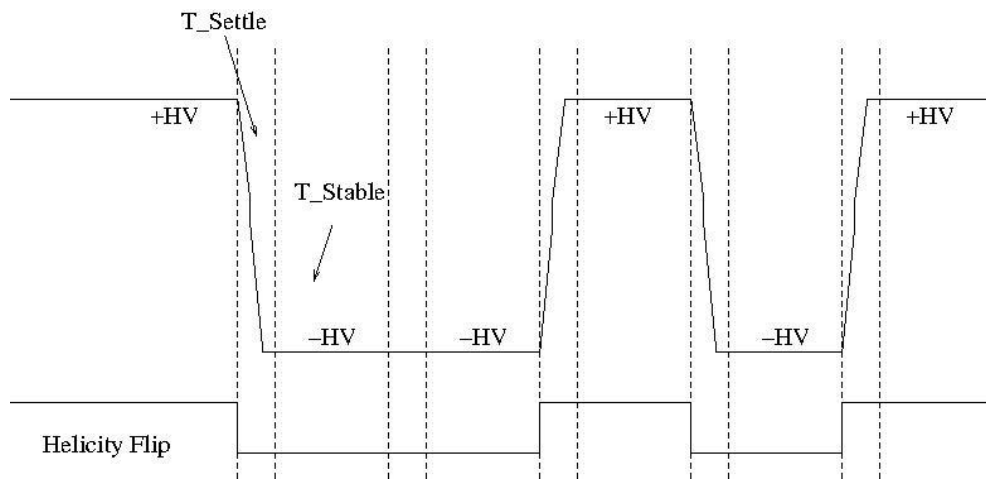


Figure 26: Pockels Cell HV showing the Helicity Flip.

## IA Control Signals

To be able to do charge feedback with Intensity Attenuator (IA) and cancel the electro-optical hysteresis of the Pockels Cell, the Helicity Board has two output signals identifying the current and the previous patterns. Figure shows the IA0 and IA1 signals when the Pair pattern is selected. Figure shows the same when the Quartet pattern is selected. Similarly for the Octet pattern.

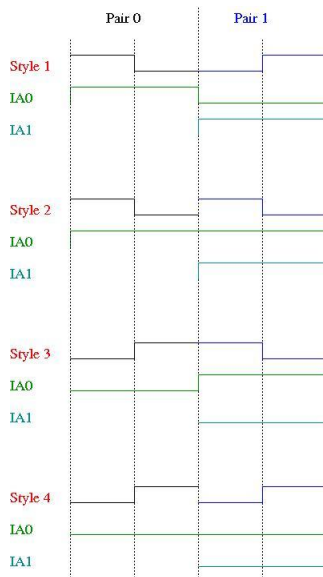


Figure 27: IA control signal IA0 and IA1 with the Pair pattern in relation to the Helicity Flip signal.



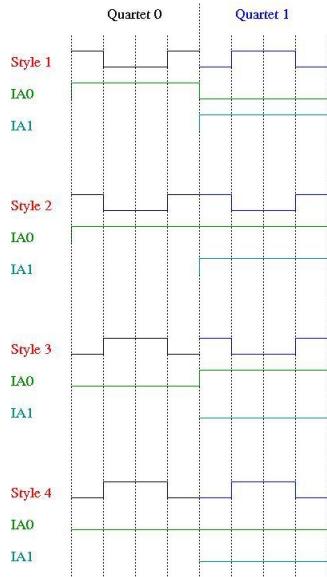


Figure 28: IA control signal IA0 and IA1 with the Quartet pattern in relation to the Helicity Flip signal.

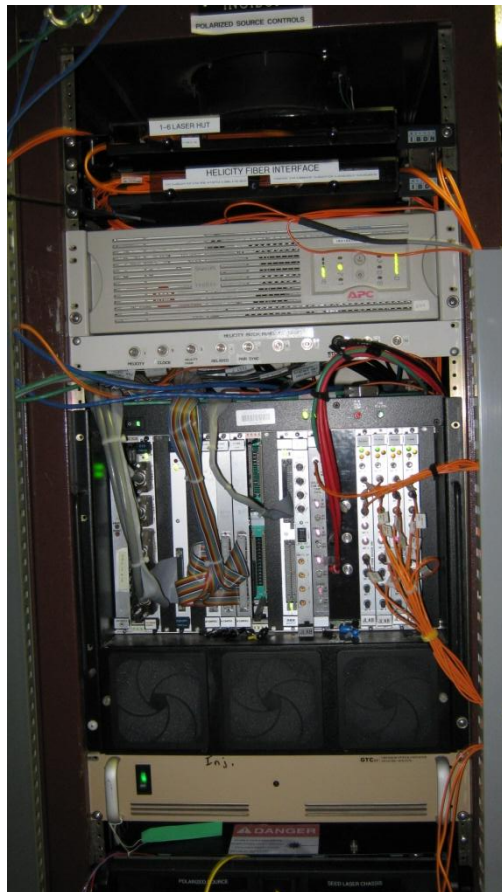


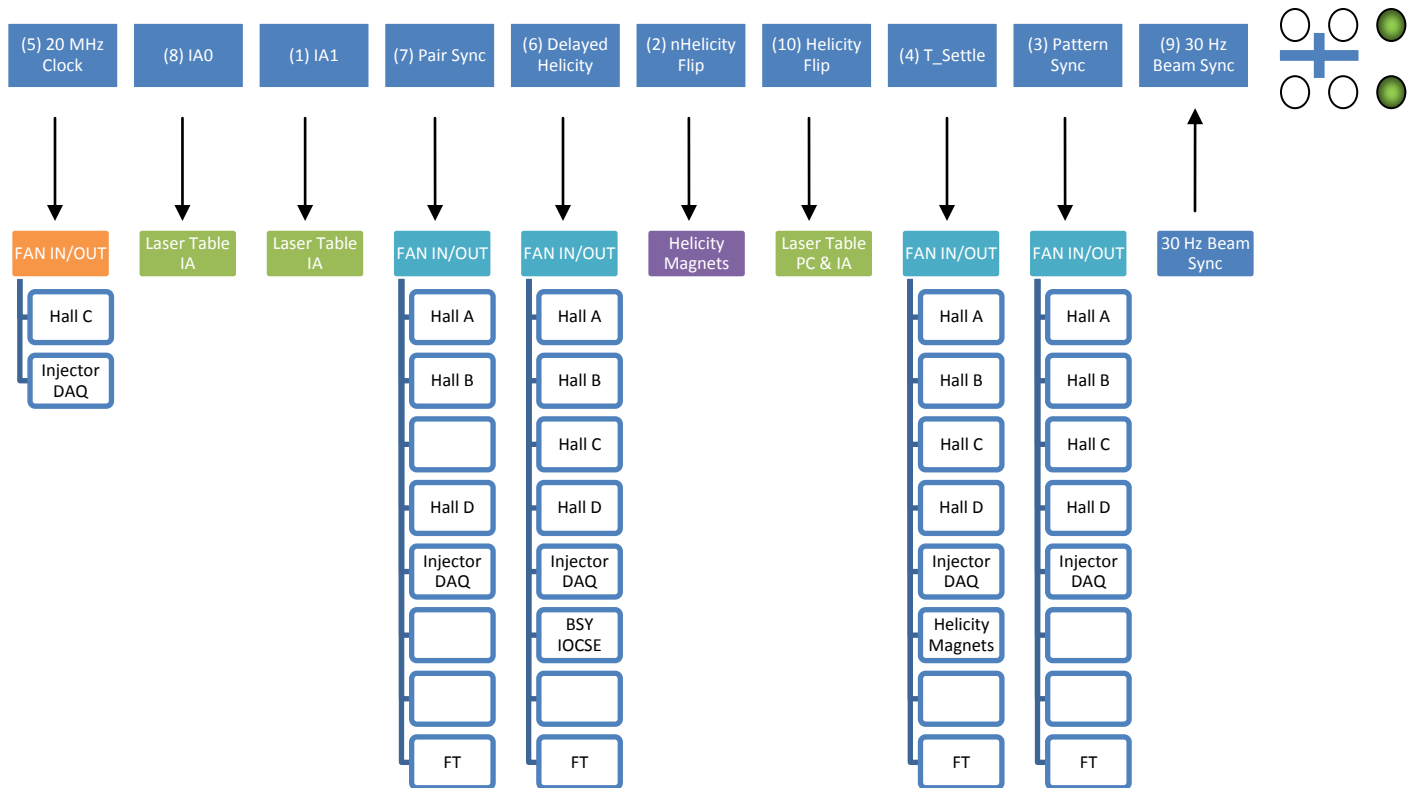
Figure 29: This is iocin6. The four FAN IN/OUT distribute Pair Sync, Delayed Helicity, T\_Settle, and Pattern Sync to the Halls and Injector DAQ. This crate is only used to provide power to the modules. There is also an FT card to be able to look at the signal on a scope.

## Fibers Distribution in Injector

We will need 2 new fibers from IN01B05 to the Laser Table: IA0 and IA1. Use the existing T120 fibers to carry the 20 MHz Clock signal from IN01B05 to the Injector Parity DAQ in IN02B24 and to the Parity DAQ in Hall C. The old name of T\_Settle is "MPS". The old name of Pattern Sync is "QRT".

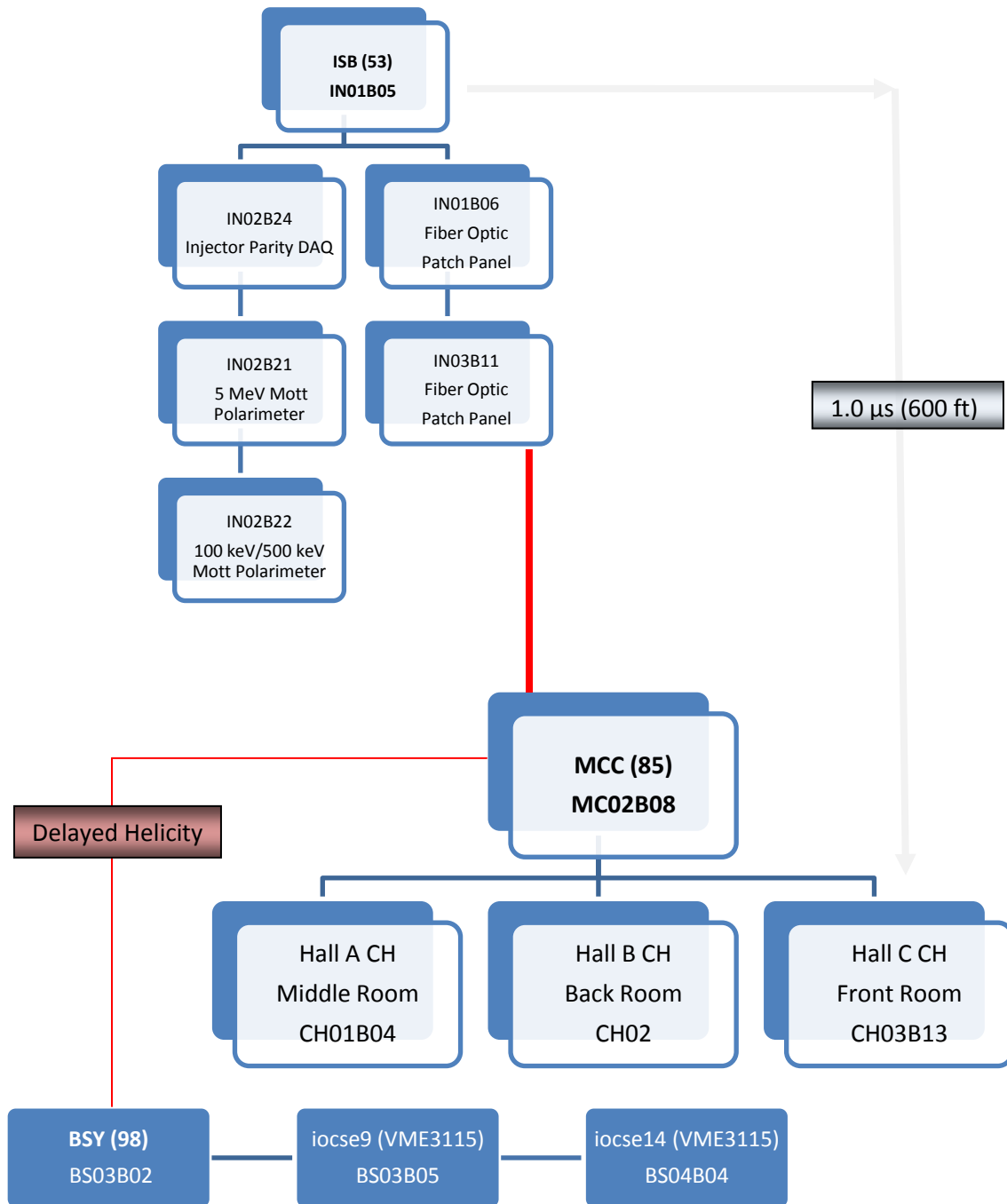
We will need four Fiber Fan IN/OUT modules to be placed in iocin6 crate. We will need special 1 Fiber Fan IN/OUT for the 20 MHz Clock signal. Also we will need a Fiber Transducer (FT) to change the signals from fiber to voltage in this crate.

These FAN IN/OUT modules will be located in the crate iocin6 shown in Figure . Fiber 11 is iochelgen TX and Fiber 12 is iochelgen RX.



## Fibers Distribution to the Halls

The following diagram shows the fiber distribution from the Injector to the Halls. (Hall B gets all 4 signals (?), Hall C: T120 instead of Pair Sync (?))



## How to Reduce 60 Hz Line Noise?

There are three ways to reduce 60 Hz line noise.

1. Select  $T\_Stable$  such that:  $f > 1$  kHz (Free Clock Mode). This way the contribution of the 60 Hz line noise does not change by much from one window to the next and thus cancels when calculating the asymmetries ( $A$ ). Even a better cancellation is achieved when using Quartet or Octet patterns. The data will still have full information about the 60 Hz line noise.
2. Integrate over 60 Hz noise per helicity window (Free Clock Mode): Select  $T\_Stable = 33,330 \mu s$  (exactly two 60 Hz cycles). This is an exact cancellation and the data collected will have no information about 60 Hz line noise.
3. Cancel 60 Hz line noise using patterns (it does not cancel per window; however it cancels when the differences are calculated). Use the Beam Sync Mode:
  - Select 30 Hz Line Sync: Select a  $T\_Settle$ , then  $T\_Stable = 33,333 \mu s - T\_Settle$   
Select Pair Pattern. Then,  $A = \frac{+1-2}{+1+2}$
  - Select 120 Hz Line Sync: Select a  $T\_Settle$ , then  $T\_Stable = 8,333 \mu s - T\_Settle$   
Select Quartet Pattern. Then,  
$$A = \frac{+1-2-3+4}{+1+2+3+4}$$
  - Select 240 Hz Line Sync: Select a  $T\_Settle$ , then  $T\_Stable = 4,167 \mu s - T\_Settle$   
Select Octet Pattern. Then,  
$$A = \frac{+1-2-3+4-5+6+7-8}{+1+2+3+4+5+6+7+8}$$

What about other noises? Choice (1) will work as well for other low frequency noises including the noise from target density fluctuation which is peaked at low frequency because it is a mechanical noise due to gas bubbles in the Hall cryogenic liquid target. Choices (2) and (3) are geared for 60 Hz noise; other noises will remain in the data. These noises will increase the width of the helicity correlated distributions like the target density fluctuations. While prominent single low frequency noise will cause double horned distributions.

## Helicity Board Tentative Configuration for PReX and QWeak

The tentative Helicity Board configuration for PReX is shown in Figure 30 and for QWeak is shown in Figure 10. Table 3 shows the Helicity Board configuration.

Helicity Control Board		
When Configuration is changed please contact Scott Higgins to set new configuration as default		
	CONTROL	MONITOR
Mode	240 Hz Line Sync	240 Hz Line Sync
1 T-SETTLE Input 1	100 usec	100
2 T-SETTLE Input 2		4066
Helicity Pattern	Octet	Octet
Reporting Delay	16 windows	16 windows
Helicity Board Frequency (Hz)		240.00
Hardware Rev. MONTH 12 DAY 11 YEAR 9		
User Guide 1		

Figure 30: Helicity Board Control Screen with PReX settings

Helicity Control Board		
When Configuration is changed please contact Scott Higgins to set new configuration as default		
	CONTROL	MONITOR
Mode	Free Clock	Free Clock
1 T-SETTLE Input 1	60 usec	60
2 T-SETTLE Input 2		
1 T-STABLE Input 1	900 usec	900
2 T-STABLE Input 2		
Helicity Pattern	Quartet	Quartet
Reporting Delay	8 windows	8 windows
Helicity Board Frequency (Hz)		1041.67
Hardware Rev. MONTH 12 DAY 11 YEAR 9		
User Guide 1		

Figure 31: Helicity Board Control Screen with QWeak settings.

Table 3: Helicity Board tentative configuration for PREx and QWeak.

	PREx	QWeak
Mode	240 Hz Line Sync	Free Clock
T_Settle	100 $\mu$ s	60 $\mu$ s
T_Stable	4,107 $\mu$ s	900 $\mu$ s
Helicity Pattern	Octet	Quartet
Reporting Delay	16 windows	8 windows
Helicity Board Frequency	240 Hz	1 kHz

## Sign of Physics Asymmetry

One may wonder how could we tell the actual helicity of the electrons when they interact with the target in the Hall. Parity Experiments measure very small asymmetries that can easily be positive or negative. There is standard theoretical prediction of the magnitude and sign of the physics asymmetry. However, the new physics that the experiment is trying to measure may be big enough to change the sign of the asymmetry.

This is easy: no need to keep track of all these conventions about helicity and how it is treated at each junction. This is simply done using the Moller Polarimeter in the Hall. The sign of the asymmetry measured in the Hall is decided using the Moller Polarimeter. Moller asymmetry is well understood in theory and the sign of the measured polarization is well known. To check the relative sign between the Moller Polarimeter DAQ and the Parity DAQ, a large charge asymmetry is introduced in the injector by changing the Pockels Cell HV (PITA) and both DAQs measure this charge asymmetry at the same time to find out the relative sign.

## Helicity Board Circuit Diagram and Description