Streaming Readout (SRO) at JLAB

(and defining concepts for EIC)

JLEIC Weekly Meeting – July 24, 2020

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Data Acquisition Support at JLAB

- Historically the DAQ group (in Physics Division) has existed at Jefferson Lab from the very beginning
  - The CODA toolkit has evolved and expanded through 3 generations so far.
  - All 4 Experimental Halls are using some version of CODA for data acquisition.

- The Fast Electronics Group (Physics) has also grown significantly
  - Experiments are becoming much more reliant on custom electronics to interface detectors and digitize signals.
  - FPGAs (Field Programmable Gate Arrays) and ASICs (Application Specific Integrated Circuit) are the Now and the Future of the Front-End.

- Recent restructuring of DAQ support has created 2 new groups moving forward
  - FEDAQ Group (Physics) combines electronics engineers with some DAQ physicists to focus on the requirements of the Front-End.
  - EPSCI Group (Experimental Physics Scientific Computing Infrastructure in CST Division) combine physicists and computer scientists to focus on development of tools for back-end processing and analysis.

- The goal is still to provide the same seamless DAQ support from detector to permanent storage for the whole experimental program at JLAB

Plans for the EIC

- Efforts are moving forward (EIC Yellow Report and the JLAB-Brookhaven partner project) in understanding the fundamental design, scale and response for the EIC detectors, which in turn define the requirements for data acquisition (DAQ) and computing resources.

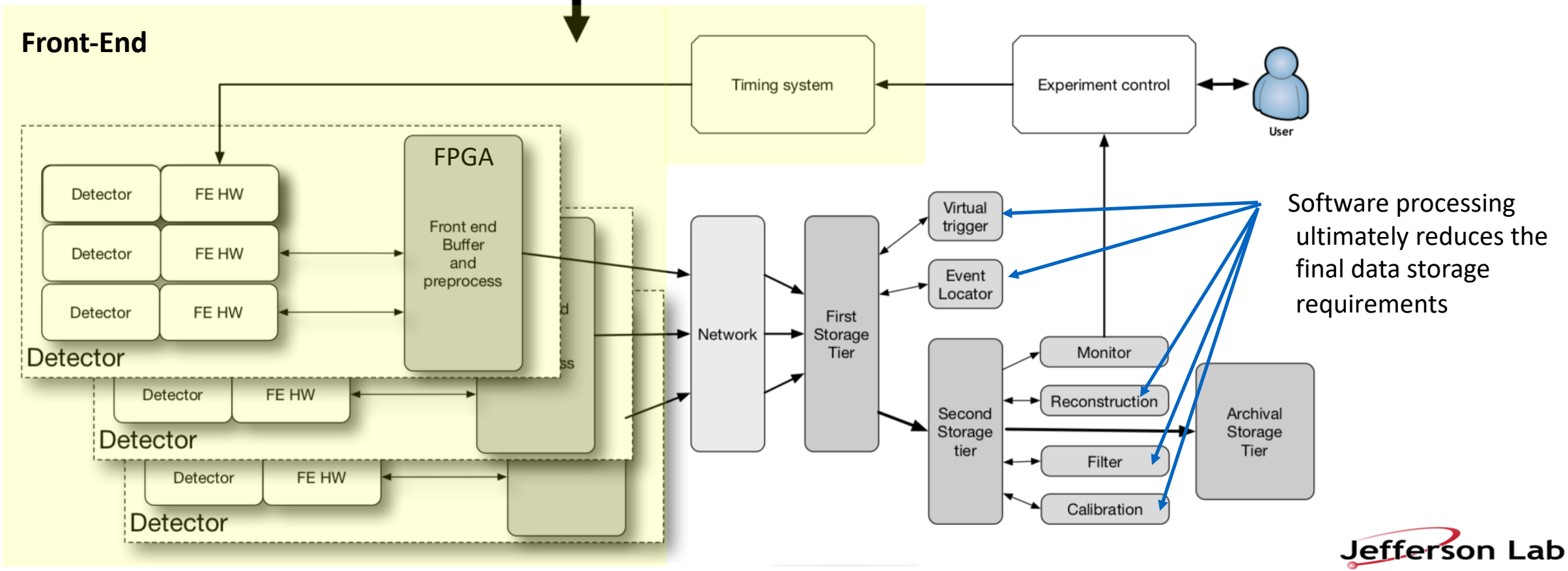
- There is a general consensus from those who are involved in the ongoing developments for the EIC project for DAQ and computing that the so-called Streaming Model should be supported as opposed to the traditional Triggered Model.

- Streaming can be thought of as a kind of ultimate goal in data acquisition, but what does it all mean in practical terms? At JLAB we are actively looking at how we can implement streaming for current and future experiments here. This has a direct translation on how it may evolve for the EIC.

- The primary focus of this talk will be on the JLAB Front-End systems.

What does Streaming look like?

- A timing system synchronizes streams at source.
- Front-end outputs data in streaming format on a net.
- DAQ consists of tiers processing separated by tiers of temporary storage



Software processing ultimately reduces the final data storage requirements

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CODA

- What is CODA (also see coda.jlab.org)
  - Software toolkit for implementing data acquisition systems.
  - Hardware/Electronics
    - Custom boards like the Trigger Interface, TDCs and ADCs.
    - Support for commercial hardware.
  - Software includes :
    - Interface with electronics (libraries/drivers).
    - Readout Front End and format data (ROC)
    - Inter-process communication - Control and Data (cMsg)
    - Merge data streams – Event building (DC, PEB, SEB)
    - Give users access to data for analysis and monitoring (ET System)
    - Online Farm / Software Trigger (FCS)
    - Write data to files (EVIO, ER)
    - Manage and control the data acquisition system (AFECS/RunControl)

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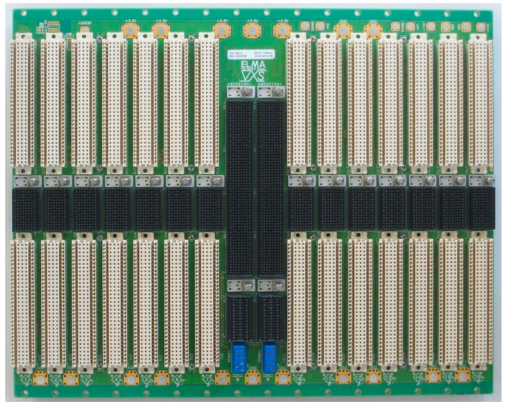
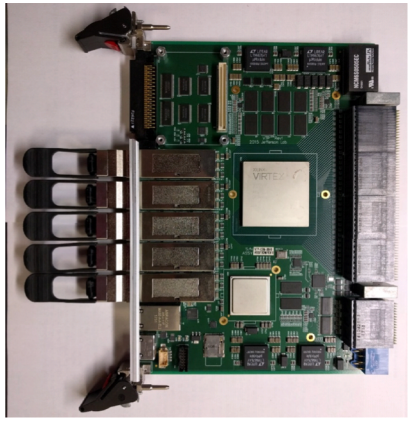
The VXS Front-end

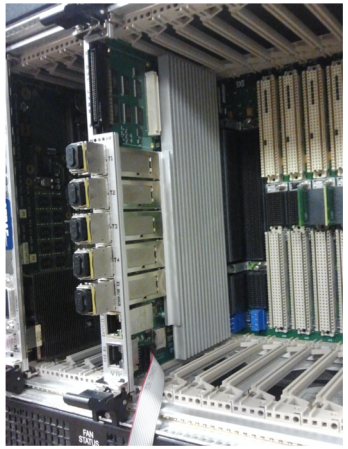
- The VXS crate supports
  - VME64x Backplane (19 slots) Readout ~200MB/s
  - High speed serial crossbar (20Gbps from each of 18 payload slots to 2 switch slots).
- Payload modules include:
  - 250 MHz Flash ADCs (16 chan/module)
  - JLAB SSP: general FPGA board supporting up to 32 fiber links from custom front-end electronics.
- VME CPU + JLAB Trigger Processor (VTP) provide Linux OS with access to both.
- We standardized on this platform for the 12GeV upgrade.
  - JLAB has a bunch of these crates.
  - We can use them for both Triggered and Streaming readout

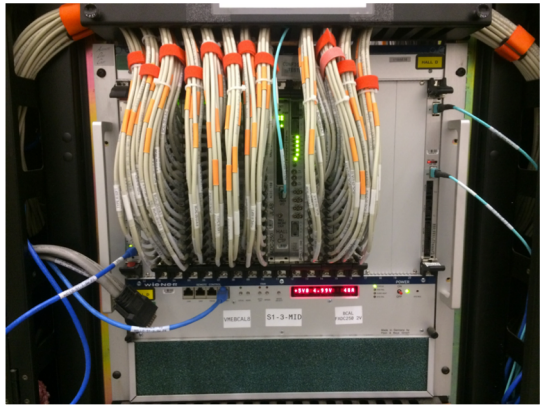


VXS



VTP





VXS Crate supporting both Trigger processing and readout

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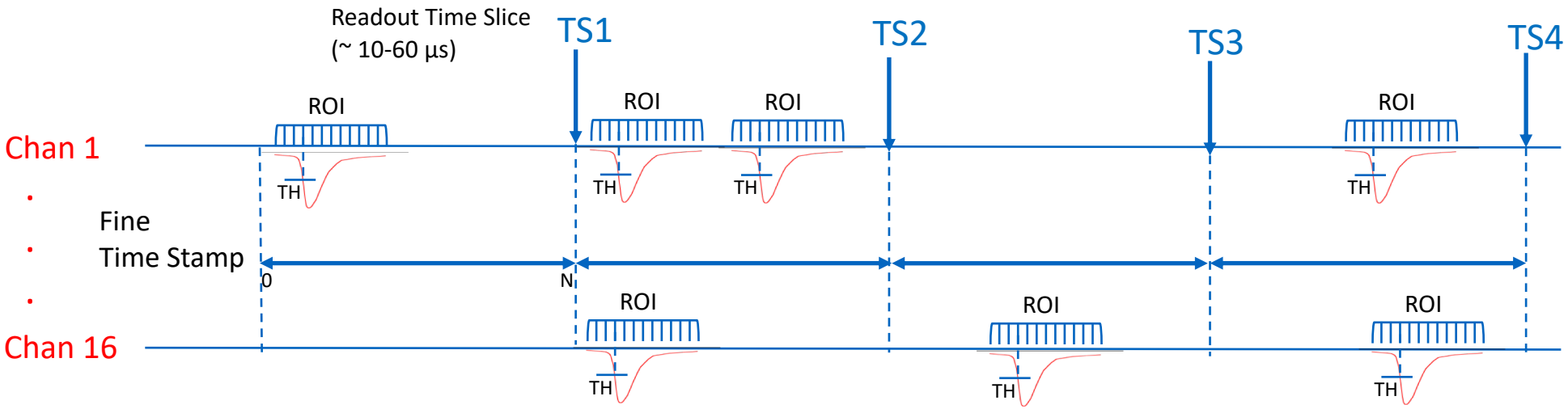
JLAB FADC in “Streaming Mode”

Streaming data can be thought of as Triggered mode where the trigger is a fixed pulser and you keep all the data for a single channel generated from the last pulse.

A 250 MHz FADC generates a 12 bit sample every 4ns. That’s 3 Gb/s for one channel. A 16 channel module is 48 Gb/s. That is over twice the available VXS bandwidth. But we don’t need ALL the data.



Within the FPGA we keep only the data around a Region of Interest (ROI) from each channel, along with a fine time stamp in each time slice window.

Depending on hit rates and available bandwidth , We can keep the individual samples or just compute a sum.

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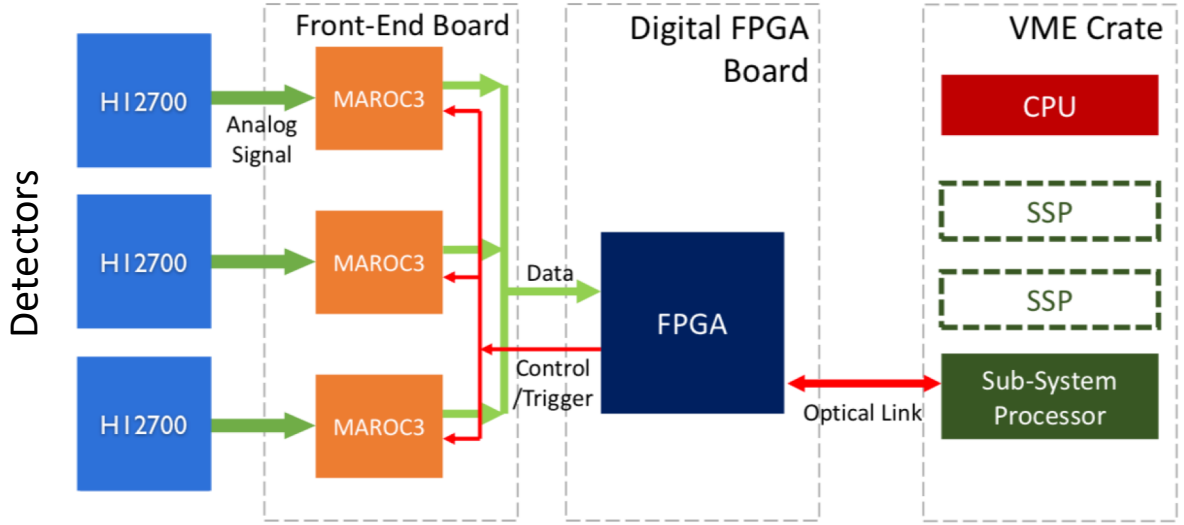
Front-End Electronics – without the crate!

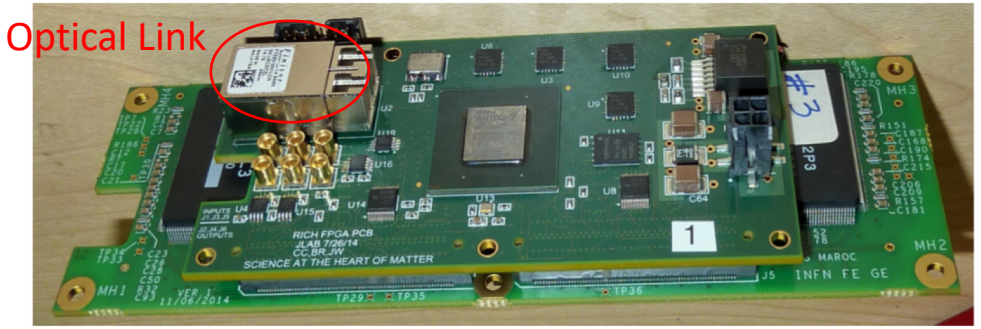
- More recent Front-End Electronics (FEE) developed by the FEDAQ group have been implemented in several detectors (CLAS12 RICH and GlueX DIRC).
- Currently the detector data is sent to another FPGA board in a VXS crate (JLAB SSP Board). This is necessary for the Triggered readout model.
- In the Streaming Model the FPGA, via the optical link, can send data directly to the Back-End Processing via standard Ethernet/TCP protocols.



MAROC ASIC "Front-End" Board

ASIC board produced for the RICH detector for CLAS12 with MAROC chips installed

FPGA Daughter Board



FPGA b Screenshot for the RICH detector for CLAS12 with ASIC board attached

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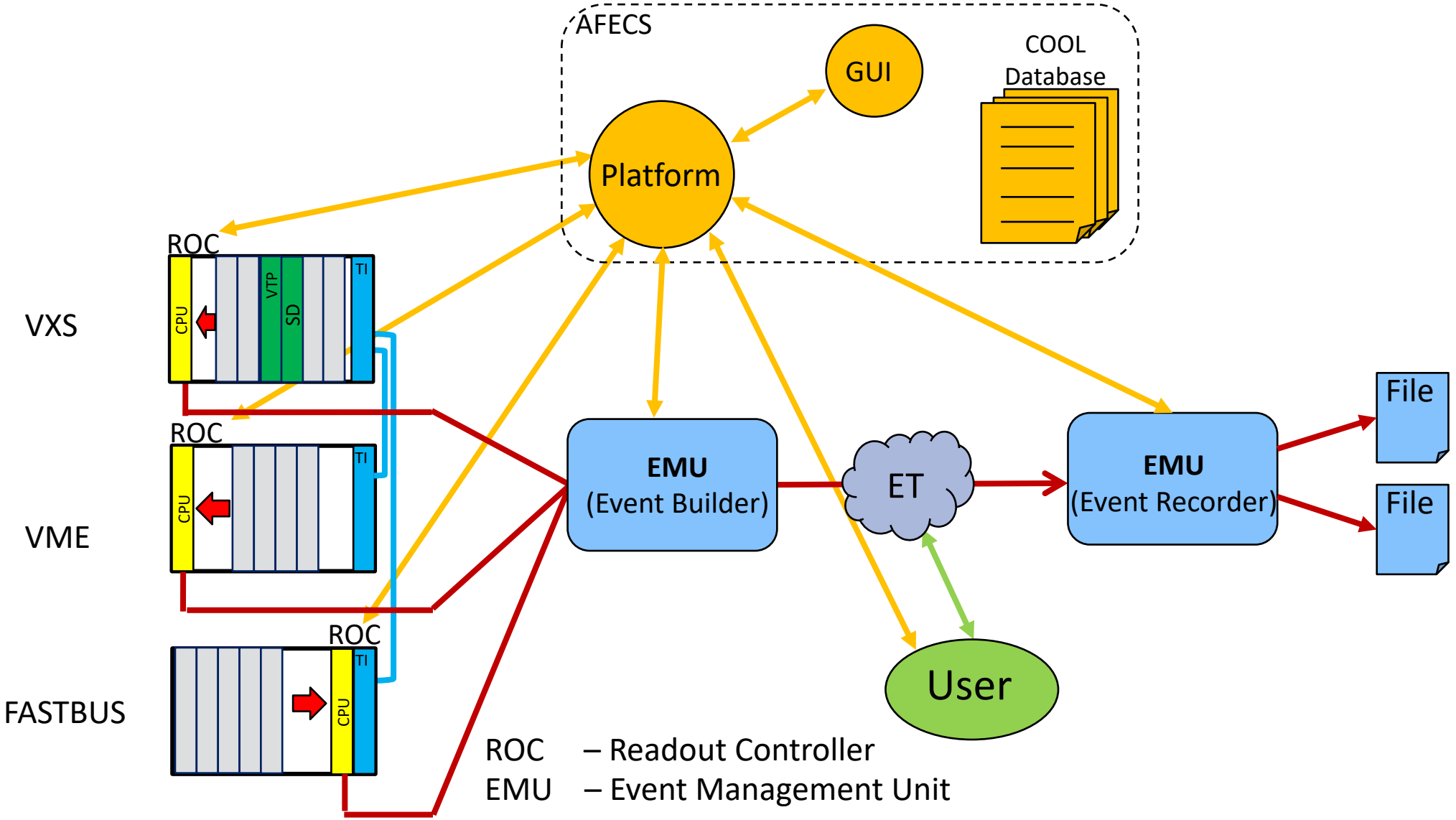
What does CODA look like?



ROC – Readout Controller
EMU – Event Management Unit
ET – Event Transport
AFECS – Agent Framework Experiment Control System

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Multi-staged and parallel

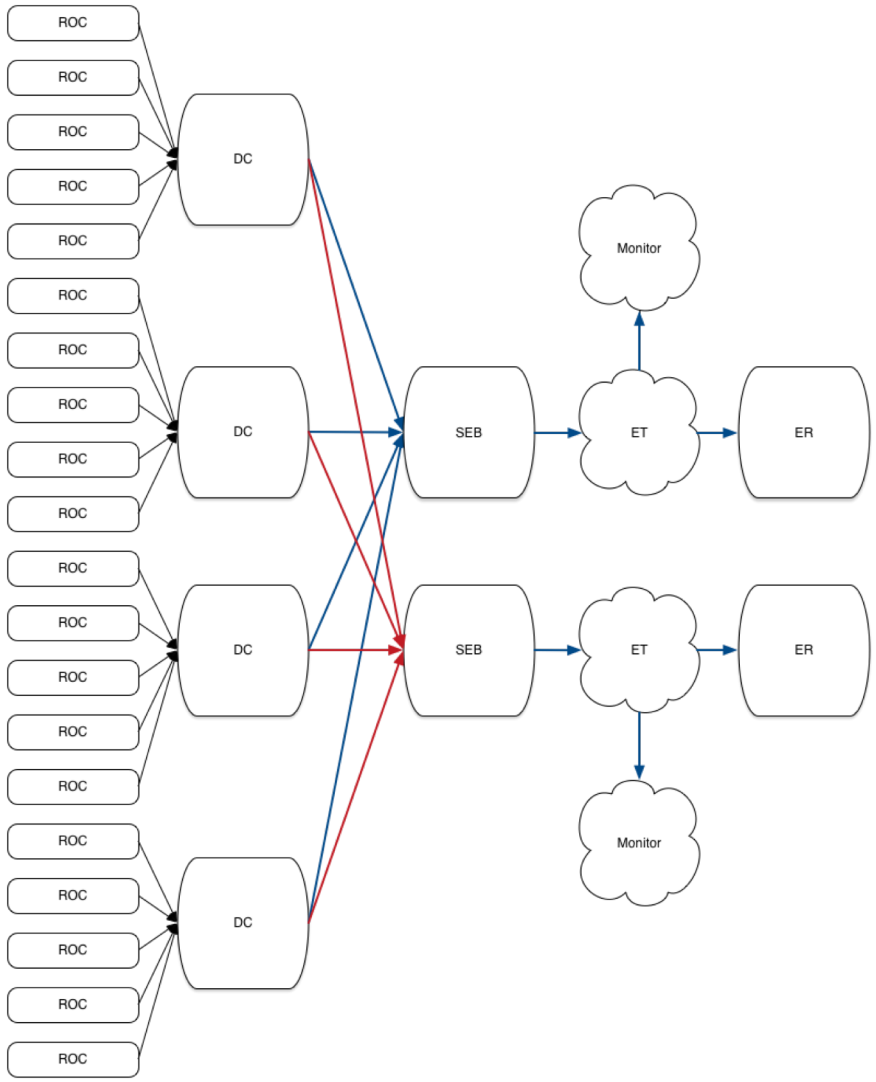
- CODA is modular and can be scaled
  - Multi-stage Event Building
  - Parallel “streams”

- Architecturally one can not really differentiate if this represents a “Triggered” system or a “Streaming” system.

- In evolving CODA to support streaming readout we are initially looking to the Front-End - where the streams originate.

- We have seen the initial experience this Fall with TRIDAS tests in Hall B which provide a proof of principle.

- Now at JLAB we want to work on how to standardize the Front-End to support both Triggered and Streaming architectures in all 4 Experimental Halls.



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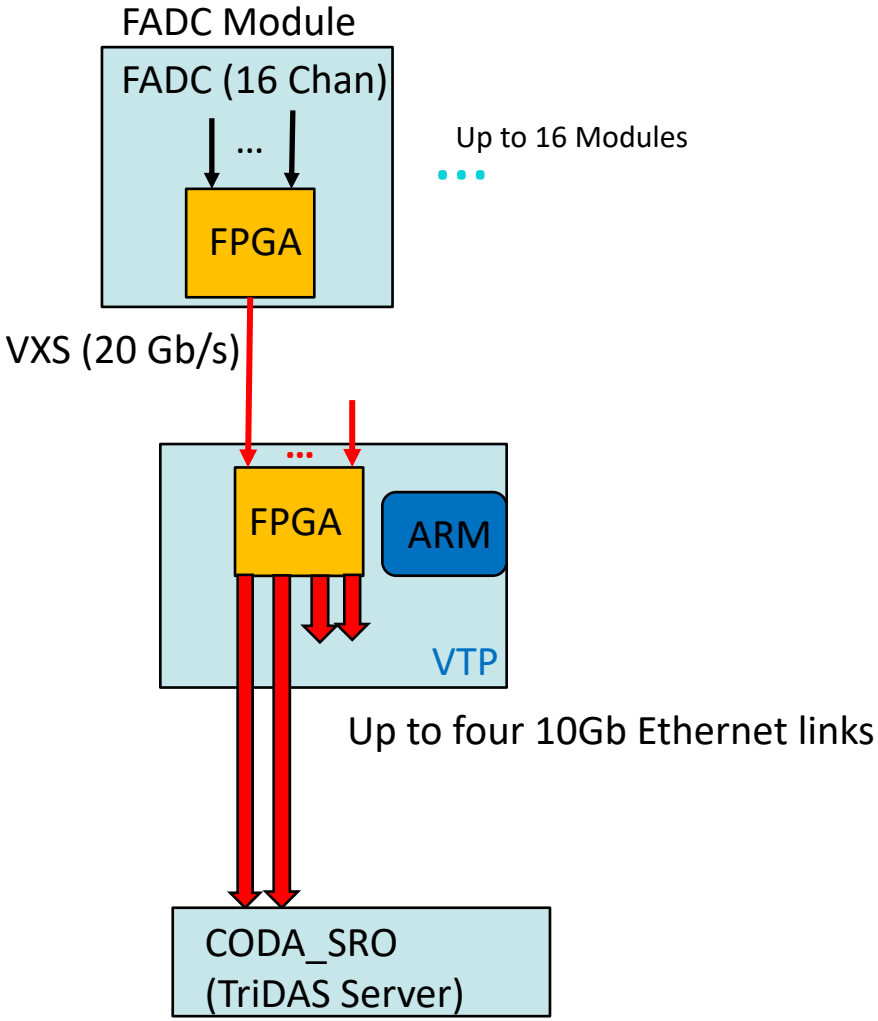
TriDAS Streaming tests

- A proof of principle test was made in Hall B last Fall using the VXS architecture with JLAB front-end electronics.
- 3 VXS crates with JLAB 250 MHz Flash ADCs digitized Forward Tagger data.
  - Integrated sums and threshold times were sent via VXS to the VTP.
- The VTP collected time slices (~ 30 μs) of data and sent them via 2 10 Gb ethernet links to a server running a special CODA component.
  - Each link sent 3 FADC modules of data
- An important question in the Streaming model is how to discard data when the system is backed up.
  - There is no “trigger” to disable
  - Flow control must be implemented in the FPGAs
  - In the TriDAS system VTP time slices were simply discarded if there was no available output buffers to hold them.



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CODA “Gen 4” – Streaming

- The primary goal for Streaming support at JLAB is to provide a “standardized” framework and set tools to allow for multiple experiments to take advantage of it

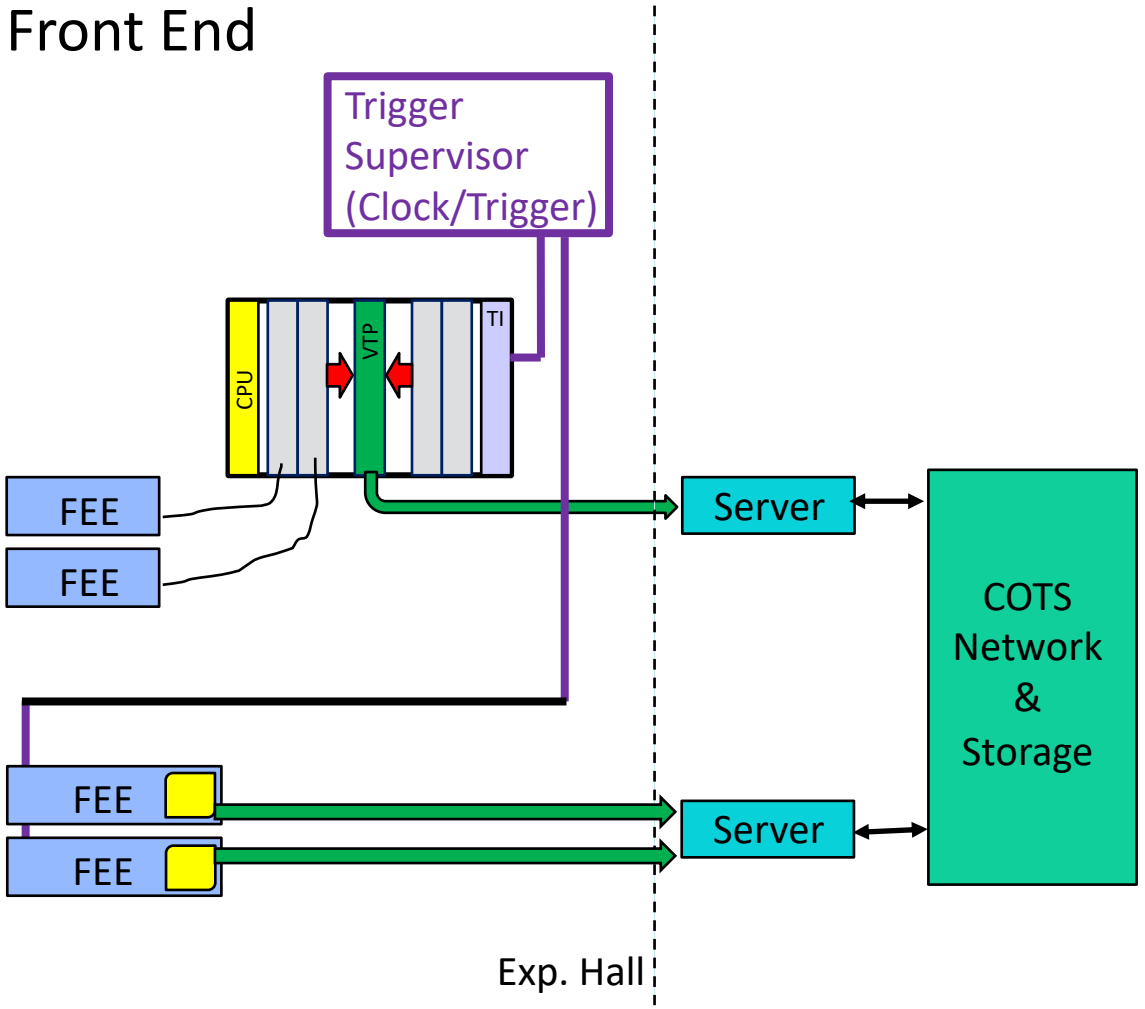
- A transition to support of Streaming does not have to be done at the expense of the older Trigger based systems. A “Hybrid” system seems not only possible but actually preferred.
  - JLAB clock/trigger distribution already exists and is suitable for both modes.

- Flexible FPGA based front-ends can be enhanced by providing a User friendly and adaptable software framework (the CODA ROC) along with general driver libraries allowing User configuration and/or loading of custom firmware objects in the FPGA at runtime.

- CODA Back-End components supporting the streaming model are being developed (by the EPSCI group) and can be integrated with the AFECS Run control system as well as with possible online processing/filtering framework like JANA2

JLAB Streaming examples

From S. Boyarinov – Streaming readout VI Workshop



Possible CLAS12-based full scale streaming data rates (based on CLAS12 RGA 50nA occupancies)

ECAL	adcecal1..6	24 x 10G	~0.6GByte/s (4% link capacity)
PCAL	adcpcal1..6	24 x 10G	
FTOF	adcftof1..6	24 x 10G	~1GByte/s (6% link capacity)
CTOF/ HTCC	adcctof1	4 x 10G	~0.1GByte/s (1% link capacity)
CND	adccnd1	4 x 10G	~0.15GByte/s (1% link capacity)
FT/ HODO	adcft1..3	12 x 10G	~0.2GByte/s (1.3% link capacity)
DC	dc11..63	6 x 12 x 10G	~10GByte/s (11% link capacity)
SVT	svt1..2	8 x 10G	~1.70GByte/s (17% link capacity)
RICH	rich4	4 x 10G	~0.20GByte/s (4% link capacity)
MM	mmft1 mvt1..2	12 x 10G	Not clear if streaming compatible

Total Streaming Data rate: ~15GBytes/sec
Data rate in triggered mode: ~300MByte/sec

188 “streams” off the detector

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Summary

- From the very beginning JLAB has focused on hardware and software DAQ support flexible enough for use in all the experimental halls.

- The next generation of DAQ development at JLAB is clearly focused on Streaming readout, but we cannot abandon what we have now.
  - Development of a hybrid system is our current path forward

- Primary attention has to be toward the 12GeV program, but close collaboration with BNL and the EIC community can bring useful advances.