Nuclear Physics Division
Fast Electronics Group

VTP Manual

Benjamin Raydo
September 2016

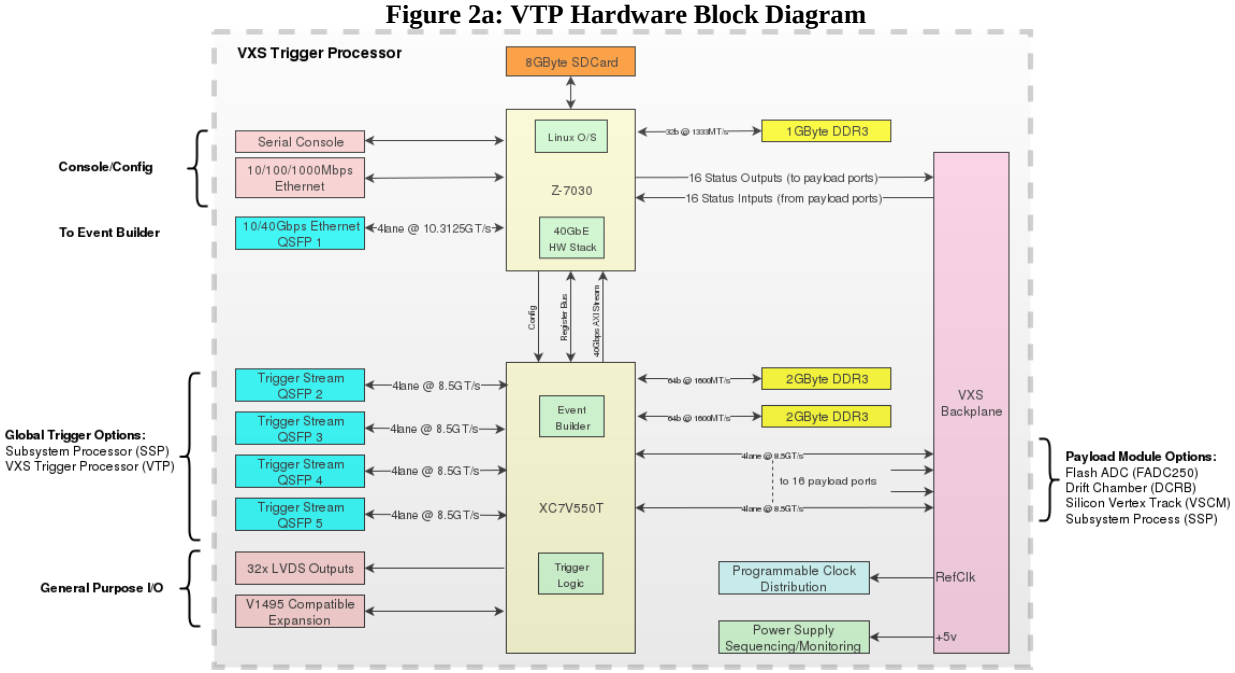
Table of Contents

1 Introduction

The VXS Trigger Processor (VTP) module is a VXS switch card module that participates in the Level 1 trigger in front-end VXS crates (a.k.a. the CTP switch slot) as well as the global-trigger VXS crate (a.k.a. the GTP switch slot). The VTP design supersedes the CTP and GTP designs as it contains more backplane serial links to front-end payload modules, more fiber optics serial links to other crates, and more FPGA resources for trigger logic. Additionally it contains a dual-core 1GHz ARM processor core that runs a CODA ROC on a Linux O/S capable of event building trigger diagnostic information from FPGA trigger logic. The processor utilizes 1Gbps Ethernet connection for configuration, control, and filesystem. Additionally a 10Gbps and 40Gbps Ethernet can be used for the CODA ROC readout in a future firmware/software development. This high speed readout can be used to read from compatible Jlab VXS electronics as an alternative to VME which provides significantly more bandwidth for future experiments that demand this.

2. Functional Description

Figure 2a: VTP Hardware Block Diagram



2.1 XC7V550T FPGA

The XC7V550T FPGA manages all the VXS backplane and optical serial streams. Custom trigger firmware collects information from the front-end (VXS payload) modules using 4 full duplex SerDes lanes. Up to 4 QSFP front panel ports can be used to communicate trigger information of other front-end crates and to the global trigger crate. LVDS (32) outputs can be used to send fixed latency trigger signals to a TI master for local crate triggering or TS (Trigger Supervisor) for global system triggering. A V1495 compatible mezzanine connector exists that allow use of commercially available ECL/TTL/NIM/ADC/DAC expansion modules mainly to eliminate the need for external level translators. Two DDR3 memories interfaces exists (each with 100Gbps bandwidth) that can be used for large event data buffers in future event building applications, debug/trace buffers, trigger logic dictionaries, histograms, etc. Dual 16bit AXI streaming busses providing a total of 40Gbps connect to the Zynq FPGA which can be used to transport high speed event data to the 10/40Gbps Ethernet. For FPGA configuration and register access a 32bit data slave bus exists which connects to the Zynq FPGA who acts as the bus master.

Summary of Features for the XC7V550T

- 16x VXS payload interfaces: 4 full duplex lanes @ up to 8.5Gbps each
- 4x QSFP interfaces: 4 full duplex lanes @ up to 8.5Gbps each
- 2x DDR3 interfaces: 64bits each @ 1600MT/s
- Dual 16bit AXI streaming bus (up to 40Gbps) transmitter to XC7Z7030

- TRIG1, TRIG2, SYNC from VXS
- 32bit LVDS output (>250Mbps per bit)
- 32bit V1495 daughtercard expansion (A395x)
- Virtex7 FPGA (364000LUT, 692800FF, 5MB BRAM, 2880DSP)

Summary of Responsibilities for the XC7V550T

- Manage 80SerDes links on the 16 VXS payload and 4 QSFP interfaces
- Run detector/experiment specific level 1 trigger algorithms
- Provide scalers and configuration registers to monitor/manage level 1 trigger
- Receive readout trigger and build experiment specific event data, stream to ROC in ZYNQ
- (Future) receive event data from 16 VXS payload and stream to ROC/EB in/through ZYNQ

2.2 XC7Z7030 FPGA

The XC7Z7030 is an FPGA and processor contained in a single chip. The processor is a dual ARM Cortex-A9 which runs Linux and the FPGA provides reasonably large resources to deal with hardware interfaces.

Summary of Features for the XC7Z7030

- Dual ARM Cortex A9 1GHz processor, 1GB DDR3 RAM 32bit @ 1333MT/s
- Bootloader in microSD card
- RS232 Console (115200bps, 8b, np) – used for boot configuration and debug terminal
- 10/100/1000Gbps Ethernet – used by Linux O/S
- 32bit data/address bus master which memory maps register space of XC7V550T into processor
- 16bit FPGA configuration bus for programming XC7V550T image
- Dual 16bit AXI streaming bus (up to 40Gbps) receiver from XC7V550T
- 10/40Gbps Ethernet – intended for FPGA accelerated TCP/IP stack for high speed event building
- 1Gbps TI (PP18) full duplex link
- Kintex7 FPGA (78600LUT, 157200FF, 1MB BRAM, 400DSP)

Summary of Responsibilities for the ZYNQ Processor/FPGA

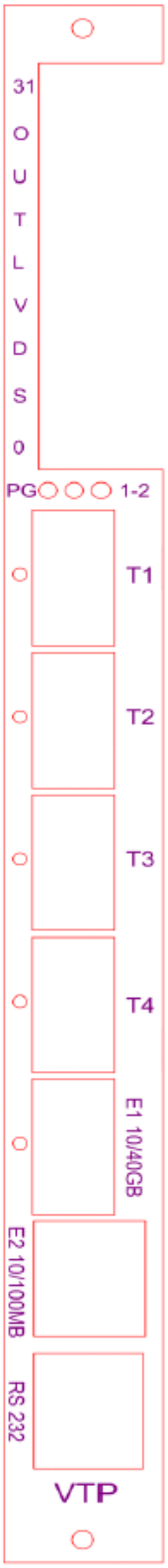
- Execute FSBL and U-Boot bootloaders from microSD card, load centrally managed Linux kernel and filesystem from NFS
- Program XC7Z7030 and XC7V550T FPGA images on boot from network
- Runs CODA ROC, event building data from TI and XC7V550T
- Report various scalers, temperatures/voltages to EPICS IOC
- Provides drivers for all VTP peripherals
- (Future) use 10/40Gbps Ethernet to stream event builder data from partial hardware accelerated ROC

3.1 Specification & I/O Summary

The VXS connection is used to interface to the trigger system without the need for loose cabling. This interface provides the following signals:

Signal	Description	Direction	Signal Type	Interface
Clock	125/250MHz System Synchronous Clock	In	LVPECL	SD
Trig1	L1 accept trigger bit, synchronous to clock	In	LVPECL	SD
Trig2	L1 accept trigger bit, synchronous to clock	In	LVPECL	SD
Sync	L1 synchronization bit, synchronous to clock	In	LVPECL	SD
Busy	Module busy signal	Out	LVDS	TI
GTP_TX	1Gbps VTP->TI TILINK	Out	LVDS	TI
GTP_RX	1Gbps TI->VTP TILINK	In	LVDS	TI
SDA/SCL	TI I2C slave interface	InOut	LVTTL	TI
STATOUT	Payload->VTP status input	In	LVTTL	PP1-16
STATIN	VTP->Payload status output	Out	LVTTL	PP1-16
L1 Trigger	8.5Gbps per lane (4) used to generate L1 trigger	In/Out	CML	PP1-16

3.2 Specification Summary



MECHANICAL

- Single width VITA 41 (VXS) Switch Module

Trigger Interface and Switch B signaling
(Signal Distribution module)

- 250MHz Clock (LVPECL)
- Trig1, Trig2, Sync (LVPECL)
- LINKUP out (LVTTL)
- BUSY out (LVTTL)

GIGABIT DATA STREAMS
From/To 16 Payload Slots (FADC, SSP, VETROC, DCRB, etc.)

- 4 full duplex lanes up to 8.5Gbps
- 544Gbps Aggregate

Outputs:

- 32 LVDS front panel outputs to Trigger Supervisor
- 1x RJ45: 100/1000Mbps Ethernet
- 32 I/O expansion mezzanine (LVDS/ECL/PECL/NIM/Analog)
- 4x QSFP Fiber Transceivers (34Gbps)
- 10/100/1000Mbps Ethernet (RJ45)
- 1x QSFP 10/40Gbps Ethernet
- RS232 console serial port

Indicators: (Front Panel)

- Power – Blue LED
- Trigger – Amber LED
- Alarm – Red LED Programming and Trigger Data Input:
- On board JTAG Port
- Virtex 7 550T; 80GTH Gigabit transceivers
- 1GHz ZYNQ-7030 SoC processor with Linux OS
- Global Trigger equation and processing for up to 16 JLAB SubSystem Processors
- Front End Trigger processing for up to 16 JLAB Flash ADC digitizers
- 8GB Micro SD card support (Linux OS file system + FPGA image)
- 1GB DDR3 SDRAM

Power Requirements:

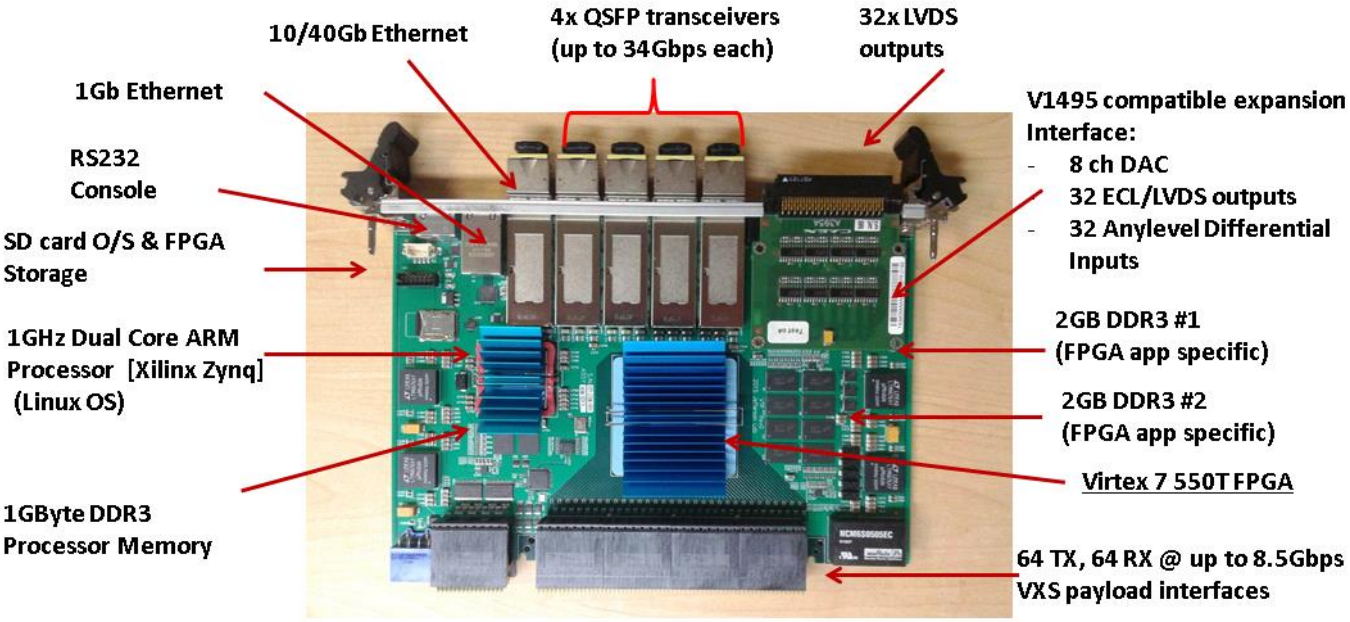
- +5v @ 10 Amps (typ. from Backplane)
- Local regulators for other required voltages

Environment:

- Forced air cooling: Heat sink
- Commercial grade components (85°C max)

4. PCB Assembly View

The VTP PCB is a 22-layer impedance controlled FR-408HR stackup



5. Readout Data Format

The word length for the readout data is 32bits. The event length is variable and depends on several factors (detector occupancy, headers, trailers, filler words).

Data Word Categories

Data words from the module are divided into two categories: Data Type Defining (bit 31 = 1) and Data Type Continuation (bit 31 = 0). Data Type Defining words contain a 4-bit data type tag (bits 30 - 27) along with a type dependent data payload (bits 26 - 0). Data Type Continuation words provide additional data payload (bits 30 – 0) for the *last defined data type*. Continuation words permit data payloads to span multiple words and allow for efficient packing of various data types spanning multiple data words. Any number of Data Type Continuation words may follow a Data Type Defining word.

Data Type List

0	Block Header
1	Block Trailer
2	Event Header
3	Trigger Time
4	ECTrigger Peak
5	ECTrigger Cluster
6	Trigger
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Data Not Valid (empty module)
15	Filler Word (non-data)

Data Type: Block Header

Type: 0x0
Size: 1 word
Description: Indicates the beginning of a block of events. (High-speed readout of a board or a set of boards is done in blocks of events)

31	30	29	28	27	26	25	24
1	0	0	0	0	-	-	-
23	22	21	20	19	18	17	16
-	-	NUM_EVENTS					
15	14	13	12	11	10	9	8
NUM_EVENTS					BLOCK_NUMBER		
7	6	5	4	3	2	1	0
BLOCK_NUMBER							

BLOCK_NUMBER:
Event block number (used to align blocks when building events)

NUM_EVENTS:
Number of events in block

Data Type: Block Trailer

Type: 0x1
Size: 1 word
Description: Indicates the end of a block of events. The data words in a block are bracketed by the block header and trailer.

31	30	29	28	27	26	25	24
1	0	0	0	1	-	-	-
23	22	21	20	19	18	17	16
-	-	NUM_WORDS					
15	14	13	12	11	10	9	8
NUM_WORDS							
7	6	5	4	3	2	1	0
NUM_WORDS							

NUM_WORDS:
Total number of words in block of events

Data Type: Event Header

Type: 0x2
Size: 1 word
Description: Indicates the start of an event. The included trigger number is useful to ensure proper alignment of event fragments when building events. The 27bit trigger number (134M count) is not a limitation, as it will be used to distinguish events within event blocks, or among events that are concurrently being built or transported.

31	30	29	28	27	26	25	24
1	0	0	1	0	TRIGGER_NUMBER		
23	22	21	20	19	18	17	16
TRIGGER_NUMBER							
15	14	13	12	11	10	9	8
TRIGGER_NUMBER							
7	6	5	4	3	2	1	0
TRIGGER_NUMBER							

TRIGGER_NUMBER:
Accepted event/trigger number

Data Type: Trigger Time

Type: 0x3
Size: 2 words
Description: Time of trigger occurrence relative to the most recent global reset. The time is measured by a 48bit counter that is clocked from the 125MHz system clock. The assertion of the global reset clears the counter. The de-assertion of global reset enables counter and thus sets t=0 for the module. The trigger time is necessary to ensure system synchronization and is useful in aligning event fragments when building events.

Word 1:

31	30	29	28	27	26	25	24
1	0	0	1	1	0	0	0
23	22	21	20	19	18	17	16
TRIGGER_TIME_H							
15	14	13	12	11	10	9	8
TRIGGER_TIME_H							
7	6	5	4	3	2	1	0
TRIGGER_TIME_H							

TRIGGER_TIME_H:

This is the upper 24bits of the trigger time

Word 2:

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
23	22	21	20	19	18	17	16
TRIGGER_TIME_L							
15	14	13	12	11	10	9	8
TRIGGER_TIME_ L							
7	6	5	4	3	2	1	0
TRIGGER_TIME_ L							

TRIGGER_TIME_L:

This is the lower 24bits of the trigger time

Data Type: ECTrigger Peak

Type: 0x4
Size: 2 words
Description: CLAS12 Electro-magnetic calorimeter trigger diagnostic words. This reports all 1-dimensional energy peaks found inside the triggered event window.

Word 1:

31	30	29	28	27	26	25	24
1	0	1	0	0	INST	AXIS	
23	22	21	20	19	18	17	16
-	-	COORD					
15	14	13	12	11	10	9	8
COORD			ENERGY				
7	6	5	4	3	2	1	0
ENERGY							

INST:

0 – first EC layer
1 – second EC layer

AXIS:

0 – U axis peak
1 – V axis peak
2 – W axis peak

COORD:

0.0-36.0: 6.3 fixed point energy weighted peak coordinate in strip units

ENERGY:

0-8191: Peak energy in units of MeV

Word 2:

31	30	29	28	27	26	25	24
0	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	TIME		
7	6	5	4	3	2	1	0
TIME							

TIME:

0-2047: Time of peak measure from beginning of trigger window in 4ns units

Data Type: ECTrigger Cluster

Type: 0x5
Size: 2 words
Description: CLAS12 Electro-magnetic calorimeter trigger diagnostic words. This reports all 2-dimensional energy clusters found inside the triggered event window.

Word 1:

31	30	29	28	27	26	25	24
1	0	1	0	1	INST	-	-
23	22	21	20	19	18	17	16
-	-	U-COORD					
15	14	13	12	11	10	9	8
U-COORD			ENERGY				
7	6	5	4	3	2	1	0
ENERGY							

INST:

0 – first EC layer
1 – second EC layer

U-COORD:

0.0-36.0: 6.3 fixed point energy weighted cluster coordinate in strip units

ENERGY:

0-8191: Cluster energy in units of MeV (path loss compensated)

Word 2:

31	30	29	28	27	26	25	24
0	-	-	W-COORD				
23	22	21	20	19	18	17	16
W-COORD				V-COORD			
15	14	13	12	11	10	9	8
V-COORD					TIME		
7	6	5	4	3	2	1	0
TIME							

W-COORD:

0.0-36.0: 6.3 fixed point energy weighted cluster coordinate in strip units

V-COORD:

0.0-36.0: 6.3 fixed point energy weighted cluster coordinate in strip units

TIME:

0-2047: Time of peak measure from beginning of trigger window in 4ns units

Data Type: Trigger

Type: 0x6
Size: 1 word
Description: Trigger word - indicates a trigger condition was found, the time, and the time inside the trigger readout window that it occurred. This is useful for tagging events during normal data taking and random triggers to be used for efficiency checking.

31	30	29	28	27	26	25	24
1	0	1	1	0	TRIGGER_TYPE		
23	22	21	20	19	18	17	16
TRIGGER_TYPE							
15	14	13	12	11	10	9	8
TRIGGER_BIT					TIME		
7	6	5	4	3	2	1	0
TIME							

TRIGGER_TYPE:
0: EC trigger 0
1: EC trigger 1
TRIGGER_BIT:
0-31: Trigger bit used
TIME:
0-2047: Time of trigger tag measure from beginning of trigger window in 4ns units

Data Type: Data Not Valid

Type: 0x14
Size: 1 word
Description: Module has no data available for readout. This can if the module is being read out too quickly after receiving (event building is in process and no data words have been put into the buffer yet) a trigger or if the module doesn't have any events to report.

31	30	29	28	27	26	25	24
1	1	1	1	0	UNDEFINED		
23	22	21	20	19	18	17	16
UNDEFINED							
15	14	13	12	11	10	9	8
UNDEFINED							
7	6	5	4	3	2	1	0
UNDEFINED							

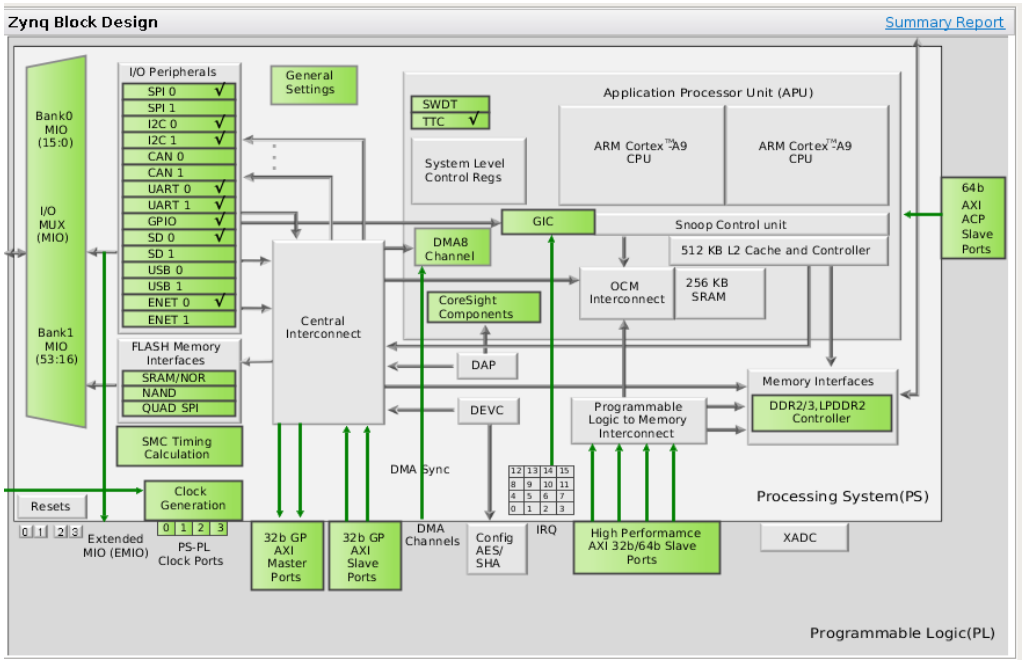
Data Type: Filler Word

Type: 0x15
Size: 1 word
Description: Non-data word appended to the block of events. This is used to force the total number of 32-bit words read out of a module to be a multiple of 2 or 4 when

31	30	29	28	27	26	25	24
1	1	1	1	1	UNDEFINED		
23	22	21	20	19	18	17	16
UNDEFINED							
15	14	13	12	11	10	9	8
UNDEFINED							
7	6	5	4	3	2	1	0
UNDEFINED							

6. Register Map

All VTP board registers (whether in Virtex 7 or Zynq 7) are memory mapped into the Zynq7 CPU address space. Many peripherals used in the Zynq7 are part of the PS (Processor System) and the Zynq7 technical reference manual can be referred to for details (ug585-Zynq-7000-TRM.pdf). The Zynq7 processor configuration is summarized in the following diagram:

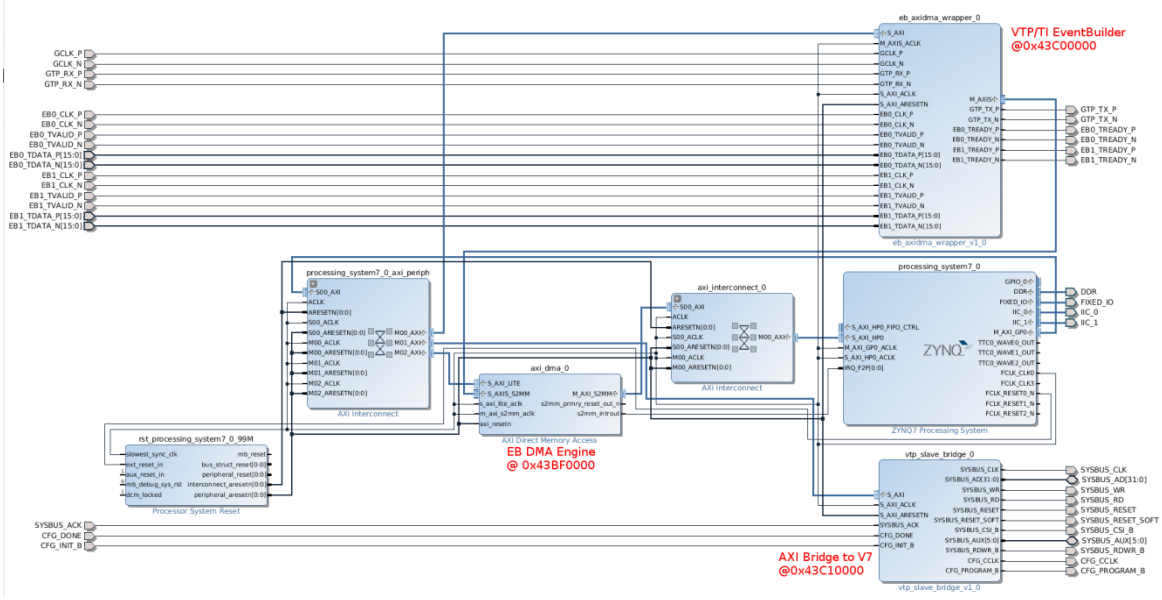


The following table indicates which PS peripherals are used on the VTP:

PS Peripherals:

Peripheral Name	Description	Address Base
SPI0	Used by: Si5341 clock synthesizer	**0xE0006000**
I2C0	Used by: 10/40Gbps QSFP for module identification & monitoring	**0xE0004000**
I2C1	Used by: LTM4676 smbus power supply monitoring	**0xE0005000**
UART0	U-boot & Linux console	**0xE0000000**
GPIO	Used by: Si5341, LEDs, 10/40Gbps QSFP, VXS STAT IN/OUT	**0xE000A000**
SD0	µSD card is the Zynq7 boot resource (contains FSBL, U-Boot)	**0xE0100000**
ENET0	10/100/1000Mbps Ethernet for U-Boot & Linux	**0xE000B000**
TTC0	U-Boot & Linux OS Timer	**0xF8001000**

Additionally, the Zynq7 contains an FPGA which currently has a few FPGA based peripherals. The Zynq7 processor and FPGA system is shown in the following diagram. The Zynq7 connects to the FPGA based peripherals (axi_dma0, eb_axidma_wrapper_0, vtp_slave_bridge_0) using the Master AXI bus interface (this is a 32bit data bus used for accessing control/status registers in both Zynq and V7 FPGAs). The "eb_axidma_wrapper_0" peripheral buffers and combines event block streams from the V7 and TI where the "axi_dma_0" peripheral takes the stream and can DMA it to the Zynq7 processor over the S_AXI_HP0 bus (which connects to the DDR3 memory).



FPGA Peripherals:

Register Name	Description	Address Offset
Event Builder peripheral	**VTP/TI Event Builder**	**0x43C00000**
LinkCtrl	TI<->VTP Serial Link Control	0x0000
TiCtrl	TI Control	0x0004
LinkStatus	TI<-> VTP Serial Link Status	0x0008
TiStatus	TI Status	0x000C
EbCtrl	Event Builder Control	0x0010

EB AXI DMA peripheral		**0x43BF0000**

V7 Bridge & FPGA Config		**0x43C10000**
Bridge space	Memory maps a ~64kByte window of V7 into Zynq7	0x0000
V7Status	V7 FPGA Configuration Status	0xFFF4
V7Ctrl	V7 FPGA Control	0xFFF8
V7Cfg	V7 FPGA Configuration	0xFFFC

V7 Clk peripheral		**0x43C10100**
Ctrl	Clock control	0x0000
Status	Clock status	0x0004

Sd peripheral (offset 0x0200)		**0x43C10200**
Ctrl	Sd Control	0x0000
Status	Sd Status	0x0004
ScalerLatch	Scaler latch control	0x0008
FPAOSel	Front Panel LVDS[31:0] Source Selection Control	0x0010
FPBOSel	Front Panel Mezzanine Source Selection Control	0x0014
BusySel	Busy Source Selection Control	0x0018
Trig1Sel	Trig1 Source Selection Control	0x001C
SyncSel	Sync Source Selection Control	0x0020
FPAOVal	Front Panel LVDS[31:0] Output Value	0x0040
FPBOVal	Front Panel Mezzanine Output Value	0x0044
FPBIStatus	Front Panel Mezzanine Input Status	0x0060
Trig1Status	Trig1 Status	0x0064
Trig2Status	Trig2 Status	0x0068
SyncStatus	Sync Status	0x006C

FadcDecoder peripheral		**0x43C10300**
Ctrl	Fadc Enable Control	0x0000
Latency[0-15]	Fadc Latency Status	0x0020 … 0x005C

VXS Serdes peripheral		**0x43C11000 … 0x43C11F00**
Ctrl	GTH Control	0x0000
Status	GTH Statusl	0x0004
DrlCtrl	Drp Control	0x0008
DrpStatus	Drp Status	0x000C

QSFP Serdes Peripheral		**0x43C12000 … 0x43C12300**
Ctrl	GTH Control	0x0000
Status	GTH Statusl	0x0004
DrlCtrl	Drp Control	0x0008
DrpStatus	Drp Status	0x000C

ECTrigger Peripheral		**0x43C14100 … 0x43C14200**
Ctrl	EC Trigger Control	0x0000

Trigger Ouptut Peripheral		**0x43C15000**
Latency	Trigger Latency control	0x0000
Width	Trigger Width Control	0x0004
BusyScaler		0x0010

V7 Event Builder Peripheral		**0x43C15100**
BlockSize	Event Builder Block Size	0x0000
TriggerFifoBusyThreshold	Queued Trigger Busy Threshold	0x0004
Lookback	Readout Window Lookback	0x0008
WindowWidth	Readout Window Width	0x000C

6.1 Event Builder Peripheral (Base Address 0x43C00000)

Register: LinkCtrl

Address Offset: 0x0000
Size: 32bits
Reset State: 0x0000000F

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	FIFORST	RXFIFORST	PLLRST	RXRST

FIFORST (RW):

'1' - TI & V7 event builder buffers reset
'0' - TI & V7 event builder buffers active

RXFIFORST (RW):

'1' - TI link receiving command FIFO reset
'0' - TI link receiving command FIFO active

PLLRST (RW):

'1' - GCLK PLL reset
'0' - GCLK PLL active

RX_RESET (RW):

'1' - TI link RX reset
'0' - TI link RX active

Notes:

For initial board configuration or when input clock changes:

1. Assert all reset bits
2. Wait until GCLK reference has been selected and stable (i.e. setup Si5341)
3. Release PLLRST reset first and confirm PLL locks (by checking bit GCLK_PLL_LOCKED in LinkStatus)
4. Release RX_RESET and confirm TI link is working (by checking bit RX_READY in LinkStatus)
5. Release RXFIFORST

Before triggers are allowed to be released:

1. Assert FIFORST to clear event builder buffers, then de-assert
2. Enable triggers

Register: TiCtrl

Address Offset: 0x0004
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	SYNCEVTRST	TI_ACK	TI_BL_REQ

SYNCEVTRST (WO):

'1' - Clear SYNC event flag
'0' - does nothing

TI_ACK (WO):

'1' -Send block acknowledgement to TI
'0' - does nothing

TI_BL_REQ (WO):

'1' - Send block level request to TI
'0' - does nothing

Register: LinkStatus

Address Offset: 0x0008
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	GCLK_PLL_LOCKED	-	RX_READY
15	14	13	12	11	10	9	8
RX_ERROR_CNT							
7	6	5	4	3	2	1	0
RX_ERROR_CNT							

GCLK_PLL_LOCK (RO):

'1' - GCLK PLL is locked
'0' - GCLK PLL in not locked

RX_READY (RO):

'1' - TI link receiver is locked
'0' - TI link receiver is not locked

RX_ERROR_CNT (RO):

TI link received words having a soft error or disparity violation

Register: TiStatus

Address Offset: 0x000C
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	SYNC_EVT
15	14	13	12	11	10	9	8
NEXT_BL							
7	6	5	4	3	2	1	0
CUR_BL							

SYNC_EVT (RO):

'1' - Sync event received since last Sync event reset
'0' - No sync event received since last Sync event reset

NEXT_BL (RO):

TI next block level

CUR_BL (RO):

TI current block level

Register: EbCtrl

Address Offset: 0x0010
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	BUILDVTP	BUILDTI

BUILDVTP (RW):

'1' - VTP events are put of event data stream that DMA engine reads
'0' - VTP events not part of event data stream that DMA engine reads

BUILDTI (RW):

'1' - TI events are put of event data stream that DMA engine reads
'0' - TI events not part of event data stream that DMA engine reads

6.2 AXI DMA Peripheral (Base Address 0x43BF0000)

Refer to AXI DMA v7.1 manual (pg021_axi_dma.pdf) for details on this peripheral. It is a IP block from Vivado and is responsible for performing DMA operations to efficiently move data from Event Builder buffers into the Zynq7 processor memory.

For Linux driver/device-tree setup refer here:
http://www.wiki.xilinx.com/DMA+Drivers+-+Soft+IPs#AXI%20DMA--Device%20Tree%20Node

6.3 V7 Bridge & FPGA Config (Base Address 0x43C10000)

This peripheral bridges the V7 register space into the Zynq7 processor memory space. It uses a custom bus/protocol and is also used as the configuration interface for the V7 FPGA image. The V7 FPGA is setup as a 16bit SelectMap slave device for configuration. The last three 32bit words in the 64kB peripheral space are used for V7 FPGA configuration control and status registers, while the remaining lower space in the 64kB peripheral space maps registers in the V7 FPGA. This allows the Zynq7 processor to read/write registers using normal memory reads/writes.

Register: V7Status

Address Offset: 0xFFF4
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	INIT_B	DONE

INIT_B (RO):

Reads the V7 INIT_B status
'0' - indicates V7 FPGA configuration is in the reset state

DONE (RO):

Reads the V7 DONE status
'1' - indicates the V7 FPGA configuration is valid and running
'0' - indicates the V7 FPGA configuration is invalid or incomplete

Register: V7Ctrl

Address Offset: 0xFFF8
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	PROGRAM_B	RDWR_B	CSI_B	RESET_SOFT	RESET

PROGRAM_B (WO):

'0' - FPGA configuration reset
'1' - FPGA configuration can commence

RDWR_B (WO):

'1' - indicates the V7 FPGA configuration bus will perform a read on next V7Cfg access
'0' - indicates the V7 FPGA configuration bus will perform a write on next V7Cfg access

CSI_B (WO):

'1' - deselects V7 FPGA configuration
'0' - selects V7 FPGA configuration

RESET_SOFT (WO):

'1' - asserts soft reset signal to Z7 and V7 peripherals
'0' - deasserts soft reset signal to Z7 and V7 peripherals

RESET (WO):

'1' - asserts hard reset signal to Z7 and V7 peripherals
'0' - deasserts hard reset signal to Z7 and V7 peripherals

Register: V7Cfg

Address Offset: 0xFFFC
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
CFG_DATA							
7	6	5	4	3	2	1	0
CFG_DATA							

CFG_DATA (RW):

Data to read/write to the V7 configuration interface

6.4 V7 Clk (Base Address 0x43C10100)

Register: Ctrl

Address Offset: 0x0000
Size: 32bits
Reset State: 0x00000001

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	GCLK_RESET

GCLK_RESET (RW):

'1' - GCLK PLL reset
'0' - GCLK PLL run

Register: Status

Address Offset: 0x0004
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	GCLK_LOCKED

GCLK_LOCKED (RO):

'1' - GCLK PLL locked
'0' - GCLK PLL not locked

6.5 Sd (Base Address 0x43C10200)

Register: Ctrl

Address Offset: 0x0000
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	FPB_OEN	FPB_SEL

FPB_OEN (RW):

Front panel mezzanine expansion board Output Enable (Inverted) control. Not all mezzanine board types can disable their output. Refer to mezzanine board document on how this signal will control that board type (A395D: 0=enable, 1=disable).

FPB_SEL (RW):

Front panel mezzanine expansion board signal format selection control. Not all mezzanine board types can disable their output. Refer to mezzanine board document on how this signal will control that board type (A395D: 0=NIM, 1=TTL).

Register: Status

Address Offset: 0x0004
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	FPB_ID		

FPB_ID (RO):

Front panel mezzanine expansion board identifier:

0: A395A (32 x IN LVDS/ECL)
1: A395B (32 x OUT LVDS)
2: A395C (32 x OUT ECL)
3: A395D (8 x IN/OUT NIM/TTL)

Register: ScalerLatch

Address Offset: 0x0008
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	LATCH

LATCH (RW):

Distributed to board scalers & histograms for global control capture of counters. Two types of counters (buffered & unbuffered) use this signal differently. For buffered counters, the counter is copied to the readout register on the 0>1 transition of LATCH allowing dead-timeless operation. For unbuffered counters, the counts is halt while LATCH is 1, this allows all counters to stop for readout, then when LATCH returns to 0 the counters can continue to count.

Register: FPAOSel

Address Offset: 0x0010
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
SEL							
23	22	21	20	19	18	17	16
SEL							
15	14	13	12	11	10	9	8
SEL							
7	6	5	4	3	2	1	0
SEL							

SEL (RW):

Each bit in SEL corresponds to the same bit on the front panel LVDS output bus.
'1' - bit uses user programmable logic to drive LVDS bit
'0' - bit uses FPAOVal register bit to drive LVDS bit

Register: FPBOSel

Address Offset: 0x0014
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
SEL							
23	22	21	20	19	18	17	16
SEL							
15	14	13	12	11	10	9	8
SEL							
7	6	5	4	3	2	1	0
SEL							

SEL (RW):

Each bit in SEL corresponds to the same bit on the front panel mezzanine output bus.
'1' - bit uses user programmable logic to drive mezzanine output bit
'0' - bit uses FPBOVal register bit to drive mezzanine output bit

Register: BusySel

Address Offset: 0x0018
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	SEL	

SEL (RW): determines what is output on VXS BUSY signal to TI
- 0 - '0'
- 1 - '1'
- 2 - VTP Event Builder BUSY logic
- 3 - reserved

Register: Trig1Sel

Address Offset: 0x001C
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	SEL	

SEL (RW): determines what signal is routed to VTP internal Trig1
- 0 - '0'
- 1 - '1'
- 2 - VXS Trig1
- 3 - reserved

Register: SyncSel

Address Offset: 0x0020
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	SEL	

SEL (RW): determines what signal is routed to VTP internal Sync
- 0 - '0'
- 1 - '1'
- 2 - VXS Sync
- 3 - reserved

Register: FPAOVal

Address Offset: 0x0040
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

VAL (RW):

Each bit in VAL corresponds to the same bit on the front panel LVDS output bus when the corresponding bit in FPAOSel is set to drive a value from this register.

Register: FPBOVal

Address Offset: 0x0044
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

VAL (RW):

Each bit in VAL corresponds to the same bit on the front panel mezzanine output bus when the corresponding bit in FPBOSel is set to drive a value from this register.

Register: FPBIStatus

Address Offset: 0x0060
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

VAL (RO):

Each bit in VAL corresponds to the bit value read on the front panel mezzanine input bus.

Register: Trig1Status

Address Offset: 0x0064
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	STATUS

STATUS (RO):

Value read on VXS Trig1 line

Register: Trig2Status

Address Offset: 0x0068
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	STATUS

STATUS (RO):

Value read on VXS Trig2 line

Register: SyncStatus

Address Offset: 0x006C
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	STATUS

STATUS (RO):

Value read on VXS Sync line

6.6 Fadc Decoder (Base Address 0x43C10300)

Register: Ctrl

Address Offset: 0x0000
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
PP16EN	PP15EN	PP14EN	PP13EN	PP12EN	PP11EN	PP10EN	PP9EN
7	6	5	4	3	2	1	0
PP8EN	PP7EN	PP6EN	PP5EN	PP4EN	PP3EN	PP2EN	PP1EN

PPxEN (RW):

'1' - enabled VXS payload port x for trigger processing.
'0' - disables VXS payload port x for trigger processing.

Register: Latency[]

Address Offset: 0x0020, 0x0024, …, 0x005C
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
LATENCY							
7	6	5	4	3	2	1	0
LATENCY							

LATENCY[x] (RO):

For each VXS payload port x this is the measured input latency (in 4ns units) of Fadc serial stream with respect to deassertion of SYNC.

6.7 VXS Serdes (Base Address 0x43C11000, 0x43C11100, …, 0x43C11F00)

Register: Ctrl

Address Offset: 0x0000
Size: 32bits
Reset State: 0x00000003

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	ERCNTRST	LOOPBACK
7	6	5	4	3	2	1	0
LOOPBACK		POWER_DOWN	-	-	-	RESET	GT_RESET

ERCNTRST (RW):

'1' - Serdes soft error counter reset
'0' - Serdes soft error counter run

LOOPBACK (RW):

0 - normal operation (no loopback)
1 - near end PCS loopback
2 - near end PMA loopback
3 - reserved
4 - far end PMA loopback
5 - reserved
6 - far end PCS loopback
7 - reserved

POWERDOWN (RW):

'1' - Serdes is not powered
'0' - Serdes is powered

RESET (RW):

'1' - Serdes link reset
'0' - Serdes link run

GT_RESET (RW):

'1' - Serdes transceiver reset
'0' - Serdes transceiver run

Register: Status

Address Offset: 0x0004
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	LINK_RST	RX_RST_DONE	TX_RST_DONE	TX_LOCK	-	-
15	14	13	12	11	10	9	8
SOFT_ERR_CNT							
7	6	5	4	3	2	1	0
-	CHUP	-	-	LANE1_UP	LANE0_UP	SOFT_ERR	HARD_ERR

LINK_RST (RO):
Indicates link is in process of being reset

RX_RST_DONE (RO):
Indicates rx serdes reset is done.

TX_RST_DONE (RO):
Indicates tx serdes reset is done.

TX_LOCK (RO):
'1' - TX PLL is locked
'0' - TX PLL not locked

SOFT_ERR_CNT (RO):
Soft rrror count since last link reset

CHUP (RO):
'1' - Serdes channel is up
'0' - Serdes channel is down

LANEx_UP (RO):
'1' - Serdes lane x is up
'0' - Serdes lane x is down

SOFT_ERR (RO):
'1' - Soft error seen
'0' - No soft error seen

HARD_ERR (RO):
'1' - Hard error exists (must reset Serdes)
'0' - No hard error

Register: DrpCtrl

Address Offset: 0x0008
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	EN1	EN0	WE	ADDR
23	22	21	20	19	18	17	16
ADDR							
15	14	13	12	11	10	9	8
DI							
7	6	5	4	3	2	1	0
DI							

EN1 (WO):
'1' - Execute DRP transaction for lane 1 (self clearing)
'0' - does nothing

EN0 (WO):
'1' - Execute DRP transaction for lane 0 (self clearing)
'0' - does nothing

WE (RW):
'1' - DRP transaction performs a write
'0' - DRP transaction performs a read

ADDR (RW):
DRP transaction address

DI (RW):
DRP transaction write data

Register: DrpStatus

Address Offset: 0x000C
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	RDY
15	14	13	12	11	10	9	8
DO							
7	6	5	4	3	2	1	0
DO							

RDY (RW):
DRP transaction result ready

DO (RO):
DRP transaction read data

6.8 QSFP Serdes (Base Address 0x43C12000, 0x43C12100, 0x43C12200 , 0x43C12300)

Register: Ctrl

Address Offset: 0x0000
Size: 32bits
Reset State: 0x00000003

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	ERCNTRST	LOOPBACK
7	6	5	4	3	2	1	0
LOOPBACK		POWER_DOWN	RESETL	MODSELL	LINKSTATUS	RESET	GT_RESET

ERCNTRST (RW):

'1' - Serdes soft error counter reset
'0' - Serdes soft error counter run

LOOPBACK (RW):

0 - normal operation (no loopback)
1 - near end PCS loopback
2 - near end PMA loopback
3 - reserved
4 - far end PMA loopback
5 - reserved
6 - far end PCS loopback
7 - reserved

POWERDOWN (RW):

'1' - Serdes is not powered
'0' - Serdes is powered

RESETL (RW):

'1' - QSFP module run
'0' - QSFP module reset

MODSELL (RW):

'1' - Deselect QSFP I2C interface
'0' - Select QSFP I2C interface

LINKSTATUS (RW):

'1' - Turn QSFP linkstatus LED on
'0' - Turn QSFP linkstatus LED off

RESET (RW):

'1' - Serdes link reset
'0' - Serdes link run

GT_RESET (RW):

'1' - Serdes transceiver reset
'0' - Serdes transceiver run

Register: Status

Address Offset: 0x0004
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	LINK_RST	RX_RST_DONE	TX_RST_DONE	TX_LOCK	-	-
15	14	13	12	11	10	9	8
SOFT_ERR_CNT							
7	6	5	4	3	2	1	0
-	CHUP	LANE3_UP	LANE2_UP	LANE1_UP	LANE0_UP	SOFT_ERR	HARD_ERR

LINK_RST (RO):
Indicates link is in process of being reset

RX_RST_DONE (RO):
Indicates rx serdes reset is done.

TX_RST_DONE (RO):
Indicates tx serdes reset is done.

TX_LOCK (RO):
'1' - TX PLL is locked
'0' - TX PLL not locked

SOFT_ERR_CNT (RO):
Soft rrror count since last link reset

CHUP (RO):
'1' - Serdes channel is up
'0' - Serdes channel is down

LANEx_UP (RO):
'1' - Serdes lane x is up
'0' - Serdes lane x is down

SOFT_ERR (RO):
'1' - Soft error seen
'0' - No soft error seen

HARD_ERR (RO):
'1' - Hard error exists (must reset Serdes)
'0' - No hard error

Register: DrpCtrl

Address Offset: 0x0008
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	EN3	EN2	EN1	EN0	WE	ADDR
23	22	21	20	19	18	17	16
ADDR							
15	14	13	12	11	10	9	8
DI							
7	6	5	4	3	2	1	0
DI							

ENx (WO):
'1' - Execute DRP transaction for lane x (self clearing)
'0' - does nothing

WE (RW):
'1' - DRP transaction performs a write
'0' - DRP transaction performs a read

ADDR (RW):
DRP transaction address

DI (RW):
DRP transaction write data

Register: DrpStatus

Address Offset: 0x000C
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	RDY
15	14	13	12	11	10	9	8
DO							
7	6	5	4	3	2	1	0
DO							

RDY (RW):
DRP transaction result ready

DO (RO):
DRP transaction read data

6.9 ECTrigger (Base Address 0x43C14100, 0x43C14200)

Register: Ctrl

Address Offset: 0x0000
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
TCOIN				DALITZ_MAX			
15	14	13	12	11	10	9	8
DALITZ_MAX						DALITZ_MIN	
7	6	5	4	3	2	1	0
DALITZ_MIN							

TCOIN (RW):

0 to 15: FADC hit timing coincidence in +/-4ns units to form 1D EC peaks. Also 1D EC peak timing coincidence to form 2D EC cluster.

DALITZ_MAX (RW):

0 to 127.875: 7.3 fixed point number representing maximum requirement of ECAL 1D peak sum Dalitz rule

DALITZ_MIN (RW):

0 to 127.875: 7.3 fixed point number representing minimum requirement of ECAL 1D peak sum Dalitz rule

6.10 Trigger Output (Base Address 0x43C15000)

Register: Latency

Address Offset: 0x0000
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	LATENCY		
7	6	5	4	3	2	1	0
LATENCY							

LATENCY (RW):

0 to 2047: Trigger output latency in 4ns ticks

Register: Width

Address Offset: 0x0004
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
WIDTH							

WIDTH (RW):

0 to 255: Trigger output width in 4ns ticks

Register: TriggerBusyScaler

Address Offset: 0x0010
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
SCALER							
23	22	21	20	19	18	17	16
SCALER							
15	14	13	12	11	10	9	8
SCALER							
7	6	5	4	3	2	1	0
SCALER							

SCALER (RO):

Number of 4ns ticks VTP busy was asserted due to trigger logic overflow protection.

6.11 V7 Event Builder (Base Address 0x43C15100)

Register: BlockSize

Address Offset: 0x0000
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
BLOCKSIZE							

BLOCKSIZE (RW):

0 to 255: Number of events to build in event block

Register: TriggerFifoBusyThreshold

Address Offset: 0x0004
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
BUSYLEVEL							

BUSYLEVEL (RW):

0 to 255: Threshold for number of unprocessed triggers to assert busy

Register: Lookback

Address Offset: 0x0008
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	LOOKBACK		
7	6	5	4	3	2	1	0
LOOKBACK							

LOOKBACK (RW):

0 to 2047: Readout window lookback in 4ns ticks

Register: WindowWidth

Address Offset: 0x000C
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8
-	-	-	-	-	WINDOW		
7	6	5	4	3	2	1	0
WINDOW							

WINDOW (RW):

0 to 2047: Readout window size in 4ns ticks