fADC125 register map

test firmware: Raw mode, PTW

Firmware version 0x0001 – 0x0100

**Main FPGA**(0x0000-0x0ffc)

Board ID – Status (0x0000)

0xADC12500

Swap Control – Control/Status (0x0004)

Any write other than “0” swaps.

Firmware version – Status (0x0008)

Main CSR - Control/Status (0x000C)

1-0 (R/W) – select clock

 00 – P2 clock

 01 – P0 clock

 10 – On

 11 – local 125Mhz – (default in firmware)

Power Control - Control/Status (0x0010)

Writing 0x3000ABCD turns “ON”,

Anything else turns “OFF”

DAC Control – Control (0x0014) – note: write only

0 – (W) –

1 – (W) – Serial Interface Chip Load (main and mezz chains)

2 – (W) – Serial Interface Clock Input (main and mezz chains)

3 – (W) –

 4 – (W) – Serial Interface Data Input (main chain)

5 – (W) –

 6 – (W) –

7– (W) –

 8 – (W) – Serial Interface Data Input (mezz chain)

Control/Status (0x0018 -0x001C) – used for testing

Serial – Status (0x0020-0x002C)

 0x0020 – main\_serial(47 downto 32)

 0x0024 – main\_serial(31 downto 0)

 0x0028 – mezz\_serial(47 downto 32)

 0x002C – mezz\_serial(31 downto 0)

Temperature – Status (0x0030-0x0034)

 0x0030 – main temperature

 0x0034 – mezz temperature

Geographical slot address – Status (0x0038)

0 – (R) – bit 0 of GAD

1 – (R) – bit 1 of GAD

2 – (R) – bit 2 of GAD

3 – (R) – bit 3 of GAD

4 – (R) – bit 4 of GAD

A32 base address – Status (0x003C)

Block CSR – Control/Status (0x0040)

0 – (R) –

 1 – (R) –

 2 – (R) – Block of Events ready for readout

 3 – (R) – BERR Status (1 = BERR asserted)

 4 – (R) – Token Status (1 = module has token)

 5 – (W) – Take Token

 6 – (W) – Pulse Soft Sync Reset

 7 – (W) – Pulse Soft Trigger (ACTUALLY bit 0 of 0xd010, on proc)

 8 – (W) – Pulse Soft Reset

 9 – (W) – Pulse Hard Reset

CTRL1 – Control/Status (0x0044)

1-0 (R/W) – Sync reset source select N/A, MOVED TO PROC (0xd00C)

00– (R/W) – N/A, moved to proc

 01 – (R/W) – N/A, moved to proc

 10 – (R/W) – N/A, moved to proc

 11 – (R/W) – N/A, moved to proc

2 – (R/W) – Enable BERR response

3 – (R/W) – Enable Multiboard protocol

4 – (R/W) – FIRST board in Multiblock system

5 – (R/W) – LAST board in Multiblock system

ADR32 – Control/Status (0x0048)

 0 – (R/W) – Enable 32-bit address decoding

 [1… 6] – (not used – read as 0)

 [15…7] – (R/W) – Base Address for 32-bit addressing mode (8 Mbyte total)

ADR\_MB – Multiblock Address for data access (0x004C)

 0 – (R/W) – Enable Multiblock address decoding

 1 – 6 – (not used – read as 0)

 [15…7] – (R/W) – Lower Limit address (ADR\_MIN) for Multiblock access

 16 – 22 – (not used – read as 0)

 [31…23] – (R/W) – Upper Limit address (ADR\_MAX) for Multiblock access

The board that has the TOKEN will respond with data when the VME address satisfies the following condition:

 ADR\_MIN ≤ Address < ADR\_MAX.

Module Busy Level – Control/Status (0x0050)

 [19…0] – Busy level (eight byte words)

 (External RAM word count > Busy level -> module busy = 1)

 [31] – Force module busy

Block Count – Control/Status (0x0054)

 [19…0] – (R) - number of event BLOCKS on board

**CONFIGURATION** **CSR** **(0x0058)** – (Firmware Update)

 [31] – (R/W) – vme program enable

 [30…28] – (R/W) – Reserved

 [27] – (R/W) – Reserved

 [26…24] – (R/W) – OPCODE (bit 31 = 1 also required)

 [23…9] – (R) – Reserved

 8 – (R) – Busy (operation in progress)

 [7…0] – (R) – Last Valid Data Read

**CONFIGURATION ADR/DATA (R/W)** **(0x005C)** – (Firmware Update)

 [31] – Execute

 [30…18] – Page address

 [17…8] – Byte address

 [7…0] – EPROM data to write

**Processor FPGA**(0xd000-0xdffc)

Processor Firmware Version – Status (0xd000)

Processor CSR – Control/Status (0xd004)

0 – (R) – busy status – not used

1 – (R/W) – processor csr clear – not used

2 – (R/W) – reset (testing) N/A

Trigger source – Control/Status (0xd008)

1 – 0 (R/W) – trig setup

 00 - trig on p0\_trg(0) rising

 01 - trig on SW TRIGGER (was internal timer)

 10 - trig on internal multiplicity sum

 11 - trig on p2\_trg(0) rising

CTRL2 – Control/Status (0xd00C)

 0– (R/W) – Enable Trigger to Module (source = Trigger source[1-0])

 1– (R/W) – Enable Sync Reset to Module N/A, MOVED TO FE (0x1004)

3-2 (R/W) – Sync reset source select - default “00”

00– (R/W) – P0 Connector (VXS)

 01 – (R/W) –

 10 – (R/W) – VME (software generated)

 11 – (R/W) – no source

Control/Status (0xd010) – used for testing

 0-R/W – SW TRIGGER

BLOCK SIZE – Control/Status (0xd014)

 [15…0] - (R/W) – number of events in a BLOCK.

 Stored Event Count ≥ BLOCK SIZE → BLOCK CSR[2] = 1.

 [31…16] – (not used)

Trigger Count – Control/Status (0xd018)

 [30…0] – (R) – total trigger count

11– (R/W) – reset count

Event Count – Control/Status (0xd01C)

 [23…0] – (R) – number of events on board

CLOCK\_125 COUNT REGISTER (0xd020)

 0 – (W) – Write ‘0’ resets the counter. Write ‘1’ initiates 20us counting interval.

 [31 - 0] – (R) – CLK\_250 counter value. (Should be 5000 after count interval.)

SYNC\_IN\_P0 COUNT REGISTER (0xd024)

 0 – (W) – Write ‘0’ resets the counter.

[31 - 0] – (R) – SYNC\_IN\_P0 counter value.

TRIG2\_IN\_P0 COUNT REGISTER (0xd028)

 0 – (W) – Write ‘0’ resets the counter.

[31 - 0] – (R) – TRIG1\_IN\_P0 counter value.

**FE PFGA**(0x1000-0xcffc)

FE Firmware Version – Status (0x1000)

FE Test Register (0x1004)

 0– (R) – reset (testing) read

1– (R/W) – Collect On default on

2– (R/W) – Enable Sync Reset to Module default on, all rst sync

FE Asynchronous ADC read – Status (0xN020-0xN034) – not used

FE FIFO ADC read – Status (0xN040-0xN054) – not used

PTW (0x1058)

 [8 - 0] – (R/W) – Window Width

PL (0x105C)

 [15 - 0] – (R/W) – # of samples back from trigger point

PTW DAT BUF LAST ADDR (0x1060)

 [11 - 0] – (R/W) – Last Address of secondary buffer (see calculation 1.0 below)

PTW MAX BUF (0x1064)

[7 - 0] – (R/W) – Max # of unprocessed PTW blocks to store in secondary buffer (see calculation 2.0 below)

NSB (0x1068)

[12 - 0] – (R/W) – # of samples before (including) trigger point to include in data processing

NSA (0x106C)

[13 - 0] – (R/W) – # of samples after trigger point to include in data processing

TET 1 (0xN070)

[11 - 0] – (R/W) – Trigger energy threshold

TET 2 (0xN074)

[11 - 0] – (R/W) – Trigger energy threshold

TET 3 (0xN078)

[11 - 0] – (R/W) – Trigger energy threshold

TET 4 (0xN07C)

[11 - 0] – (R/W) – Trigger energy threshold

TET 5 (0xN080)

[11 - 0] – (R/W) – Trigger energy threshold

TET 6 (0xN084)

[11 - 0] – (R/W) – Trigger energy threshold

CONFIG1 (0x1088)

[2 - 0] – (R/W) – Process mode select

 “000” = Select option 1

 “001” = Select option 2

“010” = Select option 3

“011” = Select option 4

“111” = Run option 1 the option 4

 [3] – (R/W) – Run (Collect On) default ‘1’

 [6-5] – (R/W) – Number of pulses in Mode 1 and 2

 [7] – (R/W) – Test Mode (playback)

Trigger Number (0xN08C)

[15- 0] – (R) – Trigger number

 Calculation - 1.0

 PTW MAX BUF = INT(2016/(PTW+8))

 Where:

 2016 = Number of addresses in secondary buffer

 PTW = Window width in samples (Even #?)

 Calculation - 2.0

 PTW DATA BUF LAST ADR =

PTW MAX BUF\*(PTW+8)-1

 Where:

 6 = 4 addresses for time stamp, 2 for Trigger Number

 Number of bytes per trigger = PTW\*125MHz